

### FEATURES

- Double Side Cooling
- High Surge Capability

### APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

### KEY PARAMETERS

$V_{DRM}$	<b>1800V</b>
$I_{T(AV)}$	<b>4920A</b>
$I_{TSM}$	<b>63100A</b>
$dV/dt^*$	<b>2000V/<math>\mu</math>s</b>
$dI/dt$	<b>300A/<math>\mu</math>s</b>

\* Higher  $dV/dt$  selections are available on request

### VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages $V_{DRM}$ and $V_{RRM}$ (V)	Conditions
DCR4940V18	1800	$T_{vj} = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$ , $I_{DRM} = I_{RRM} = 200\text{mA}$ , $V_{DRM}, V_{RRM} t_p = 10\text{ms}$ $V_{DSM} \& V_{RSM} =$ $V_{DRM} \& V_{RRM} + 100\text{V}$ respectively
DCR4940V16	1600	

Lower voltage grades available.

### ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

#### DCR4940V18

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

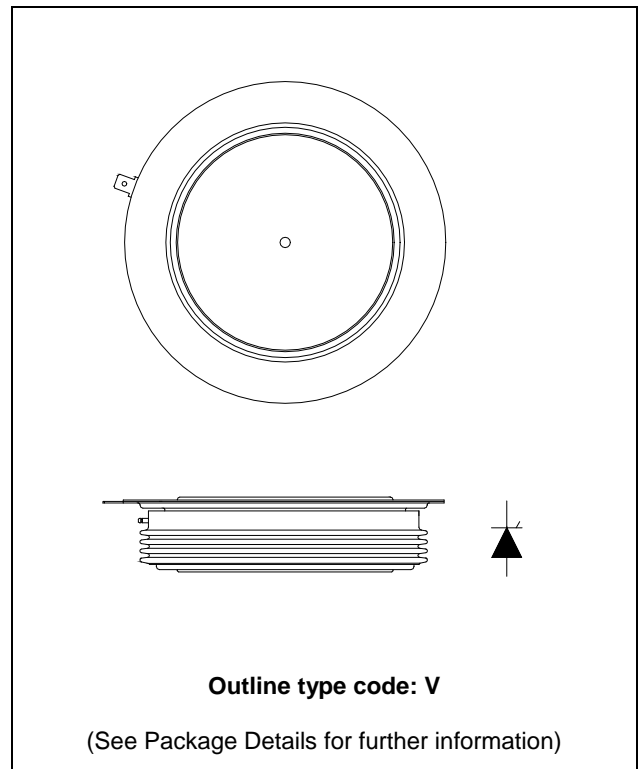


Fig. 1 Package outline

## CURRENT RATINGS

$T_{case} = 60^{\circ}\text{C}$  unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
<b>Double Side Cooled</b>				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	4920	A
$I_{T(RMS)}$	RMS value	-	7730	A
$I_r$	Continuous (direct) on-state current	-	6910	A

## SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
$I_{TSM}$	Surge (non-repetitive) on-state current	10ms half sine, $T_{case} = 125^{\circ}\text{C}$ $V_R = 0$	63.1	kA
$I^2t$	$I^2t$ for fusing		19.9	MA <sup>2</sup> s

## THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
$R_{th(j-c)}$	Thermal resistance - junction to case	Double side cooled	DC	-	7.5	$^{\circ}\text{C}/\text{kW}$
		Single side cooled	Anode DC	-	13.0	$^{\circ}\text{C}/\text{kW}$
			Cathode DC	-	17.8	$^{\circ}\text{C}/\text{kW}$
$R_{th(c-h)}$	Thermal resistance - case to heatsink	Clamping force 54kN (with mounting compound)	Double side	-	2	$^{\circ}\text{C}/\text{kW}$
			Single side	-	4	$^{\circ}\text{C}/\text{kW}$
$T_{vj}$	Virtual junction temperature	Blocking $V_{DRM} / V_{RRM}$	-	125	$^{\circ}\text{C}$	
$T_{stg}$	Storage temperature range		-55	125	$^{\circ}\text{C}$	
$F_m$	Clamping force		48	59	kN	

**DYNAMIC CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
<b>I<sub>RRM</sub>/I<sub>DRM</sub></b>	Peak reverse and off-state current	At V <sub>RRM</sub> /V <sub>DRM</sub> , T <sub>case</sub> = 125°C	-	200	mA	
<b>V<sub>TM</sub></b>	Instantaneous forward voltage	At 4000A peak, T <sub>j</sub> = 125°C	1.02	1.08	V	
<b>dV/dt</b>	Max. linear rate of rise of off-state voltage	To 67% V <sub>DRM</sub> , T <sub>j</sub> = 125°C, gate open	-	2000	V/μs	
<b>di/dt</b>	Rate of rise of on-state current	From 67% V <sub>DRM</sub> to 2x I <sub>T(AV)</sub> Gate source 30V, 10Ω tr < 0.5μs, T <sub>j</sub> = 125°C	Repetitive 50Hz	-	150	A/μs
			Non-repetitive	-	300	A/μs
<b>V<sub>T(TO)</sub></b>	Threshold voltage - Low level	500A to 3500A at T <sub>case</sub> = 125°C	-	0.71	V	
	Threshold voltage - High level	3500A to 8000A at T <sub>case</sub> = 125°C	-	0.85	V	
<b>r<sub>T</sub></b>	On-state slope resistance - low level	500A to 3500A at T <sub>case</sub> = 125°C	-	0.10	mΩ	
	On-state slope resistance - High level	3500A to 8000A at T <sub>case</sub> = 125°C	-	0.06	mΩ	
<b>t<sub>gd</sub></b>	Delay time	V <sub>D</sub> = 67% V <sub>DRM</sub> , gate source 30V, 10Ω tr = 0.5μs, T <sub>j</sub> = 25°C	-	3	μs	
<b>t<sub>q</sub></b>	Turn-off time	T <sub>j</sub> = 125°C, V <sub>R</sub> = 200V, di/dt = 1A/μs, dV <sub>DR</sub> /dt = 20V/μs linear		250	μs	
<b>Q<sub>s</sub></b>	Stored charge	I <sub>T</sub> = 2000A, T <sub>j</sub> = 125°C, di/dt = 1A/μs	980	2090	μC	
<b>I<sub>RR</sub></b>	Reverse recovery current	V <sub>R(peak)</sub> ~ 1100V, V <sub>RM</sub> ~ 720V	23	35	A	
<b>I<sub>L</sub></b>	Latching current	T <sub>j</sub> = 25°C, V <sub>D</sub> = 5V	-	3	A	
<b>I<sub>H</sub></b>	Holding current	T <sub>j</sub> = 25°C, R <sub>G-K</sub> = ∞, I <sub>TM</sub> = 500A, I <sub>T</sub> = 5A	-	300	mA	

## GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
$V_{GT}$	Gate trigger voltage	$V_{DRM} = 5V, T_{case} = 25^{\circ}C$	1.5	V
$V_{GD}$	Gate non-trigger voltage	At 50% $V_{DRM}, T_{case} = 125^{\circ}C$	0.4	V
$I_{GT}$	Gate trigger current	$V_{DRM} = 5V, T_{case} = 25^{\circ}C$	250	mA
$I_{GD}$	Gate non-trigger current	At 50% $V_{DRM}, T_{case} = 125^{\circ}C$	10	mA

## CURVES

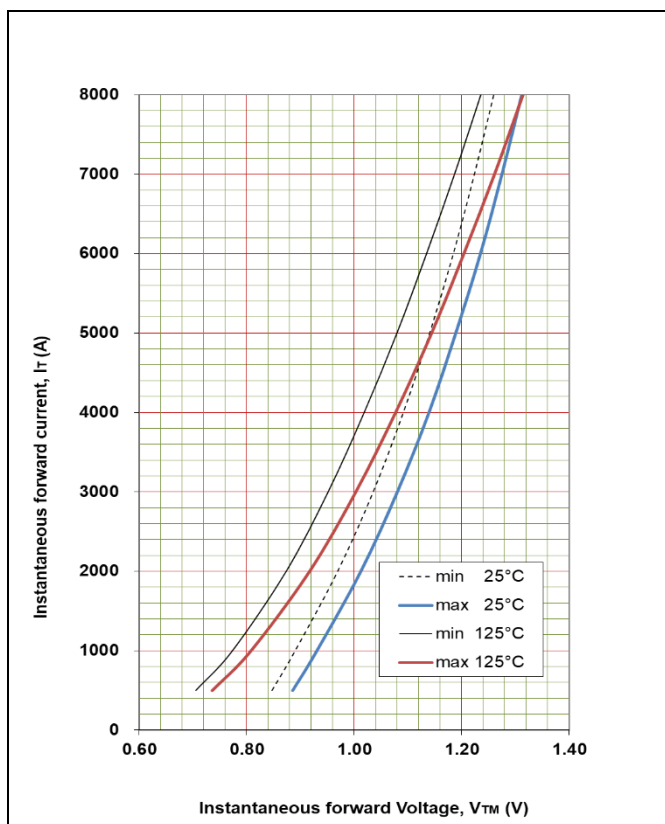


Fig. 2 Maximum & minimum on state characteristics

## $V_{TM}$ EQUATION

$$V_{TM} = A + B \cdot \ln(I_T) + C \cdot I_T + D \cdot \sqrt{I_T}$$

Where  $A = 0.628851$

$B = -0.014195$

$C = 0.000005$

$D = 0.008621$

These values are valid for  $T_j = 125^{\circ}C$  for  $I_T$  500A to 8000A

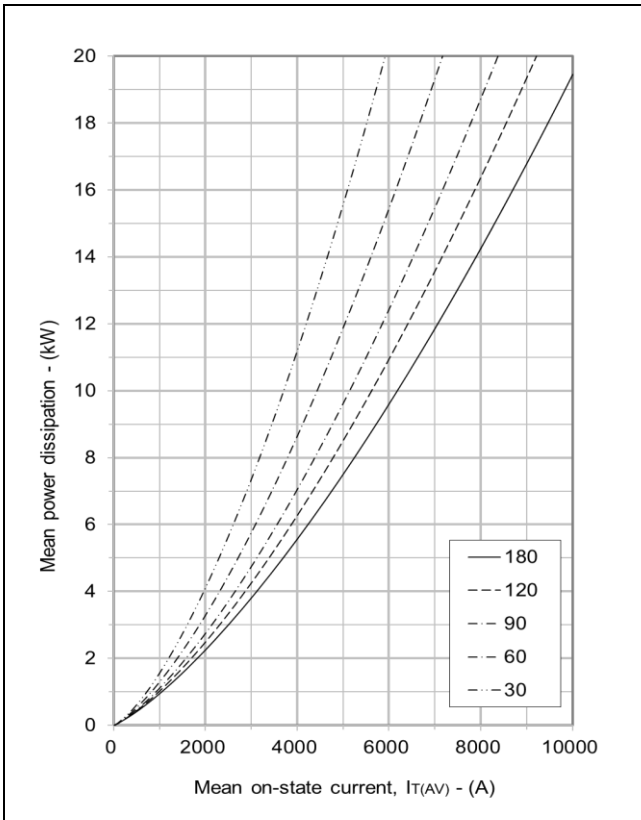


Fig. 3 On-state power dissipation - sine wave

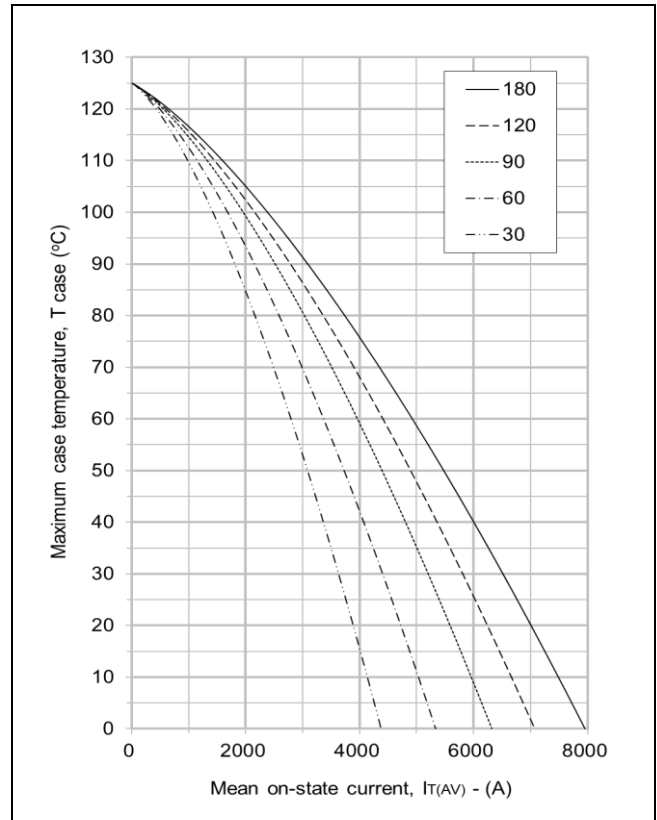


Fig. 4 Maximum permissible case temperature, double side cooled - sine wave

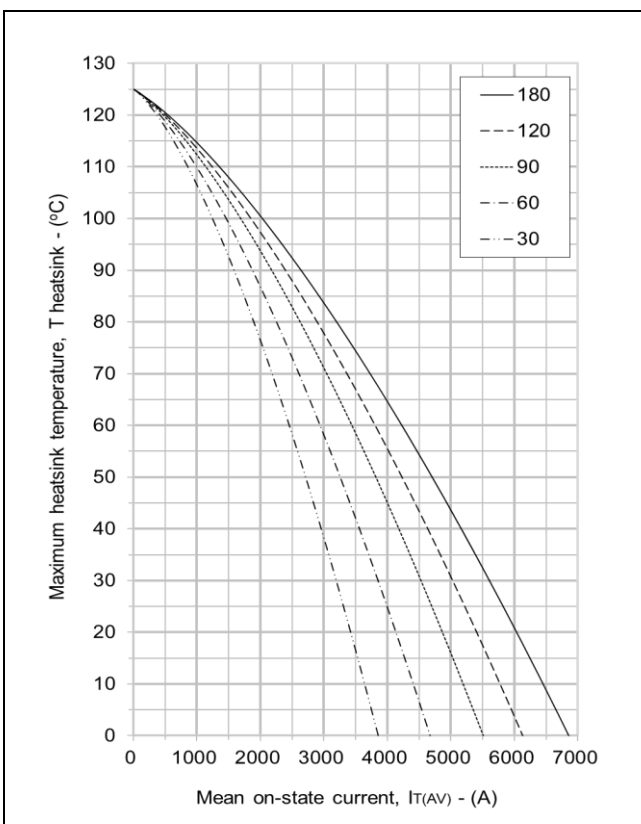


Fig. 5 Maximum permissible heatsink temperature, double side cooled - sine wave

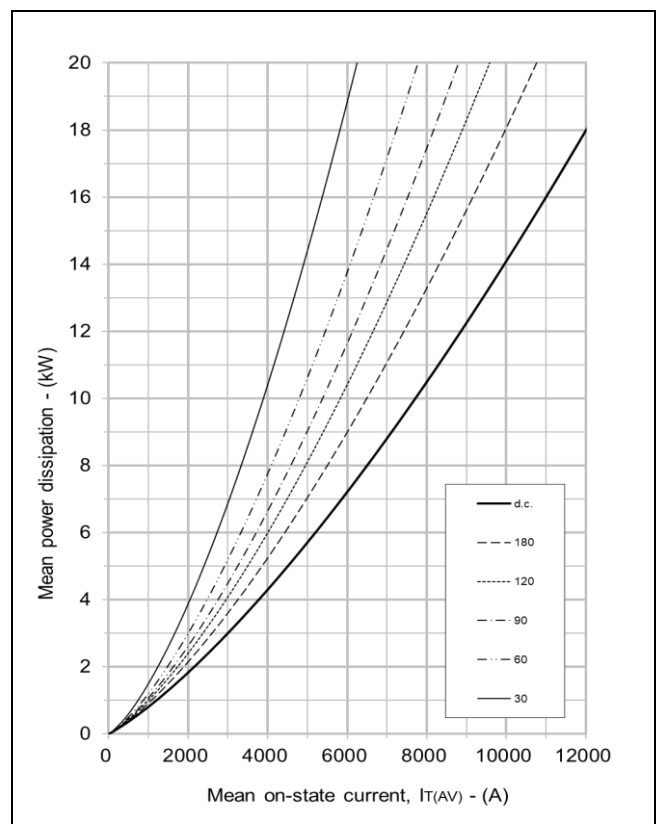


Fig. 6 On-state power dissipation - rectangular wave

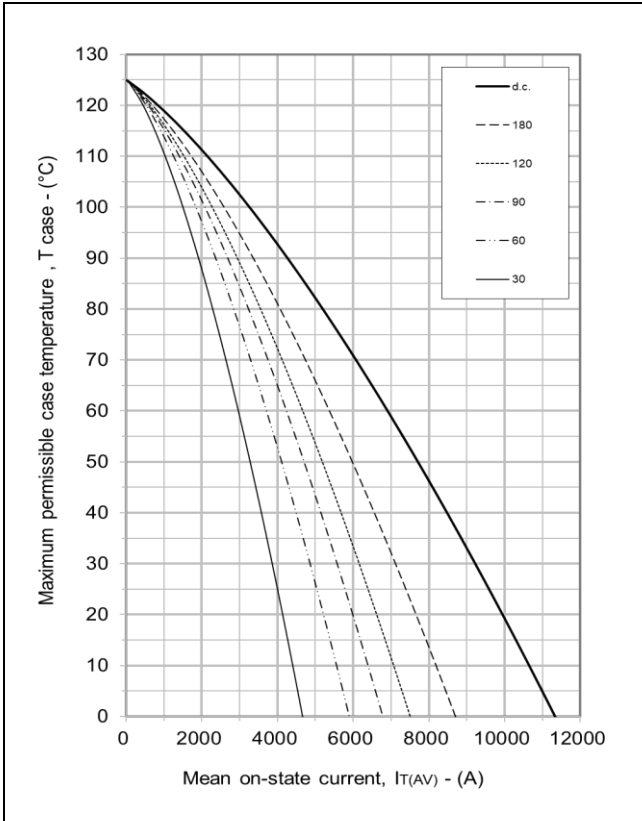


Fig. 7 Maximum permissible case temperature, double side cooled - rectangular wave

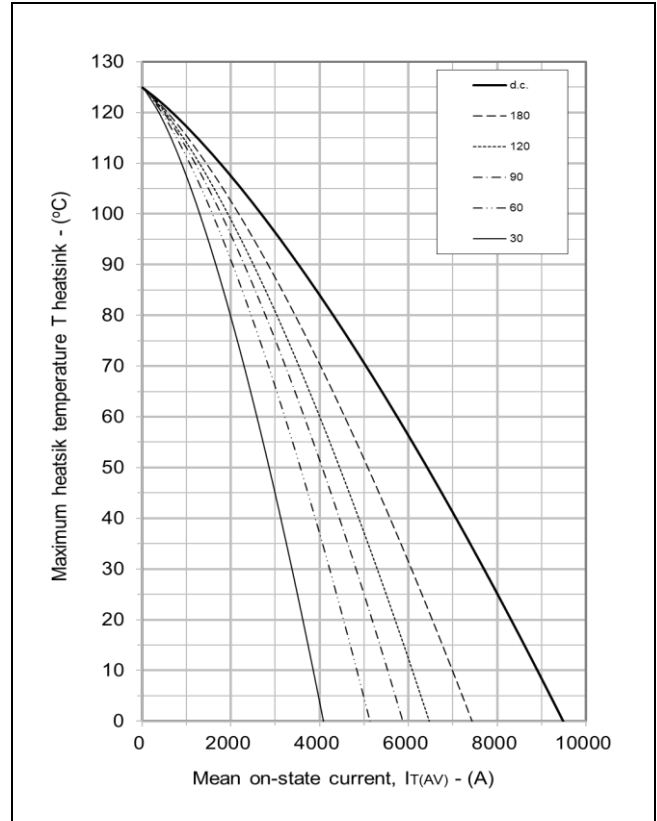


Fig. 8 Maximum permissible heatsink temperature, double side cooled - rectangular wave

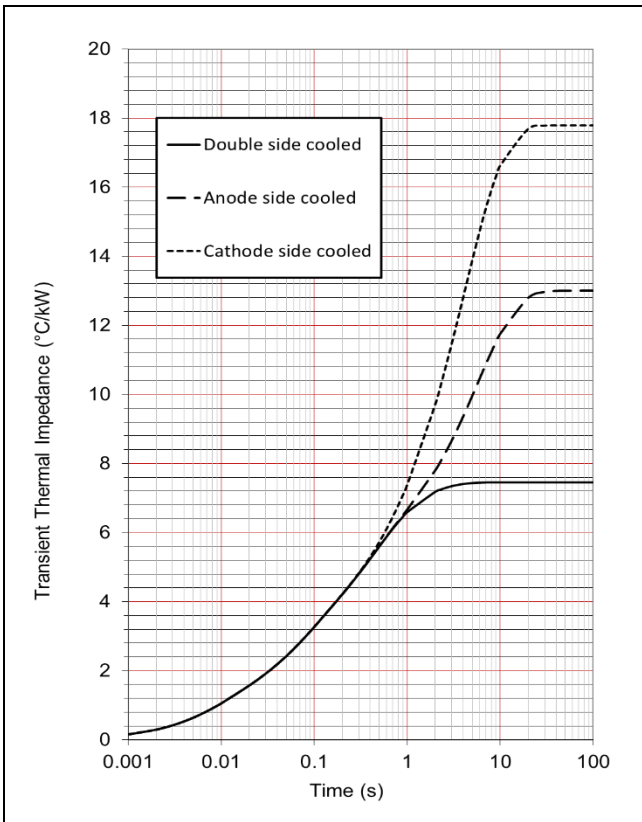


Fig. 9 Maximum (limit) transient thermal impedance – junction to case (degC/kW)

		1	2	3	4
Double side cooled	Ri(°C/kW)	0.921	1.830	3.402	1.304
	Ti(s)	0.008	0.058	0.408	1.209
Anode side cooled	Ri(°C/kW)	0.903	1.672	3.010	7.427
	Ti(s)	0.008	0.054	0.314	5.624
Cathode side cooled	Ri(°C/kW)	0.948	2.066	1.688	13.085
	Ti(s)	0.008	0.065	0.389	4.145

$$Z_{th} = \sum_{i=1}^{i=4} R_i \cdot \left(1 - \exp\left(-\frac{T}{T_i}\right)\right)$$

$\Delta R_{th(j-c)}$  Conduction

Tables show the increments of thermal resistance  $R_{th(j-c)}$  when the device operates at conduction angles other than d.c.

Double side cooling			Anode Side Cooling			Cathode Sided Cooling		
$\phi^\circ$	$\Delta Z_{th}(z)$		$\phi^\circ$	$\Delta Z_{th}(z)$		$\phi^\circ$	$\Delta Z_{th}(z)$	
	sine	rect		sine	rect		sine	rect
180	1.34	0.88	180	1.34	0.88	180	1.33	0.88
120	1.57	1.30	120	1.57	1.30	120	1.57	1.29
90	1.83	1.54	90	1.84	1.54	90	1.83	1.53
60	2.08	1.81	60	2.08	1.81	60	2.07	1.80
30	2.27	2.11	30	2.28	2.11	30	2.26	2.10
15	2.36	2.28	15	2.37	2.28	15	2.35	2.26

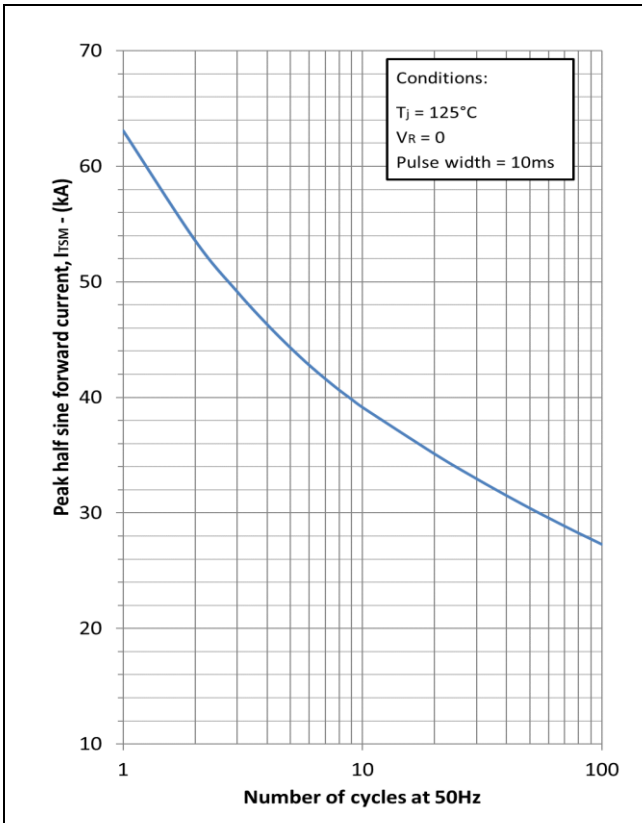


Fig. 10 Multi-cycle surge current

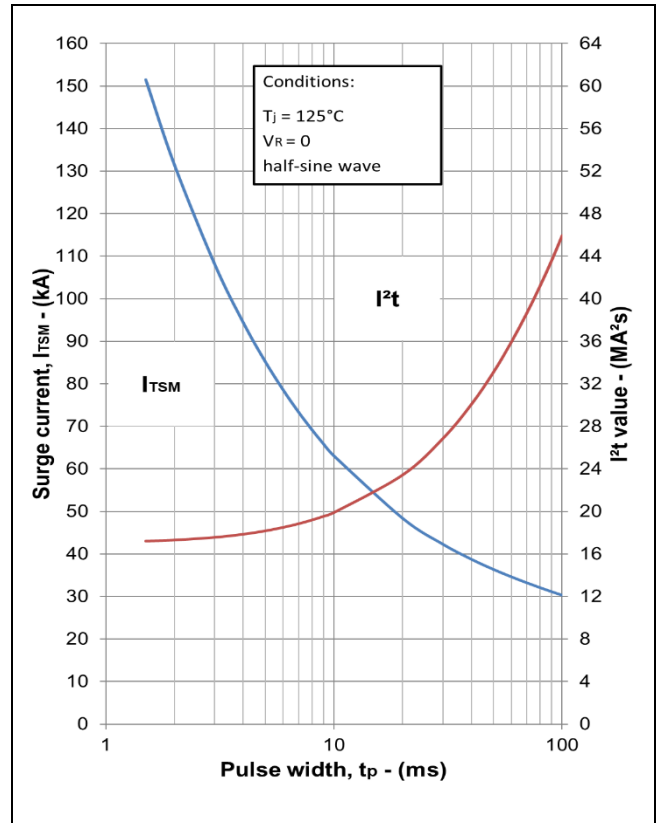


Fig. 11 Single-cycle surge current

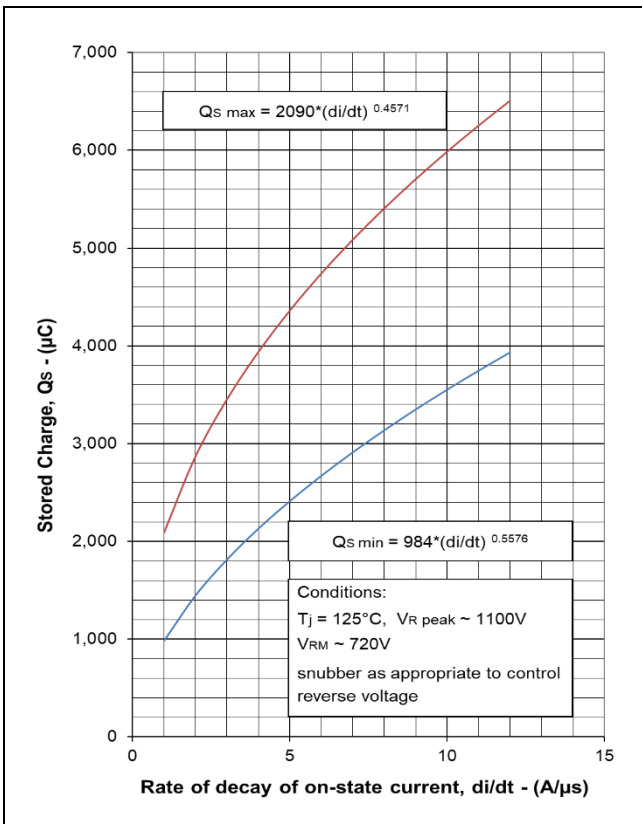


Fig. 12 Stored charge

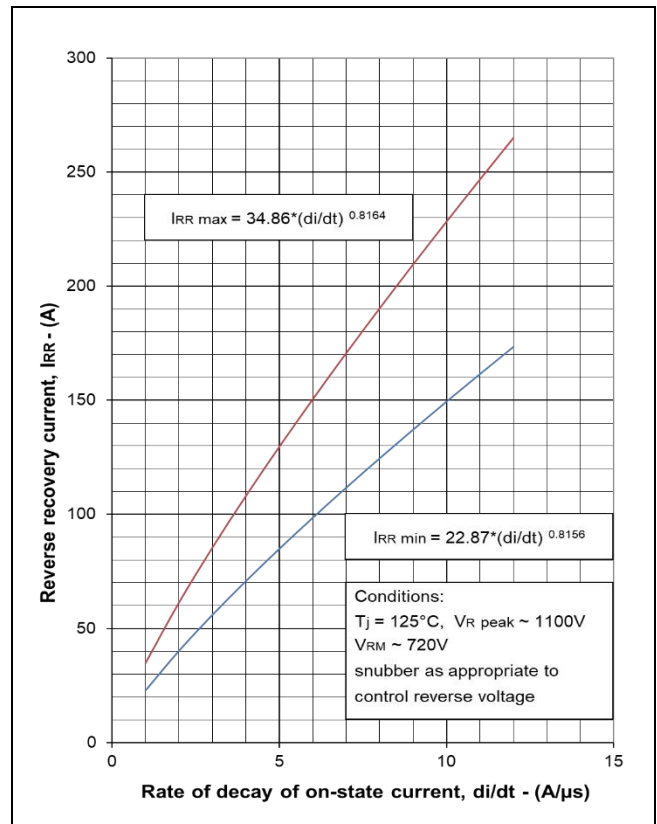


Fig. 13 Reverse recovery current

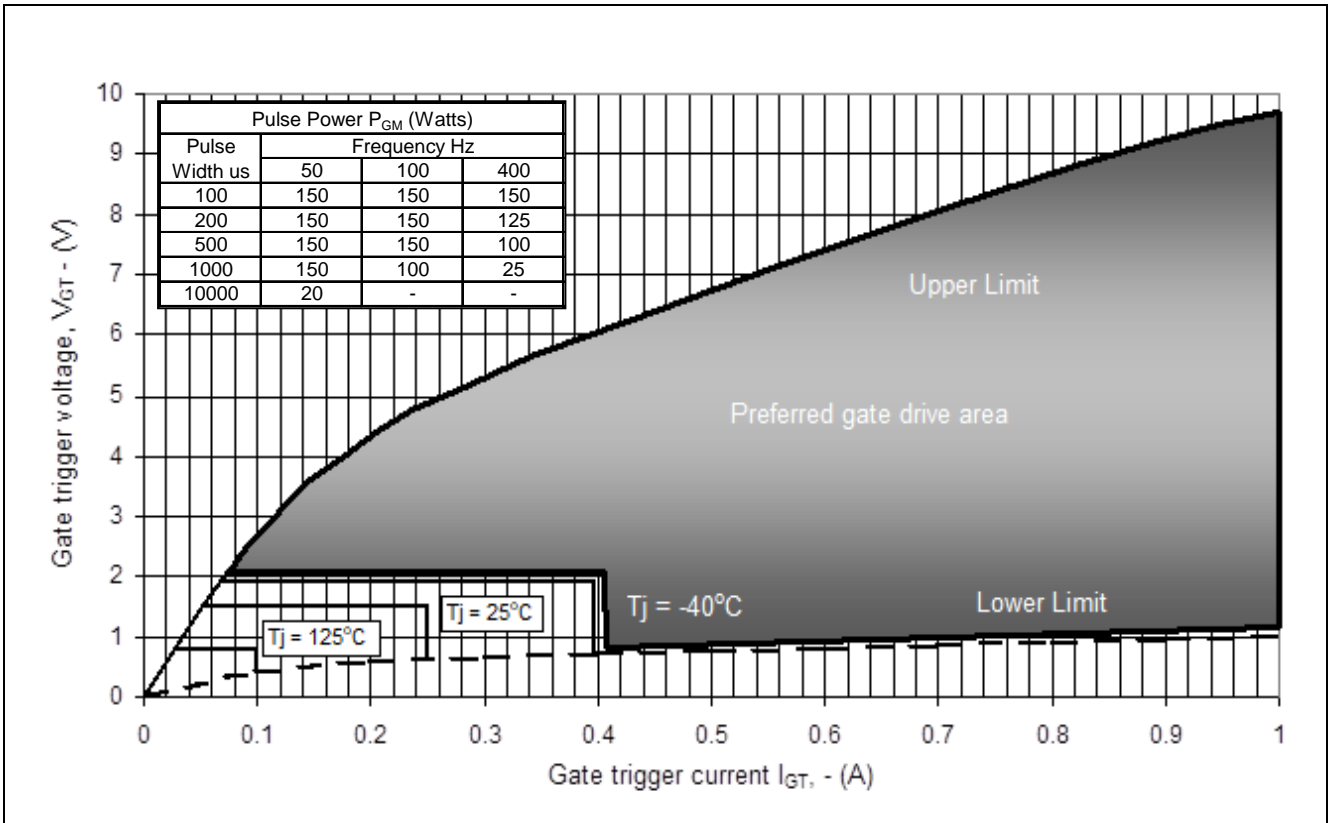


Fig. 14 Gate characteristics

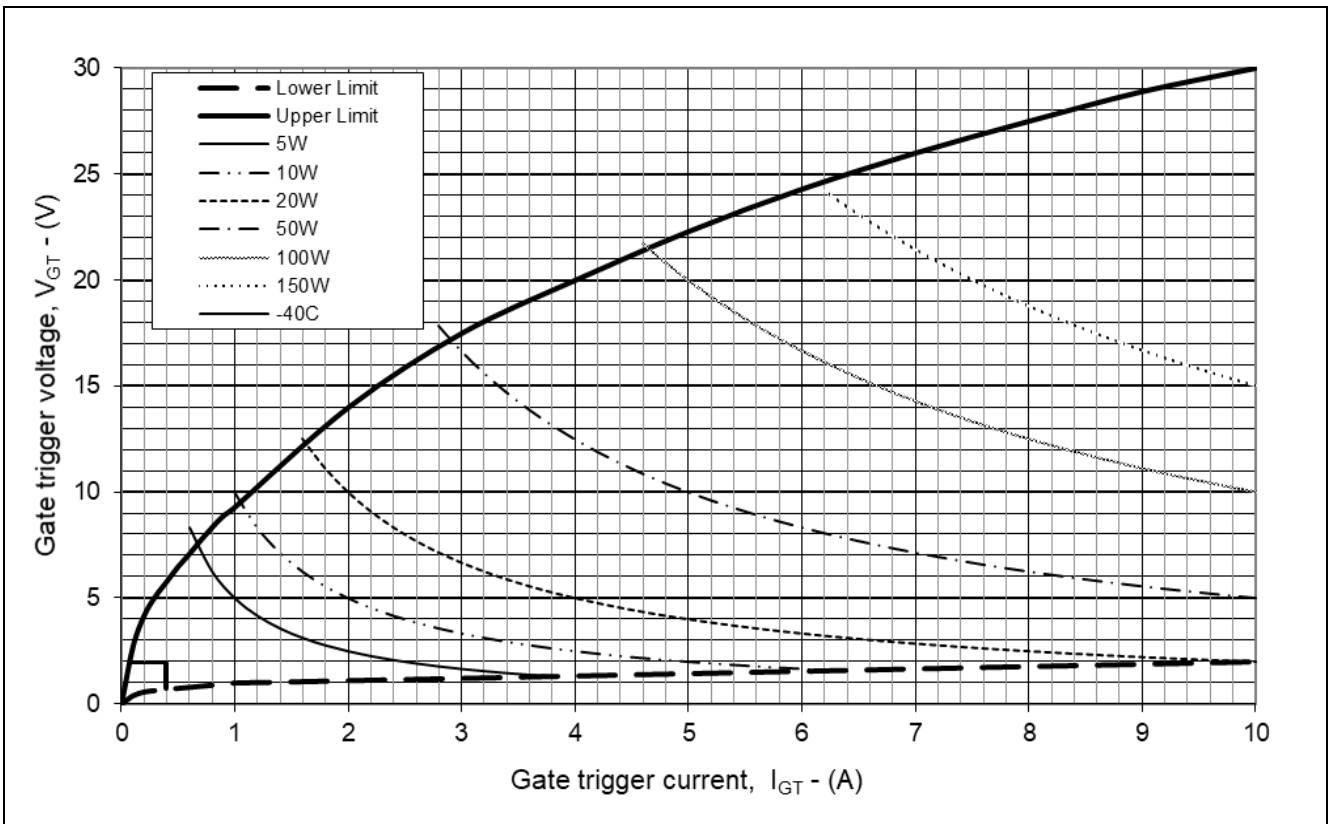


Fig. 15 Gate characteristics



**PACKAGE DETAILS**

For further package information, please contact Customer services.

All dimensions in mm, unless stated otherwise.

DO NOT SCALE

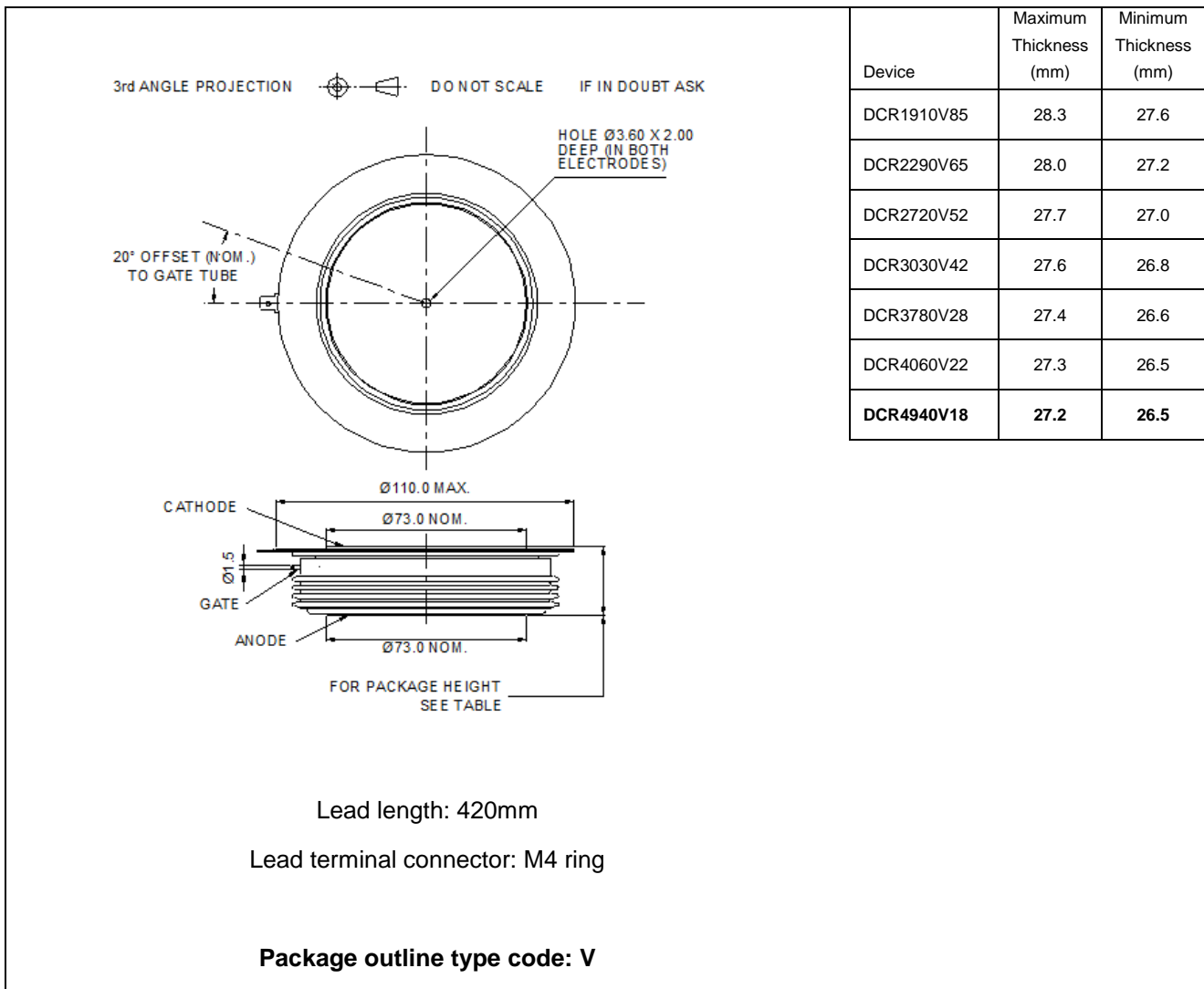


Fig. 16 Package outline

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