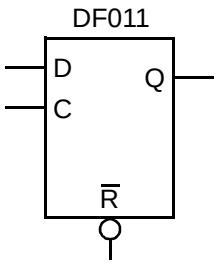
Description

DF011 is a static, master-slave D flip-flop. RESET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	D	C	Q
L	X	X	L
H	L	↑	L
H	H	↑	H
H	X	L	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	1.0
RN	1.0

Equivalent Gates 8.0

HDL Syntax

Verilog ..... DF011 *inst_name* (Q, C, D, RN);

VHDL..... *inst_name*: DF011 port map (Q, C, D, RN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	17.8	Eq-load

See page 2-15 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	2	5	8	10 (max)
C	Q	t_{PLH} t_{PHL}	0.72 0.57	0.78 0.62	0.94 0.72	1.09 0.81	1.19 0.86
RN	Q	t_{PHL}	0.31	0.35	0.45	0.54	0.59

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

AMI5HG 0.5 micron CMOS Gate Array

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	0.71
Min C Width	Low	t_w	0.71
Min RN Width	Low	t_w	0.54
Min D Setup		t_{su}	0.43
Min D Hold		t_h	0.18
Min RN Setup		t_{su}	0.36
Min RN Hold		t_h	0.34

Logic Schematic