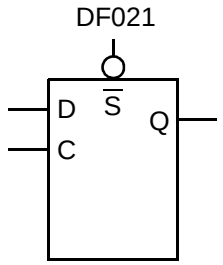
Description

DF021 is a static, master-slave D flip-flop. SET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	D	C	Q
L	X	X	H
H	L	↑	L
H	H	↑	H
H	X	L	NC

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
C	1.0
SN	2.1

Equivalent Gates 7.0

HDL Syntax

Verilog.....DF021 *inst_name* (Q, C, D, SN);

VHDL..... *inst_name*: DF021 port map (Q, C, D, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	14.5	Eq-load

See page 2-15 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	2	5	8	10 (max)
C	Q	t_{PLH} t_{PHL}	0.66 0.61	0.69 0.65	0.79 0.80	0.87 0.96	0.92 1.08
SN	Q	t_{PLH}	0.14	0.17	0.27	0.36	0.40

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	0.66
Min C Width	Low	t_w	0.76
Min SN Width	Low	t_w	0.60
Min D Setup		t_{su}	0.48
Min D Hold		t_h	0.17
Min SN Setup		t_{su}	0.19
Min SN Hold		t_h	0.50

Logic Schematic