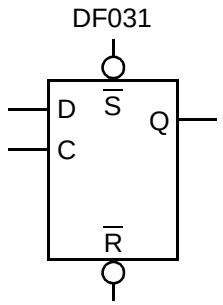
Description

DF031 is a static, master-slave D flip-flop. SET and RESET are asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	RN	D	C	Q
L	L	X	X	IL
L	H	X	X	H
H	L	X	X	L
H	H	L	↑	L
H	H	H	↑	H
H	H	X	L	NC

NC = No Change
IL = Illegal

Pin Loading

	Equivalent Load
D	1.0
C	1.0
SN	2.1
RN	2.2

Core Logic

Equivalent Gates 9.0

HDL Syntax

Verilog ..... DF031 *inst_name* (Q, D, RN, SN);

VHDL..... *inst_name*: DF031 port map (Q, D, RN, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	18.9	Eq-load

See page 2-15 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	2	5	8	10 (max)
C	Q	t_{PLH} t_{PHL}	0.65 0.63	0.68 0.68	0.77 0.84	0.86 1.00	0.92 1.09
RN	Q	t_{PHL}	0.79	0.84	1.00	1.16	1.27
SN	Q	t_{PLH}	0.14	0.18	0.29	0.39	0.45

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	0.65
Min C Width	Low	t_w	0.76
Min RN Width	Low	t_w	0.78
Min SN Width	Low	t_w	0.73
Min D Setup		t_{su}	0.49
Min D Hold		t_h	0.16
Min RN Setup		t_{su}	0.36
Min RN Hold		t_h	0.32
Min SN Setup		t_{su}	0.22
Min SN Hold		t_h	0.48

Logic Schematic