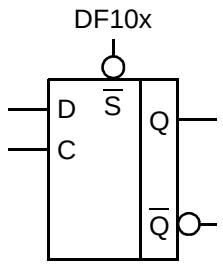
Description

DF10x is a family of static, master-slave D flip-flops. SET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	D	C	Q	QN
L	X	X	H	L
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

HDL Syntax

Verilog.....DF10x *inst_name* (Q, QN, C, D, SN);

VHDL..... *inst_name*: DF10x port map (Q, QN, C, D, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DF101	DF102	DF104	DF106
D	1.0	1.0	1.0	1.0
C	1.0	1.0	1.0	1.0
SN	2.1	2.1	3.2	3.2

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static IDD (TJ = 85°C) (nA)	EQLpd (Eq-load)
DF101	8.0	TBD	17.8
DF102	9.0	TBD	21.0
DF104	13.0	TBD	32.5
DF106	15.0	TBD	39.3

a. See page 2-15 for power equation.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
DF101	From: C To: Q	t_{PLH} t_{PHL}	0.69 0.58	0.80 0.72	0.92 0.87	1.06 1.04	1.17 1.16
	From: C To: QN	t_{PLH} t_{PHL}	0.86 0.88	0.93 0.97	1.05 1.09	1.20 1.25	1.32 1.37
	From: SN To: Q	t_{PLH}	0.57	0.68	0.79	0.93	1.04
	From: SN To: QN	t_{PHL}	0.29	0.39	0.52	0.68	0.80
	Number of Equivalent Loads		**1**	**8**	**15**	**22**	**30 (max)**
DF102	From: C To: Q	t_{PLH} t_{PHL}	0.72 0.62	0.85 0.81	0.96 0.94	1.05 1.06	1.15 1.18
	From: C To: QN	t_{PLH} t_{PHL}	1.03 0.97	1.12 1.10	1.20 1.20	1.28 1.30	1.37 1.40
	From: SN To: Q	t_{PLH}	0.65	0.75	0.85	0.96	1.09
	From: SN To: QN	t_{PHL}	0.31	0.46	0.57	0.67	0.77
	Number of Equivalent Loads		**1**	**14**	**28**	**42**	**56 (max)**
DF104	From: C To: Q	t_{PLH} t_{PHL}	0.70 0.68	0.84 0.81	0.94 0.91	1.04 1.03	1.12 1.16
	From: C To: QN	t_{PLH} t_{PHL}	0.97 0.99	1.02 1.08	1.10 1.14	1.20 1.25	1.32 1.37
	From: SN To: Q	t_{PLH}	0.83	0.91	1.01	1.13	1.28
	From: SN To: QN	t_{PHL}	0.26	0.40	0.51	0.60	0.71
	Number of Equivalent Loads		**1**	**21**	**42**	**62**	**83 (max)**
DF106	From: C To: Q	t_{PLH} t_{PHL}	0.78 0.66	0.91 0.81	1.01 0.91	1.09 1.01	1.18 1.13
	From: C To: QN	t_{PLH} t_{PHL}	1.13 1.06	1.25 1.18	1.33 1.31	1.39 1.42	1.44 1.54
	From: SN To: Q	t_{PLH}	1.00	1.14	1.23	1.31	1.39
	From: SN To: QN	t_{PHL}	0.31	0.45	0.56	0.65	0.75

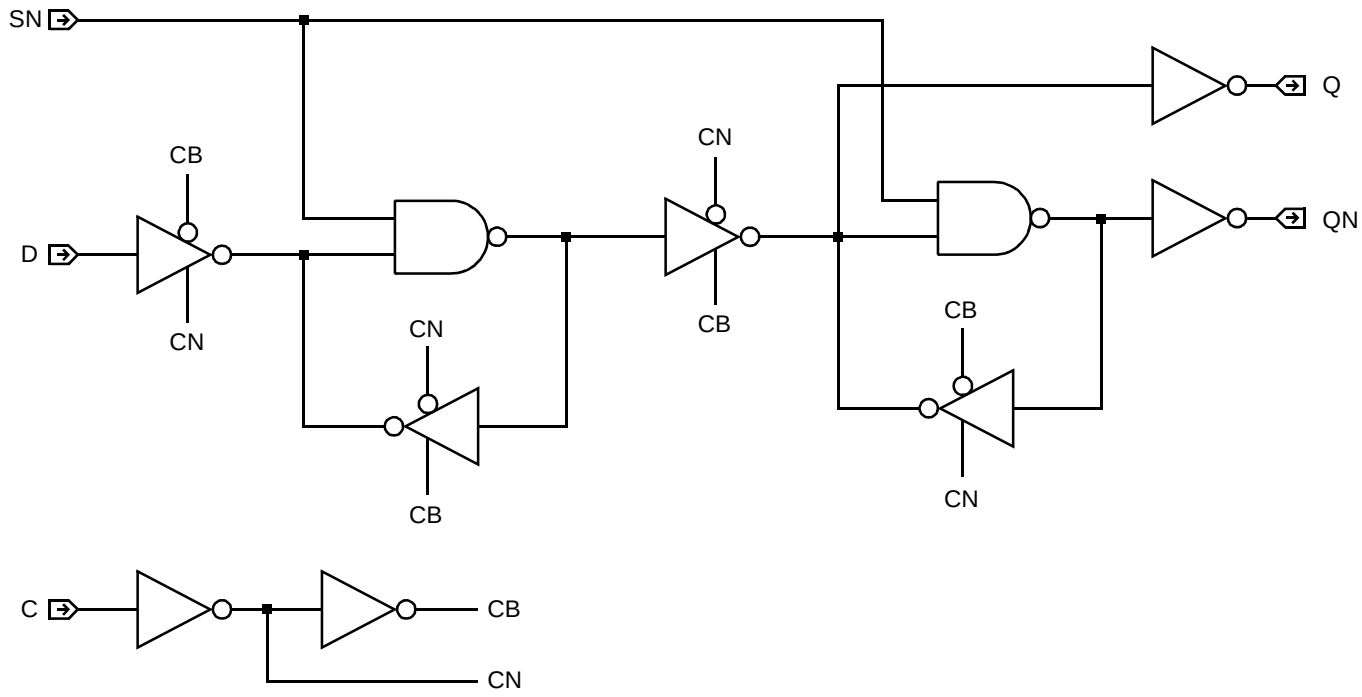
Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF101	DF102	DF104	DF106
Min C Width	High	t_w	0.72	0.84	0.81	0.97
Min C Width	Low	t_w	0.75	0.75	0.84	0.84
Min SN Width		t_w	0.42	0.50	0.63	0.76
Min D Setup		t_{su}	0.48	0.48	0.52	0.52
Min D Hold		t_h	0.17	0.17	0.19	0.19
Min SN Setup		t_{su}	0.19	0.19	0.23	0.23
Min SN Hold		t_h	0.49	0.49	0.54	0.54

Logic Schematic



Core Logic