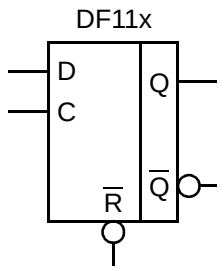
AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

DF11x is a family of static, master-slave D flip-flops. RESET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

RN	D	C	Q	QN
L	X	X	L	H
H	L	↑	L	H
H	H	↑	H	L
H	X	L	NC	NC

NC = No Change

HDL Syntax

Verilog.....DF11x *inst_name* (Q, QN, C, D, RN);

VHDL.....inst_DF11x : DF11x port map (Q, QN, C, D, RN);

Pin Loading

Pin Name	Equivalent Loads			
	DF111	DF112	DF114	DF116
D	1.0	1.0	1.0	1.0
C	1.0	1.0	1.0	1.0
RN	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF111	9.0	TBD	21.1
DF112	10.0	TBD	24.4
DF114	14.0	TBD	37.0
DF116	16.0	TBD	43.5

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
DF111	From: C To: Q	t_{PLH} t_{PHL}	0.69 0.60	0.80 0.74	0.92 0.89	1.06 1.05	1.16 1.18
	From: C To: QN	t_{PLH} t_{PHL}	0.76 0.99	0.86 1.11	0.97 1.24	1.10 1.40	1.19 1.51
	From: RN To: Q	t_{PHL}	0.81	0.95	1.09	1.25	1.36
	From: RN To: QN	t_{PLH}	0.42	0.52	0.64	0.78	0.89
	Number of Equivalent Loads		**1**	**8**	**15**	**22**	**30 (max)**
DF112	From: C To: Q	t_{PLH} t_{PHL}	0.72 0.64	0.85 0.82	0.95 0.96	1.05 1.07	1.15 1.19
	From: C To: QN	t_{PLH} t_{PHL}	0.88 1.11	0.99 1.25	1.08 1.37	1.16 1.48	1.25 1.60
	From: RN To: Q	t_{PHL}	0.89	1.08	1.21	1.31	1.42
	From: RN To: QN	t_{PLH}	0.44	0.56	0.66	0.75	0.87
	Number of Equivalent Loads		**1**	**14**	**28**	**42**	**56 (max)**
DF114	From: C To: Q	t_{PLH} t_{PHL}	0.69 0.62	0.85 0.81	0.96 0.94	1.04 1.05	1.11 1.16
	From: C To: QN	t_{PLH} t_{PHL}	0.82 1.11	0.90 1.22	0.99 1.33	1.09 1.44	1.20 1.54
	From: RN To: Q	t_{PHL}	1.19	1.31	1.46	1.62	1.78
	From: RN To: QN	t_{PLH}	0.46	0.55	0.66	0.75	0.86
	Number of Equivalent Loads		**1**	**21**	**42**	**62**	**83 (max)**
DF116	From: C To: Q	t_{PLH} t_{PHL}	0.75 0.65	0.87 0.85	0.99 1.01	1.08 1.13	1.18 1.23
	From: C To: QN	t_{PLH} t_{PHL}	0.99 1.22	1.06 1.37	1.14 1.49	1.21 1.59	1.28 1.69
	From: RN To: Q	t_{PHL}	1.33	1.58	1.75	1.86	1.96
	From: RN To: QN	t_{PLH}	0.51	0.60	0.69	0.78	0.88

AMI5HG 0.5 micron CMOS Gate Array

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF111	DF112	DF114	DF116
Min C Width	High	t_w	0.78	0.90	0.89	1.01
Min C Width	Low	t_w	0.71	0.71	0.79	0.79
Min RN Width		t_w	0.54	0.54	0.63	0.63
Min D Setup		t_{su}	0.43	0.43	0.47	0.47
Min D Hold		t_h	0.17	0.17	0.19	0.19
Min RN Setup		t_{su}	0.36	0.36	0.44	0.44
Min RN Hold		t_h	0.34	0.34	0.36	0.37

Logic Schematic