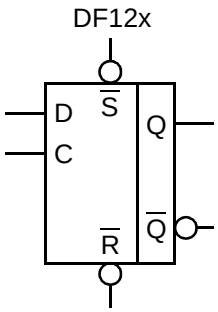
Description

DF12x is a family of static, master-slave D flip-flops. SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

SN	RN	D	C	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	L	↑	L	H
H	H	H	↑	H	L
H	H	X	L	NC	NC

IL = Illegal NC = No Change

HDL Syntax

Verilog ..... DF12x *inst_name* (Q, QN, C, D, RN, SN);

VHDL..... *inst_name*: DF12x port map (Q, QN, C, D, RN, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DF121	DF122	DF124	DF126
D	1.0	1.0	1.0	1.0
C	1.0	1.0	1.0	1.0
SN	2.1	2.1	2.1	2.1
RN	2.2	2.2	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF121	10.0	TBD	22.2
DF122	11.0	TBD	25.6
DF124	14.0	TBD	36.1
DF126	16.0	TBD	43.0

a. See page 2-15 for power equation.

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Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
DF121	From: C To: Q	t_{PLH} t_{PHL}	0.68 0.58	0.78 0.71	0.91 0.86	1.05 1.03	1.16 1.16
	From: C To: QN	t_{PLH} t_{PHL}	0.86 0.87	0.94 0.96	1.06 1.09	1.21 1.25	1.33 1.37
	From: SN To: Q	t_{PLH}	0.73	0.84	0.96	1.10	1.21
	From: SN To: QN	t_{PHL}	0.29	0.42	0.55	0.70	0.82
	From: RN To: Q	t_{PHL}	0.76	0.89	1.04	1.21	1.34
	From: RN To: QN	t_{PLH}	1.03	1.10	1.22	1.37	1.50
	Number of Equivalent Loads		**1**	**8**	**15**	**22**	**30 (max)**
DF122	From: C To: Q	t_{PLH} t_{PHL}	0.71 0.62	0.85 0.80	0.96 0.94	1.05 1.05	1.16 1.17
	From: C To: QN	t_{PLH} t_{PHL}	1.05 0.97	1.14 1.09	1.22 1.20	1.29 1.31	1.39 1.43
	From: SN To: Q	t_{PLH}	0.83	0.96	1.07	1.17	1.28
	From: SN To: QN	t_{PHL}	0.32	0.47	0.59	0.70	0.81
	From: RN To: Q	t_{PHL}	0.79	0.96	1.10	1.22	1.35
	From: RN To: QN	t_{PLH}	1.20	1.32	1.40	1.47	1.54

	Number of Equivalent Loads		1	14	28	42	56 (max)
DF124	From: C To: Q	t_{PLH} t_{PHL}	1.20 1.13	1.30 1.24	1.40 1.34	1.49 1.44	1.58 1.54
	From: C To: QN	t_{PLH} t_{PHL}	0.81 0.77	0.89 0.99	0.98 1.13	1.08 1.25	1.18 1.38
	From: SN To: Q	t_{PLH}	0.51	0.62	0.71	0.80	0.89
	From: SN To: QN	t_{PHL}	0.81	0.99	1.10	1.19	1.29
	From: RN To: Q	t_{PHL}	0.78	0.93	1.04	1.13	1.23
	From: RN To: QN	t_{PLH}	1.13	1.22	1.31	1.40	1.49
	Number of Equivalent Loads		**1**	**21**	**42**	**62**	**83 (max)**
DF126	From: C To: Q	t_{PLH} t_{PHL}	1.30 1.23	1.41 1.34	1.50 1.45	1.58 1.54	1.67 1.63
	From: C To: QN	t_{PLH} t_{PHL}	0.92 1.01	1.00 1.13	1.08 1.24	1.17 1.35	1.27 1.47
	From: SN To: Q	t_{PLH}	0.58	0.68	0.77	0.87	0.97
	From: SN To: QN	t_{PHL}	0.91	1.11	1.21	1.30	1.40
	From: RN To: Q	t_{PHL}	0.88	1.02	1.15	1.24	1.34
	From: RN To: QN	t_{PLH}	1.20	1.29	1.39	1.49	1.60

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

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Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF121	DF122	DF124	DF126
Min C Width	High	t_w	0.71	0.86	0.79	0.80
Min C Width	Low	t_w	0.76	0.76	0.76	0.77
Min RN Width	Low	t_w	0.87	1.02	0.62	0.62
Min SN Width	Low	t_w	0.57	0.64	0.45	0.45
Min D Setup		t_{su}	0.49	0.49	0.50	0.50
Min D Hold		t_h	0.16	0.16	0.16	0.16
Min RN Setup		t_{su}	0.36	0.36	0.37	0.37
Min RN Hold		t_h	0.33	0.33	0.33	0.33
Min SN Setup		t_{su}	0.22	0.22	0.23	0.23
Min SN Hold		t_h	0.49	0.49	0.48	0.49

Logic Schematic