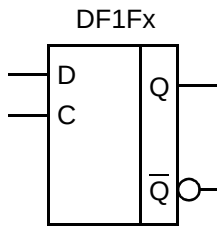
Description

DF1Fx is a family of static, master-slave D flip-flops without SET or RESET. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

D	C	Q	QN
X	X	L	H
L	↑	L	H
H	↑	H	L
X	L	NC	NC

NC = No Change

HDL Syntax

Verilog ..... DF1Fx *inst_name* (Q, QN, C, D);

VHDL..... *inst_name*: DF1Fx port map (Q, QN, C, D)

Pin Loading

Pin Name	Equivalent Loads			
	DF1F1	DF1F2	DF1F4	DF1F6
D	1.0	1.0	1.0	1.0
C	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF1F1	7.0	TBD	17.4
DF1F2	8.0	TBD	20.7
DF1F4	11.0	TBD	30.7
DF1F6	14.0	TBD	38.9

a. See page 2-15 for power equation.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
DF1F1	From: C To: Q	t_{PLH} t_{PHL}	0.69 0.60	0.78 0.74	0.91 0.90	1.06 1.06	1.18 1.19
	From: C To: QN	t_{PLH} t_{PHL}	0.77 0.88	0.86 0.98	0.97 1.11	1.10 1.27	1.20 1.39
	Number of Equivalent Loads		**1**	**8**	**15**	**22**	**30 (max)**
DF1F2	From: C To: Q	t_{PLH} t_{PHL}	0.71 0.63	0.84 0.81	0.95 0.94	1.05 1.07	1.17 1.19
	From: C To: QN	t_{PLH} t_{PHL}	0.89 0.98	1.00 1.11	1.09 1.21	1.17 1.31	1.27 1.40
	Number of Equivalent Loads		**1**	**14**	**28**	**42**	**56 (max)**
DF1F4	From: C To: Q	t_{PLH} t_{PHL}	1.15 1.04	1.25 1.11	1.33 1.22	1.39 1.34	1.46 1.47
	From: C To: QN	t_{PLH} t_{PHL}	0.78 0.86	0.87 1.03	0.95 1.14	1.04 1.23	1.12 1.31
	Number of Equivalent Loads		**1**	**21**	**42**	**62**	**83 (max)**
DF1F6	From: C To: Q	t_{PLH} t_{PHL}	1.19 1.10	1.25 1.23	1.34 1.32	1.43 1.39	1.53 1.45
	From: C To: QN	t_{PLH} t_{PHL}	0.84 0.95	0.93 1.12	1.02 1.22	1.11 1.30	1.21 1.39

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell DF1F1	DF1F2	DF1F4	DF1F6
Min C Width	High	t_w	0.72	0.81	0.75	0.79
Min C Width	Low	t_w	0.70	0.70	0.69	0.69
Min D Setup		t_{su}	0.42	0.42	0.42	0.42
Min D Hold		t_h	0.17	0.17	0.17	0.17

Logic Schematic