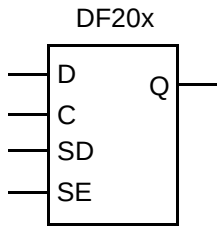
AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

DF20x is a family of static, master-slave, multiplexed scan D flip-flops without SET or RESET. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	SD	SE	Q
↑	H	X	L	H
↑	L	X	L	L
↑	X	H	H	H
↑	X	L	H	L
L	X	X	X	NC

NC = No Change

HDL Syntax

Verilog ..... DF20x *inst_name* (Q, C, D, SD, SE);

VHDL..... *inst_name*: DF20x port map (Q, C, D, SD, SE);

Pin Loading

Pin Name	Equivalent Loads	
	DF201	DF202
C	1.0	1.0
D	1.0	1.0
SD	1.0	1.0
SE	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF201	8.0	TBD	18.1
DF202	9.0	TBD	19.8

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
DF201	From: C	t_{PLH}	0.65	0.74	0.86	0.99	1.10
	To: Q	t_{PHL}	0.55	0.66	0.80	0.95	1.07
	Number of Equivalent Loads		**1**	**8**	**15**	**22**	**30 (max)**
DF202	From: C	t_{PLH}	0.69	0.81	0.92	1.01	1.10
	To: Q	t_{PHL}	0.57	0.73	0.85	0.96	1.08

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell	
			DF201	DF202
Min C Width	High	t_w	0.65	0.67
Min C Width	Low	t_w	0.81	0.81
Min D Setup		t_{su}	0.67	0.67
Min D Hold		t_h	0.16	0.16
Min SD Setup		t_{su}	0.67	0.67
Min SD Hold		t_h	0.16	0.16
Min SE Setup		t_{su}	0.81	0.81
Min SE Hold		t_h	0.16	0.16

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Logic Schematic