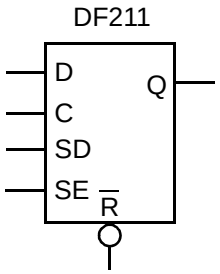
Description

DF211 is a static, master-slave, multiplexed scan D flip-flop. RESET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	Q
↑	H	H	X	L	H
↑	L	H	X	L	L
↑	X	H	H	H	H
↑	X	H	L	H	L
X	X	L	X	X	L
L	X	H	X	X	NC

NC = No Change

Pin Loading

	Equivalent Load
C	1.0
D	1.0
RN	1.0
SD	1.0
SE	2.1

Equivalent Gates 11.0

HDL Syntax

Verilog ..... DF211 *inst_name* (Q, C, D, RN, SD, SE);

VHDL..... *inst_name*: DF211 port map (Q, C, D, RN, SD, SE);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	22.3	Eq-load

See page 2-15 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	2	5	8	10 (max)
C	Q	t_{PLH} t_{PHL}	0.74 0.58	0.79 0.63	0.94 0.74	1.10 0.82	1.21 0.87
RN	Q	t_{PHL}	0.32	0.36	0.46	0.55	0.60

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

AMI5HG 0.5 micron CMOS Gate Array

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	0.74
Min C Width	Low	t_w	0.85
Min RN Width	Low	t_w	0.53
Min D Setup		t_{su}	0.69
Min D Hold		t_h	0.17
Min SD Setup		t_{su}	0.69
Min SD Hold		t_h	0.17
Min SE Setup		t_{su}	0.84
Min SE Hold		t_h	0.17
Min RN Setup		t_{su}	0.37
Min RN Hold		t_h	0.33

Logic Schematic