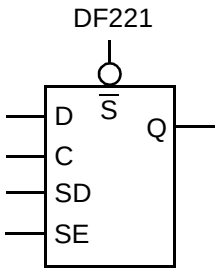
Description

DF221 is a static, master-slave, multiplexed scan D flip-flop. SET is asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	SD	SE	SN	Q
↑	H	X	L	H	H
↑	L	X	L	H	L
↑	X	H	H	H	H
↑	X	L	H	H	L
X	X	X	X	L	H
L	X	X	X	H	NC

NC = No Change

Pin Loading

	Equivalent Load
C	1.0
D	1.0
SD	1.0
SE	2.1
SN	2.1

Core Logic

Equivalent Gates 11.0

HDL Syntax

Verilog ..... DF221 *inst_name* (Q, C, D, SD, SE, SN);

VHDL..... *inst_name*: DF221 port map (Q, C, D, SD, SE, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	19.5	Eq-load

See page 2-15 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	2	5	8	10 (max)
C	Q	t_{PLH} t_{PHL}	0.67 0.64	0.70 0.69	0.79 0.85	0.88 1.00	0.95 1.10
SN	Q	t_{PLH}	0.15	0.18	0.27	0.35	0.41

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	0.67
Min C Width	Low	t_w	0.95
Min SN Width	Low	t_w	0.40
Min D Setup		t_{su}	0.79
Min D Hold		t_h	0.17
Min SD Setup		t_{su}	0.79
Min SD Hold		t_h	0.17
Min SE Setup		t_{su}	0.95
Min SE Hold		t_h	0.17
Min SN Setup		t_{su}	0.21
Min SN Hold		t_h	0.48

Logic Schematic