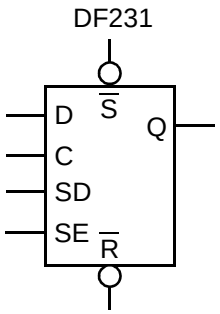
Description

DF231 is a static, master-slave, multiplexed scan D flip-flop. SET and RESET are asynchronous and active low. Output is unbuffered and changes state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	SN	Q
↑	H	H	X	L	H	H
↑	L	H	X	L	H	L
↑	X	H	H	H	H	H
↑	X	H	L	H	H	L
X	X	L	X	X	H	L
X	X	H	X	X	L	H
X	X	L	X	X	L	IL
L	X	H	X	X	H	NC

NC = No Change IL = Illegal Condition

Pin Loading

	Equivalent Load
C	1.0
D	1.0
RN	2.1
SD	1.0
SE	2.1
SN	2.1

Equivalent Gates 12.0

HDL Syntax

Verilog ..... DF231 *inst_name* (Q, C, D, RN, SD, SE, SN);

VHDL..... *inst_name*: DF231 port map (Q, C, D, RN, SD, SE, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	22.7	Eq-load

See page 2-15 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	2	5	8	10 (max)
C	Q	t_{PLH} t_{PHL}	0.66 0.62	0.69 0.69	0.78 0.84	0.88 0.97	0.95 1.06
RN	Q	t_{PHL}	0.77	0.82	0.97	1.13	1.24
SN	Q	t_{PLH}	0.14	0.17	0.26	0.36	0.42

Delay (ns)

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

AMI5HG 0.5 micron CMOS Gate Array

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min C Width	High	t_w	0.67
Min C Width	Low	t_w	0.96
Min RN Width	Low	t_w	0.78
Min SN Width	Low	t_w	0.55
Min D Setup		t_{su}	0.79
Min D Hold		t_h	0.17
Min SD Setup		t_{su}	0.79
Min SD Hold		t_h	0.17
Min SE Setup		t_{su}	0.95
Min SE Hold		t_h	0.17
Min RN Setup		t_{su}	0.36
Min RN Hold		t_h	0.33
Min SN Setup		t_{su}	0.24
Min SN Hold		t_h	0.49

Logic Schematic