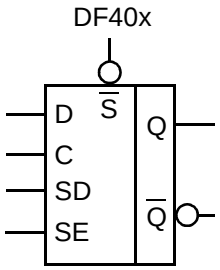
Description

DF40x is a family of static, master-slave, multiplexed scan D flip-flops. SET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	SD	SE	SN	Q	QN
↑	H	X	L	H	H	L
↑	L	X	L	H	L	H
↑	X	H	H	H	H	L
↑	X	L	H	H	L	H
X	X	X	X	L	H	L
L	X	X	X	H	NC	NC

NC = No Change

HDL Syntax

Verilog ..... DF40x *inst_name* (Q, QN, C, D, SD, SE, SN);

VHDL..... *inst_name*: DF40x port map (Q, QN, C, D, SD, SE, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DF401	DF402	DF404	DF406
C	1.0	1.0	1.0	1.0
D	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.1	2.1	2.2	2.2
SN	2.1	2.1	3.1	3.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF401	11.0	TBD	22.8
DF402	12.0	TBD	26.1
DF404	15.0	TBD	37.3
DF406	18.0	TBD	44.2

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
DF401	From: C To: Q	t_{PLH} t_{PHL}	0.70 0.58	0.80 0.73	0.92 0.89	1.07 1.06	1.18 1.19
	From: C To: QN	t_{PLH} t_{PHL}	0.87 0.90	0.97 1.00	1.09 1.13	1.22 1.27	1.33 1.40
	From: SN To: Q	t_{PLH}	0.60	0.70	0.82	0.97	1.08
	From: SN To: QN	t_{PHL}	0.30	0.42	0.55	0.70	0.82
	Number of Equivalent Loads		**1**	**8**	**15**	**22**	**30 (max)**
DF402	From: C To: Q	t_{PLH} t_{PHL}	0.72 0.64	0.85 0.83	0.97 0.97	1.07 1.08	1.18 1.21
	From: C To: QN	t_{PLH} t_{PHL}	1.05 1.01	1.13 1.12	1.23 1.22	1.32 1.33	1.42 1.45
	From: SN To: Q	t_{PLH}	0.67	0.78	0.88	0.98	1.08
	From: S To: QN	t_{PHL}	0.33	0.47	0.58	0.68	0.80
	Number of Equivalent Loads		**1**	**14**	**28**	**42**	**56 (max)**
DF404	From: C To: Q	t_{PLH} t_{PHL}	0.76 0.60	0.88 0.79	0.98 0.92	1.07 1.04	1.17 1.14
	From: C To: QN	t_{PLH} t_{PHL}	0.99 0.96	1.09 1.09	1.18 1.20	1.27 1.28	1.35 1.37
	From: SN To: Q	t_{PLH}	0.83	0.94	1.06	1.18	1.28
	From: SN To: QN	t_{PHL}	0.29	0.43	0.53	0.62	0.71

	Number of Equivalent Loads		1	21	42	62	83 (max)
DF406	From: C To: Q	t_{PLH} t_{PHL}	0.79 0.68	0.91 0.88	1.02 1.02	1.11 1.13	1.21 1.24
	From: C To: QN	t_{PLH} t_{PHL}	1.16 1.06	1.28 1.19	1.37 1.30	1.44 1.39	1.51 1.47
	From: SN To: Q	t_{PLH}	1.00	1.12	1.24	1.33	1.43
	From: SN To: QN	t_{PHL}	0.31	0.46	0.57	0.67	0.76

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Core Logic

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF401	DF402	DF404	DF406
Min C Width	High	t_w	0.73	0.86	0.84	1.00
Min C Width	Low	t_w	0.95	0.95	1.00	1.00
Min SN Width	Low	t_w	0.44	0.52	0.64	0.76
Min D Setup		t_{su}	0.79	0.79	0.80	0.80
Min D Hold		t_h	0.17	0.17	0.19	0.19
Min SD Setup		t_{su}	0.79	0.79	0.80	0.80
Min SD Hold		t_h	0.17	0.17	0.19	0.19
Min SE Setup		t_{su}	0.95	0.95	0.95	0.95
Min SE Hold		t_h	0.17	0.17	0.19	0.19
Min SN Setup		t_{su}	0.21	0.21	0.24	0.24
Min SN Hold		t_h	0.48	0.48	0.54	0.54

AMI5HG 0.5 micron CMOS Gate Array

Logic Schematic