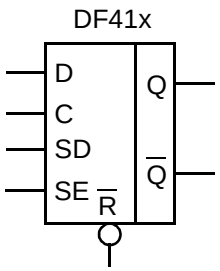
Description

DF41x is a family of static, master-slave, multiplexed scan D flip-flops. RESET is asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	Q	QN
↑	H	H	X	L	H	L
↑	L	H	X	L	L	H
↑	X	H	H	H	H	L
↑	X	H	L	H	L	H
X	X	L	X	X	L	H
L	X	H	X	X	NC	NC

NC = No Change

HDL Syntax

Verilog ..... DF41x *inst_name* (Q, QN, C, D, RN, SD, SE);

VHDL..... *inst_name*: DF41x port map (Q, QN, C, D, RN, SD, SE);

Pin Loading

Pin Name	Equivalent Loads			
	DF411	DF412	DF414	DF416
C	1.0	1.0	1.0	1.0
D	1.0	1.0	1.0	1.0
RN	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.1	2.1	2.2	2.2

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF411	12.0	TBD	25.6
DF412	13.0	TBD	28.8
DF414	17.0	TBD	34.8
DF416	19.0	TBD	47.6

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
DF411	From: C To: Q	t_{PLH} t_{PHL}	0.70 0.62	0.80 0.76	0.92 0.92	1.06 1.08	1.18 1.20
	From: C To: QN	t_{PLH} t_{PHL}	0.78 1.02	0.86 1.15	0.97 1.29	1.11 1.45	1.22 1.57
	From: RN To: Q	t_{PHL}	0.84	0.98	1.13	1.29	1.41
	From: RN To: QN	t_{PLH}	0.42	0.52	0.65	0.79	0.90
	Number of Equivalent Loads		**1**	**8**	**15**	**22**	**30 (max)**
DF412	From: C To: Q	t_{PLH} t_{PHL}	0.72 0.64	0.85 0.84	0.97 0.97	1.07 1.09	1.17 1.21
	From: C To: QN	t_{PLH} t_{PHL}	0.90 1.17	0.99 1.32	1.09 1.42	1.18 1.52	1.28 1.62
	From: RN To: Q	t_{PHL}	0.88	1.06	1.19	1.31	1.44
	From: RN To: QN	t_{PLH}	0.44	0.56	0.66	0.76	0.87
	Number of Equivalent Loads		**1**	**14**	**28**	**42**	**56 (max)**
DF414	From: C To: Q	t_{PLH} t_{PHL}	0.73 0.60	0.80 0.80	0.90 0.94	1.01 1.05	1.14 1.15
	From: C To: QN	t_{PLH} t_{PHL}	0.85 1.11	0.95 1.23	1.03 1.36	1.11 1.48	1.22 1.58
	From: RN To: Q	t_{PHL}	1.18	1.40	1.54	1.67	1.79
	From: RN To: QN	t_{PLH}	0.46	0.56	0.66	0.75	0.84

	Number of Equivalent Loads		1	21	42	62	83 (max)
DF416	From: C To: Q	t_{PLH} t_{PHL}	0.76 0.74	0.91 0.88	1.02 1.01	1.10 1.13	1.19 1.24
	From: C To: QN	t_{PLH} t_{PHL}	0.98 1.28	1.08 1.40	1.16 1.51	1.23 1.60	1.30 1.70
	From: RN To: Q	t_{PHL}	1.32	1.55	1.71	1.85	1.98
	From: RN To: QN	t_{PLH}	0.53	0.60	0.70	0.79	0.87

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell DF411	DF412	DF414	DF416
Min C Width	High	t_w	0.80	0.91	0.91	1.02
Min C Width	Low	t_w	0.85	0.85	0.90	0.90
Min RN Width	Low	t_w	0.53	0.53	0.62	0.62
Min D Setup		t_{su}	0.69	0.69	0.70	0.70
Min D Hold		t_h	0.17	0.17	0.19	0.19
Min SD Setup		t_{su}	0.69	0.69	0.70	0.70
Min SD Hold		t_h	0.17	0.17	0.19	0.19
Min SE Setup		t_{su}	0.84	0.84	0.85	0.85
Min SE Hold		t_h	0.17	0.17	0.19	0.19
Min RN Setup		t_{su}	0.37	0.37	0.43	0.43
Min RN Hold		t_h	0.33	0.33	0.35	0.35

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AMI5HG 0.5 micron CMOS Gate Array

Logic Schematic