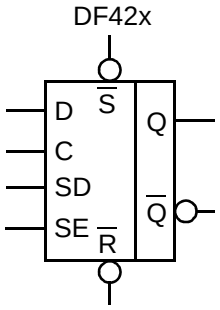
Description

DF42x is a family of static, master-slave, multiplexed scan D flip-flops. SET and RESET are asynchronous and active low. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	RN	SD	SE	SN	Q	QN
↑	H	H	X	L	H	H	L
↑	L	H	X	L	H	L	H
↑	X	H	H	H	H	H	L
↑	X	H	L	H	H	L	H
X	X	L	X	X	H	L	H
X	X	H	X	X	L	H	L
X	X	L	X	X	L	IL	IL
L	X	H	X	X	H	NC	NC

NC = No Change IL = Illegal Condition

HDL Syntax

Verilog ..... DF421x *inst_name* (Q, QN, C, D, RN, SD, SE, SN);

VHDL..... *inst_name*: DF421x port map (Q, QN, C, D, RN, SD, SE, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DF421	DF422	DF424	DF426
C	1.0	1.0	1.0	1.0
D	1.0	1.0	1.0	1.0
RN	2.1	2.1	1.1	1.1
SD	1.0	1.0	1.0	1.0
SE	2.1	2.1	2.1	2.1
SN	2.1	2.1	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF421	13.0	TBD	26.1

AMI5HG 0.5 micron CMOS Gate Array

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF422	14.0	TBD	29.4
DF424	17.0	TBD	41.4
DF426	19.0	TBD	47.7

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
DF421	From: C To: Q	t_{PLH} t_{PHL}	0.71 0.61	0.81 0.74	0.94 0.89	1.08 1.06	1.20 1.18
	From: C To: QN	t_{PLH} t_{PHL}	0.86 0.90	0.95 1.00	1.07 1.13	1.21 1.27	1.32 1.38
	From: RN To: Q	t_{PHL}	0.78	0.92	1.07	1.24	1.36
	From: RN To: QN	t_{PLH}	1.03	1.12	1.24	1.38	1.49
	From: SN To: Q	t_{PLH}	0.75	0.84	0.97	1.12	1.24
	From: SN To: QN	t_{PHL}	0.29	0.41	0.54	0.69	0.81
	Number of Equivalent Loads		**1**	**8**	**15**	**22**	**30 (max)**
DF422	From: C To: Q	t_{PLH} t_{PHL}	0.75 0.65	0.87 0.82	0.98 0.96	1.07 1.08	1.18 1.20
	From: C To: QN	t_{PLH} t_{PHL}	1.03 1.02	1.12 1.13	1.21 1.23	1.29 1.32	1.38 1.42
	From: RN To: Q	t_{PHL}	0.82	0.99	1.13	1.26	1.39
	From: RN To: QN	t_{PLH}	1.20	1.29	1.37	1.46	1.55
	From: SN To: Q	t_{PLH}	0.83	0.95	1.06	1.16	1.28
	From: SN To: QN	t_{PHL}	0.32	0.46	0.57	0.67	0.79

	Number of Equivalent Loads		1	14	28	42	56 (max)
DF424	From: C To: Q	t_{PLH} t_{PHL}	1.25 1.16	1.36 1.29	1.44 1.39	1.51 1.47	1.63 1.55
	From: C To: QN	t_{PLH} t_{PHL}	0.83 0.96	0.91 1.11	1.01 1.23	1.11 1.32	1.22 1.42
	From: RN To: Q	t_{PHL}	0.80	0.95	1.05	1.15	1.25
	From: RN To: QN	t_{PLH}	1.19	1.28	1.38	1.46	1.54
	From: SN To: Q	t_{PLH}	0.53	0.62	0.71	0.80	0.90
	From: SN To: QN	t_{PHL}	0.88	0.99	1.13	1.22	1.31
	Number of Equivalent Loads		**1**	**21**	**42**	**62**	**83 (max)**
DF426	From: C To: Q	t_{PLH} t_{PHL}	1.33 1.23	1.42 1.36	1.51 1.46	1.60 1.55	1.70 1.65
	From: C To: QN	t_{PLH} t_{PHL}	0.93 1.03	1.02 1.18	1.12 1.31	1.21 1.42	1.30 1.52
	From: RN To: Q	t_{PHL}	0.88	1.06	1.16	1.25	1.34
	From: RN To: QN	t_{PLH}	1.25	1.32	1.42	1.51	1.63
	From: SN To: Q	t_{PLH}	0.56	0.67	0.78	0.87	0.96
	From: SN To: QN	t_{PHL}	0.95	1.11	1.21	1.30	1.40

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

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Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF421	DF422	DF424	DF426
Min C Width	High	t_w	0.73	0.85	0.82	0.82
Min C Width	Low	t_w	0.96	0.96	0.97	0.97
Min RN Width	Low	t_w	0.87	1.01	0.65	0.65
Min SN Width	Low	t_w	0.59	0.64	0.46	0.46
Min D Setup		t_{su}	0.79	0.79	0.79	0.79
Min D Hold		t_h	0.17	0.17	0.18	0.18
Min SD Setup		t_{su}	0.79	0.79	0.79	0.79
Min SD Hold		t_h	0.17	0.17	0.18	0.18
Min SE Setup		t_{su}	0.95	0.95	0.95	0.95
Min SE Hold		t_h	0.17	0.17	0.18	0.18
Min RN Setup		t_{su}	0.36	0.36	0.40	0.40
Min RN Hold		t_h	0.33	0.33	0.34	0.34
Min SN Setup		t_{su}	0.24	0.24	0.23	0.23
Min SN Hold		t_h	0.50	0.50	0.51	0.51

Logic Schematic