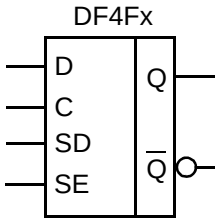
Description

DF4Fx is a family of static, master-slave, multiplexed scan D flip-flops without SET or RESET. Outputs are buffered and change state on the rising edge of the clock.

Logic Symbol



Truth Table

C	D	SD	SE	Q	QN
↑	H	X	L	H	L
↑	L	X	L	L	H
↑	X	H	H	H	L
↑	X	L	H	L	H
L	X	X	X	NC	NC

NC = No Change

HDL Syntax

Verilog ..... DF4Fx *inst_name* (Q, QN, C, D, SD, SE);

VHDL..... *inst_name*: DF4Fx port map (Q, QN, C, D, SD, SE);

Pin Loading

Pin Name	Equivalent Loads			
	DF4F1	DF4F2	DF4F4	DF4F6
C	1.0	1.0	1.0	1.0
D	1.0	1.0	1.0	1.0
SD	1.0	1.0	1.0	1.0
SE	2.1	2.1	2.1	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DF4F1	9.0	TBD	21.4
DF4F2	10.0	TBD	24.7
DF4F4	13.0	TBD	34.6
DF4F6	16.0	TBD	42.8

a. See page 2-15 for power equation.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
DF4F1	From: C To: Q	t_{PLH} t_{PHL}	0.68 0.59	0.79 0.72	0.92 0.88	1.06 1.04	1.16 1.17
	From: C To: QN	t_{PLH} t_{PHL}	0.74 0.86	0.84 0.97	0.95 1.09	1.08 1.23	1.19 1.35
	Number of Equivalent Loads		**1**	**8**	**15**	**22**	**30 (max)**
DF4F2	From: C To: Q	t_{PLH} t_{PHL}	0.71 0.62	0.84 0.82	0.95 0.95	1.05 1.07	1.16 1.18
	From: C To: QN	t_{PLH} t_{PHL}	0.87 0.96	0.97 1.09	1.06 1.20	1.15 1.29	1.25 1.40
	Number of Equivalent Loads		**1**	**14**	**28**	**42**	**56 (max)**
DF4F4	From: C To: Q	t_{PLH} t_{PHL}	1.13 1.01	1.23 1.14	1.32 1.26	1.39 1.36	1.44 1.46
	From: C To: QN	t_{PLH} t_{PHL}	0.76 0.88	0.86 1.00	0.96 1.11	1.05 1.21	1.12 1.30
	Number of Equivalent Loads		**1**	**21**	**42**	**62**	**83 (max)**
DF4F6	From: C To: Q	t_{PLH} t_{PHL}	1.16 1.06	1.26 1.16	1.34 1.24	1.40 1.34	1.46 1.44
	From: C To: QN	t_{PLH} t_{PHL}	0.80 0.96	0.91 1.10	1.02 1.20	1.11 1.28	1.19 1.39

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DF4F1	DF4F2	DF4F4	DF4F6
Min C Width	High	t_w	0.70	0.80	0.73	0.77
Min C Width	Low	t_w	0.81	0.81	0.81	0.81
Min D Setup		t_{su}	0.67	0.67	0.67	0.67
Min D Hold		t_h	0.16	0.16	0.16	0.16
Min SD Setup		t_{su}	0.67	0.67	0.67	0.67
Min SD Hold		t_h	0.16	0.16	0.16	0.16
Min SE Setup		t_{su}	0.81	0.81	0.81	0.81
Min SE Hold		t_h	0.16	0.16	0.16	0.16

Logic Schematic