Preliminary

DFBM-CS320

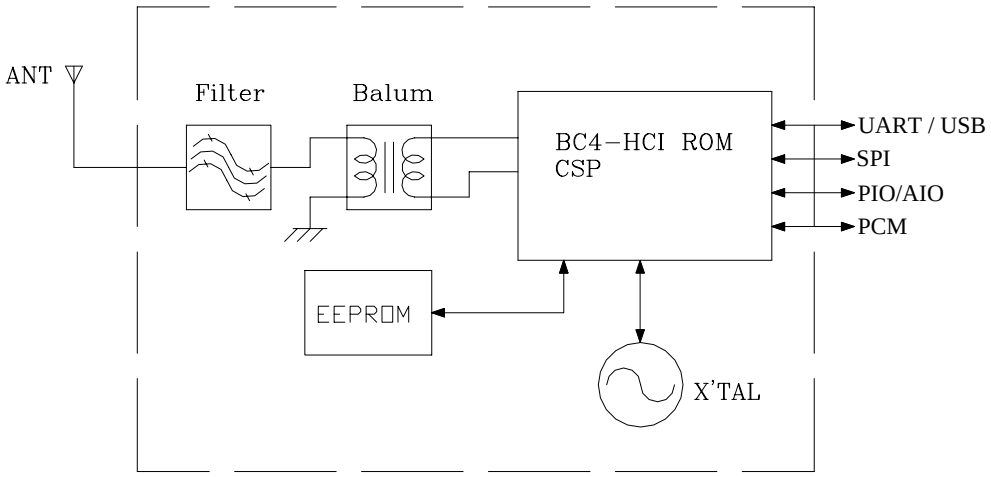
DFBM-CS320
Bluetooth™ Module Class 2

Wireless communication module compliant with Bluetooth™ Specification V2.0+EDR

FEATURES:

- ***Suitable for Cellular Phones, PDAs, Digital Cameras, ……***
- ***Small size and Low Profile using high-density packaging technology for space critical applications.***
- ***High sensitivity for better reception.***
- ***Various interfaces: UART or USB.***
- ***Wide operating temperature range: -40~+85℃.***

Device diagram



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General Specification

Bluetooth Specification	**Version 2.0+EDR**
Frequency	**2402~2480MHz**
Modulation	**GFSK/DQPSK/8DPSK**
Transmission Rate	**721K / 2M / 3M bps**
Receive Sensitivity	**Typ. -78dBm**
Maximum Output Power	**+4dBm(Class 2)**
Operating Voltage	**2.7~3.6V**
Current Consumption	**35 mA**
Operating Temperature	**-40~+85℃**
Antenna Impedance	**50Ω**
Package Size	**7.5*6.5*1.6 (mm)**

Interface

Interface	Description
Antenna	External Antenna 50Ω
UART Interface	TX, RX, RTS, CTS(9600bps~1.5Mbps)
SPI Interface	Synchronous Serial Interface for firmware download
USB Interface	Full speed Universal Serial Bus interface
PCM Interface	Supports continuous transmission and reception of PCM encoded audio data over Bluetooth
PIO Interface	8 terminals
AIO Interface	1 terminals

External Reference Clock Input

The DFBM-CS320 RF local oscillator and internal digital clocks are derived from the reference clock at DFBM-CS320 XTAL_IN input. This reference may be either an external clock or from a crystal connected between XTAL_IN and XTAL_OUT.

The external clock can either be a digital level square wave or sinusoidal and this may be directly coupled to XTAL_IN without the need for additional components. If the peaks of the reference clock are below 0 V or above 1.8 V, it must be driven through a DC blocking capacitor (~33pF) connected to XTAL_IN.

The external clock signal should meet the specifications as below table.

	Min	Typ	Max
Frequency	**7.5 MHz**	**16 MHz**	**40 MHz**
Duty cycle	**20 : 80**	**50 : 50**	**80 : 20**
Edge Jitter (At Zero Crossing)	**-**	**-**	**15ps rms**
Signal Level	**400mV pk-pk**	**-**	**1.8V ***

* If the external clock is driven through a DC blocking capacitor then maximum allowable amplitude is reduced from 1.8V to 800mV pk-pk.

Host transport selection

The firmware configures itself when it boots by reading the values on a set of PIO pins.

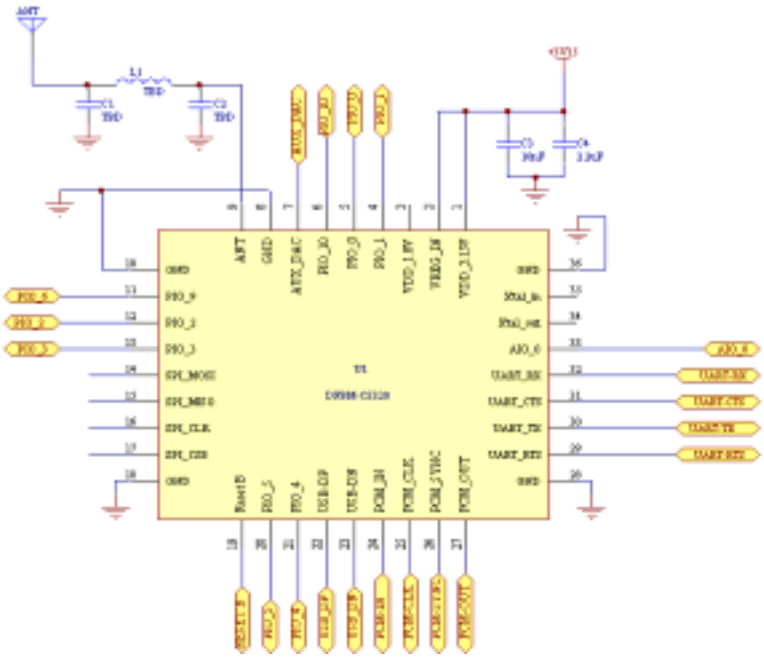
Pin Values			Host Transport	Features	
PIO[0]	**PIO[1]**	**PIO[4]**		**Auto System Clock Adaptation**	**Auto Baud Rate Adaptation**
0	0	0	BCSP (default)	Available (*1)	Available (*2)
0	0	1	BCSP with UATR configured to use 2 stop bits and no parity	Available (*1)	Available (*2)
0	1	0	USB, 16 MHz crystal	Not available	Not appropriate
0	1	1	USB, 26 MHz crystal	Not available	Not appropriate
1	0	0	Three-wire UART	Available (*1)	Available (*2)
1	0	1	H4DS	Available (*1)	Available (*2)
1	1	0	UART (H4)	Available (*1)	Available (*2)
1	1	1	Undefined	-	-

(*1) If a UART-based host transport is selected and the firmware does not know its clock frequency (because PSKEY_ANA_FREQ contains no value), then the firmware attempts to lock on to the available system clock signal. Use of this mechanism implies booting the firmware twice, as described in [AUTOBAUD]. PSKEY_ANA_FREQ has no default value.

(*2) If a UART-based host transport is selected and the baud rate defined in PSKEY_UART_BAUDRATE is zero (the default value), then the baud rate adaptation process is invoked, as described in [AUTOBAUD].

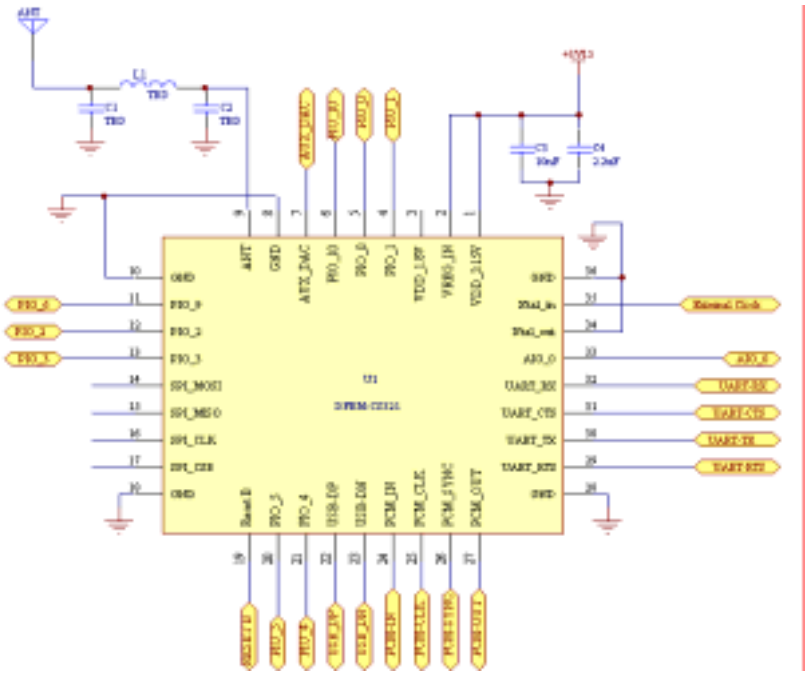
If the PS Key contains a non-zero baud rate then the UART is configured with this value. If the system clock adaptation mechanism is used, it may result in the processor running slower than normal, so the consequent (measured) baud rate will also be affected.

Application Circuit



Crystal mode circuit

External mode circuit



*****Note: The circuits are offered without warranty and Delta is unable to accept any liability for direct or consequential loss associated with their use. It is therefore important for designers to ensure that their design is properly evaluated in a Design Verification Test.

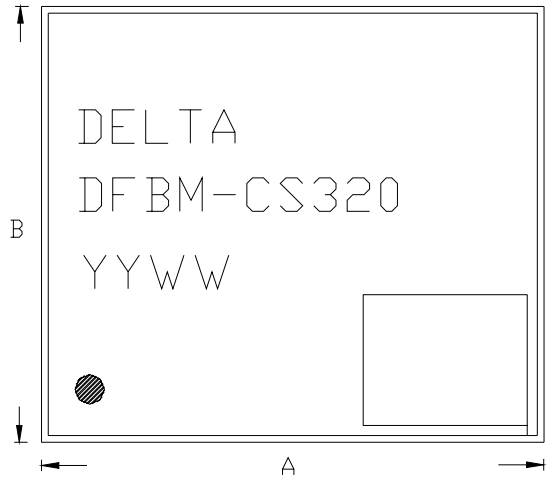
Pin description

Pin No.	Name	Description
1	Vdd_3.15V	Supply Voltage (3.15V , 2.7~3.6), INPUT
2	VREG_IN	Supply Voltage (3.15V , 2.2~3.6V), INPUT
3	Vdd_1.8V	Supply Voltage (1.8V), OUTPUT
4	PIO_1	Programmable input/output line
5	PIO_0	Programmable input/output line
6	PIO_10	Programmable input/output line
7	AUX_DAC	Voltage DAC
8	Gnd	Ground
9	ANT	RF input/output
10	Gnd	Ground
11	PIO_9	Programmable input/output line
12	PIO_2	Programmable input/output line
13	PIO_3	Programmable input/output line
14	SPI_MOSI	Serial Peripheral Interface data input
15	SPI_MISO	Serial Peripheral Interface data output
16	SPI_CLK	Serial Peripheral Interface clock
17	SPI_CSB	Chip select for Serial Peripheral Interface, active low

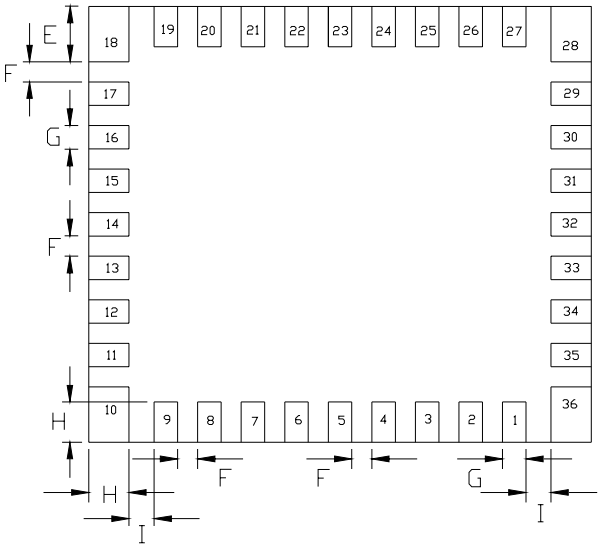
18	Gnd	Ground
19	Reset B	An active low reset
20	PIO_5	Programmable input/output line
21	PIO_4	Programmable input/output line
22	USB_DP	USB data plus with selectable internal 1.5kohm pull-up resistor
23	USB_DN	USB data minus
24	PCM_IN	Synchronous data input
25	PCM_CLK	Synchronous data clock
26	PCM_SYNC	Synchronous data sync
27	PCM_OUT	Synchronous data output
28	Gnd	Ground
29	UART_RTS	UART request to send active low
30	UART_TX	UART data output active high
31	UART_CTS	UART clear to send active low
32	UART_RX	UART data input active high
33	AIO_0	Analogue Programmable input/output
34	XTAL_OUT	Drive for crystal
35	XTAL_IN	For crystal or external clock input
36	Gnd	Ground

Dimensions (mm)

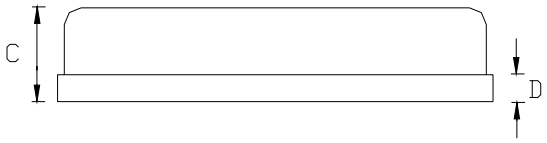
TOP VIEW



BOTTOM VIEW



SIDE VIEW



Unit : mm

A	7.5±0.2	D	0.4±0.05	G	0.35±0.05
B	6.5±0.2	E	0.825±0.05	H	0.6±0.05
C	1.6 max	F	0.30±0.05	I	0.375±0.05

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Record of changes

Date	Content of change	Maker
May 18,2005	Preliminary document release	Susan Lin

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