DFPDIV

Floating Point Pipelined Divider Unit
ver 2.15

OVERVIEW

The DFPDIV uses the **pipelined** mathematics algorithm to divide two arguments. The input numbers format is according to IEEE-754 standard. DFPDIV supports single precision real number. Divide operation was pipelined up to 15 levels. Input data are fed every clock cycle. The first result appears after 15 clock periods latency and next results are available **each clock** cycle. Full IEEE-754 precision and accuracy are included.

APPLICATION

- Math coprocessors
- DSP algorithms
- Embedded arithmetic coprocessor
- Data processing & control

KEY FEATURES

- Full IEEE-754 compliance
- Single precision real format support
- Simple interface
- No programming required
- 15 levels pipeline
- Full accuracy and precision
- Results available at every clock
- Overflow, underflow and invalid operation flags
- Fully configurable

- Fully synthesizable, static synchronous design with no internal tri-states

DELIVERABLES

- Source code:
  - ◊ VHDL Source Code or/and
  - ◊ VERILOG Source Code or/and
  - ◊ Encrypted, or plain text EDIF netlist
- VHDL & VERILOG test bench environment
  - ◊ Active-HDL automatic simulation macros
  - ◊ NCSim automatic simulation macros
  - ◊ ModelSim automatic simulation macros
  - ◊ Tests with reference responses
- Technical documentation
  - ◊ Installation notes
  - ◊ HDL core specification
  - ◊ Datasheet
- Synthesis scripts
- Example application
- Technical support
  - ◊ IP Core implementation support
  - ◊ 3 months maintenance
    - Delivery the IP Core updates, minor and major versions changes
    - Delivery the documentation updates
    - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods without royalty fees make using of IP Core easy and simply.

Single Design license allows using IP Core in single FPGA bitstream and ASIC implemen-

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tation. It also permits FPGA prototyping before ASIC production.

Unlimited Designs license allows using IP Core in unlimited number of FPGA bitstreams and ASIC implementations.

In all cases number of IP Core instantiations within a design, and number of manufactured chips are unlimited. There is no time of use limitations.

- Single Design license for
  - *VHDL, Verilog source code called HDL Source*
  - *Encrypted, or plain text EDIF called Netlist*

- Unlimited Designs license for
  - *HDL Source*
  - *Netlist*

- Upgrade from
  - *Netlist to HDL Source*
 - *Single Design to Unlimited Designs*

SYMBOL
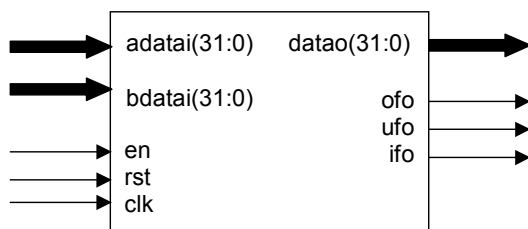
PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	Input	Global system clock
rst	Input	Global system reset
en	Input	Enable computing
adatai[31:0]	Input	A data bus input
bdatai[31:0]	Input	B data bus input
datao[31:0]	Output	Data bus output
ofo	Output	Overflow flag
ufo	Output	Underflow flag
ifo	Output	Invalid result flag

BLOCK DIAGRAM
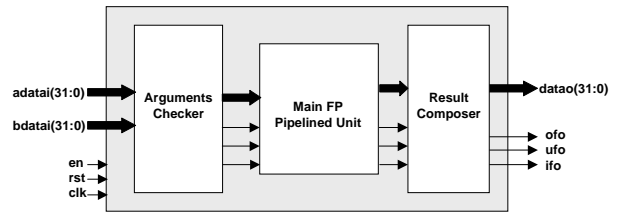
Arguments Checker - performs input data analyze against IEEE-754 number standard compliance. The appropriate numbers and information about the input data classes are given as the results to Main FP Pipelined Unit.

Main FP Pipelined Unit - performs floating point divide function. Gives the complex information about the results and makes final flags settings.

Result Composer - performs result rounding function, data alignment to IEEE-754 standard, and the final flags setting.

PERFORMANCE

The following table gives a survey about the Core area and performance in the ALTERA® devices after Place & Route :

Device	Speed grade	Logic Cells	F_{max}
FLEX10KE	-1	3100	30 MHz
ACEX1K	-1	3100	30 MHz
APEX20K	-1	2720	40 MHz
APEX20KE	-1	2720	40 MHz
APEX20KC	-7	2720	42 MHz
APEX-II	-7	2720	50 MHz
MERCURY	-5	2780	65 MHz
STRATIX	-5	2270	88 MHz
CYCLONE	-6	2270	86 MHz
STRATIX-II	-3	2040	104 MHz

Core performance in ALTERA® devices

http://www.DigitalCoreDesign.com
http://www.dcd.pl

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