64×240 dots DG06241 1/64 Duty

SANYO SEMICONDUCTOR CORP

This dot matrix module has LCD drivers with a display capacity of 64 dots by 240 dots. It receives control signals and display data from an LCD controller such as the LC7980, and displays the data on the screen. The drive type is a one-screen type for one-bit serial data.

Mechanical characteristics

Parameter	Dimensions	unit
Out line	180.0 (W)×75.0 (H)×12.0(T)	mm
Min. viewing area	132.5 (W)×39.5 (H)	mm
Dot display area	127.15(W)×33.87(H)	mm
Dot size	0.48(W)× 0.48(H)	mm
Dot pitch	0.53(W)× 0.53(H)	mm
Weight	96(approximately)	g

Absolute maximum ratings

Parameter	Symbol	min.	max.	unit
Logic supply voltage	$V_{DD}-V_{SS}$	−0.3	7.0	V
LCD supply voltage	$V_{DD}-V_O$	−0.3	20.0	V
Input voltage	V_I	−0.3	$V_{DD}+0.3$	V
Operating temperature	T_{opg}	0	+50	°C
Storage temperature	T_{stg}	−20	+70	°C

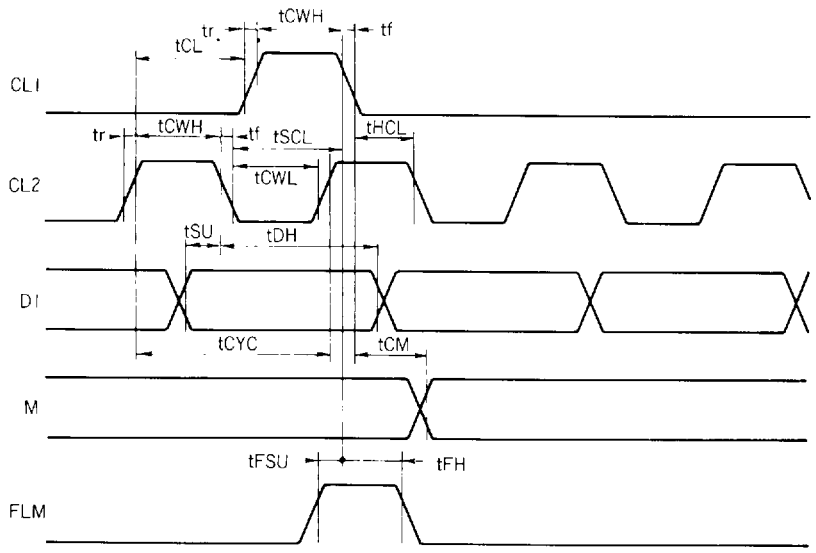
Electrical characteristics (Ta=25°C, V_{DD}=5.0±0.25V)

Parameter	Symbol	Condition	min.	typ.	max.	unit
Input high-level voltage	V_{IH}	−	0.8 V_{DD}	−	−	V
Input low-level voltage	V_{IL}	−	−	−	0.2 V_{DD}	V
LCD drive voltage	V_O	−	−	14.0	−	V
Oscillation frequency	V_{CL2}	−	−	1.0	2.5	MHz
Supply current	I_{DD}	$V_{DD}-V_O$=14.6V	−	1.5	4.0	mA
LCD supply current	I_{EE}	f_{CL2}=1.0MHz DI=GND	−	0.8	2.0	mA

Pin functions

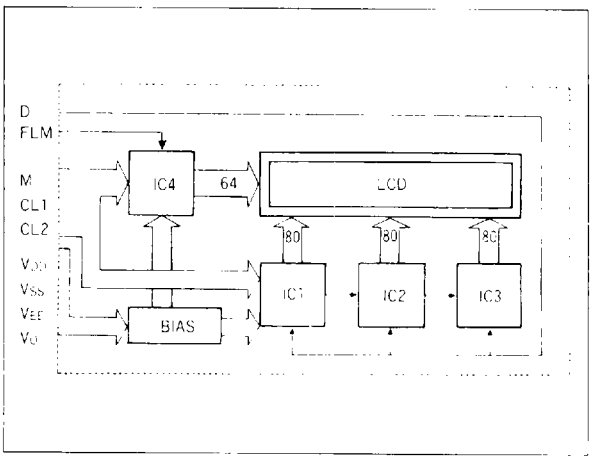
No	Symbol	Functions	No	Symbol	Functions
1	D	Display data input pin	6	NC	
2	FLM	Frame signal input pin	7	V_{DD}	Positive power pin, +5V
3	M	AC signal input pin	8	V_{SS}	Gnd pin, OV
4	CL 1	Display data latch signal input pin	9	V_{EE}	Negative power pin, −12V to −15V
5	CL 2	Display data shift clock signal input pin	10	V_O	LCD voltage control pin
			11	E 1	(High voltage side, EL input pin)
			12	E 2	(Gnd side, EL input pin)

Timing chart



Parameter	Symbol	min.	typ.	max.	unit
Clock cycle time	tCYC	400			ns
Clock pulse width (high level)	tCWH	150			ns
Clock pulse width (low level)	tCWL	150			ns
Clock setup time	tSCL	100			ns
Clock hold time	tHCL	100			ns
Clock rise time	tr			30	ns
Clock fall time	tf			30	ns
Clock phase difference	tCL	100			ns
Data setup time	tSU	80			ns
Data hold time	tDH	100			ns
FLM setup time	tFSU	100			ns
FLM hold time	tFH	100			ns
M phase difference	tCM			300	ns

Block diagram



Module dimensions

(unit : mm)

■Pattern dimensions