



Low-Voltage, Low r_{ON} , Dual DPDT Analog Switch

FEATURES

- Low Voltage Operation (2.0 V to 5.5 V)
- Low On-Resistance @ 2.7 V - r_{ON} :
 SW_1, SW_2 - 3.2 Ω
 SW_3, SW_4 - 0.64 Ω
- Fast Switching: $t_{ON} = 46$ ns
 $t_{OFF} = 21$ ns
- QFN-16 (4x4 mm) Package

BENEFITS

- Space Saving Solution
- Low Power Consumption
- Guaranteed Low Voltage Operation
- Low Voltage Logic Compatible

APPLICATIONS

- Cellular Phones
- Integrated Speaker Switching
- Audio and Video Signal Routing
- PCMCIA Cards
- Battery Operated Systems

DESCRIPTION

The DG2017 is a dual DPDT (double-pole/double-throw), optimized for high performance analog switching, and specifically designed to benefit portable audio applications.

One pair of double-throw switches is sub 1 Ω for low impedance speaker performance while the second pair of double-throw switches is suitable for microphone applications.

With the DPDT configuration, the DG2017 provides the flexibility for stereo-single-end or differential BTL output structures with a fully integrated differential microphone switching solution.

The DG2017 is an integrated monolithic device in a QFN-16 (4 x 4 mm) package that provides a space saving solution over

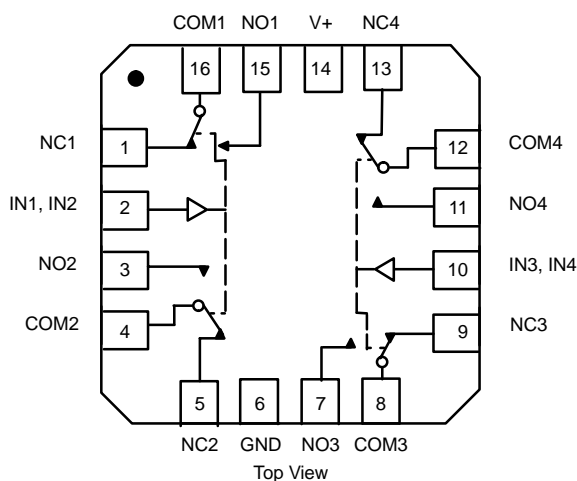
the use of multiple single SPDT devices as well as providing the advantage of on-resistance flatness and matching that single SPDT devices cannot offer.

The DG2017 provides low charge injection (2 pC), fast switching time (t_{ON} and t_{OFF} less than 100 ns), excellent Off-Isolation and Crosstalk (-70 dB @ 100 kHz). During operation, continuous current through any or all switches is rated at ± 200 mA, ideal for portable audio applications.

Built on Vishay Siliconix's low voltage CMOS process, the DG2017 contains an epitaxial layer that prevents latchup. Break-before-make is guaranteed. When on, each switch conducts equally well in both directions, and block up to the power supply level when off.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

QFN-16 (4 X 4)



TRUTH TABLE

Logic	NC1, 2, 3 and 4	NO1, 2, 3 and 4
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION

Temp Range	Package	Part Number
-40 to 85°C	16-Pin QFN (4 x 4 mm)	DG2017DN



ABSOLUTE MAXIMUM RATINGS

Reference to GND

V+	-0.3 to +6 V
IN, COM, NC, NO ^a	-0.3 to (V+ + 0.3 V)
Current (Any terminal except NO, NC or COM)	30 mA
Continuous Current (NO, NC, or COM)	±200 mA
Peak Current (Pulsed at 1 ms, 10% duty cycle)	±300 mA
Storage Temperature (D Suffix)	-65 to 150°C
Package Solder Reflow Conditions ^d	
16-Pin QFN (4 x 4 mm)	240°C

Power Dissipation (Packages)^b

QFN-16 (4x4 mm)	1880 mW
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- Notes:
- Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
 - All leads welded or soldered to PC Board.
 - Derate 23.5 mW/°C above 70°C
 - Manual soldering with iron is not recommended for leadless components. The QFN is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

SPECIFICATIONS (V+ = 3 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ±10%, V _{IN} = 0.4 or 1.6 V ^e	Temp ^a	Limits -40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	V _{NO} , V _{NC} , V _{COM}		Full	0		V+	V
DC Characteristics							
On-Resistance	r _{ON} (SW ₁ , SW ₂)	V+ = 2.7 V, V _{COM} = 0.2 V/1.5 V, I _{NO} , I _{NC} = 10 mA	Room Full		3.2	3.7 4.3	Ω
	r _{ON} (SW ₃ , SW ₄)	V+ = 2.7 V, V _{COM} = 0.2 V/1.5 V, I _{NO} , I _{NC} = 100 mA	Room Full		0.67	1.1 1.2	
r _{ON} Flatness ^d	r _{ON} (SW ₁ , SW ₂)	V+ = 2.7 V, V _{COM} = 0.2 V/1.5 V, I _{NO} , I _{NC} = 10 mA	Room Full		1.4	2.0	
	r _{ON} (SW ₃ , SW ₄)	V+ = 2.7 V, V _{COM} = 0.2 V/1.5 V, I _{NO} , I _{NC} = 100 mA	Room Full		0.12	0.3	
r _{ON} Match ^d	Δr _{ON} (SW ₁ , SW ₂)	V+ = 2.7 V, V _{COM} = 0.2 V/1.5 V, I _{NO} , I _{NC} = 10 mA	Room Full			0.3	
	Δr _{ON} (SW ₃ , SW ₄)	V+ = 2.7 V, V _{COM} = 0.2 V/1.5 V, I _{NO} , I _{NC} = 100 mA	Room Full			0.3	
Switch Off Leakage Current	I _{NO(off)} , I _{NC(off)}	V+ = 3.3 V, V _{NO} , V _{NC} = 0.3 V/3.0 V V _{COM} = 0.3 V/3.0 V	Room Full	-0.5 5.0		0.5 5.0	nA
	I _{COM(off)}		Room Full	-0.5 5.0		0.5 5.0	
Channel-On Leakage Current	I _{COM(on)}	V+ = 3.3 V, V _{NO} =V _{NC} V _{COM} = 0.3 V/3.0 V	Room Full	-0.5 5.0		0.5 5.0	
Digital Control							
Input High Voltage	V _{INH}		Full	1.6			V
Input Low Voltage	V _{INL}		Full			0.4	
Input Capacitance	C _{in}		Full		6		pF
Input Current	I _{INL} or I _{INH}	V _{IN} = 0 or V+	Full	-1		1	μA

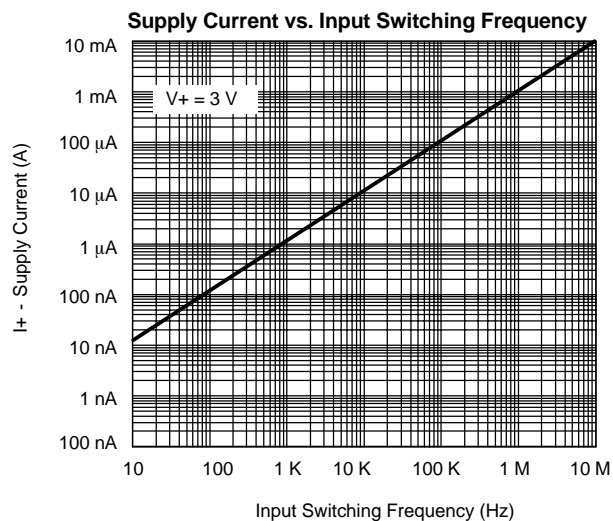
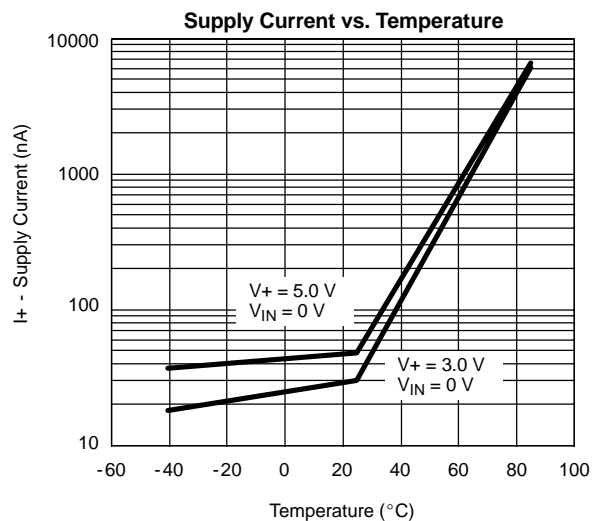
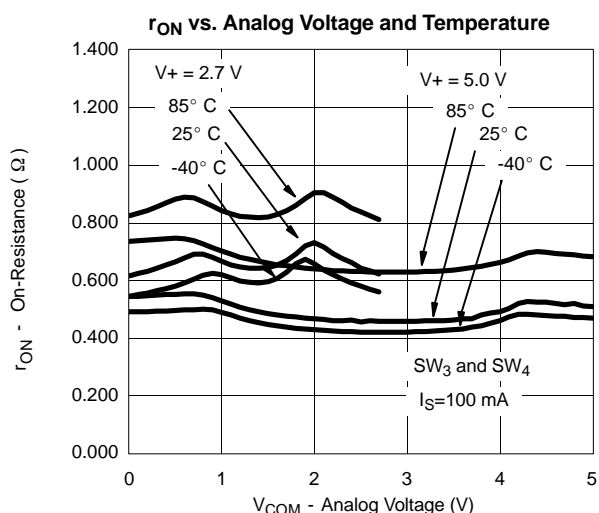
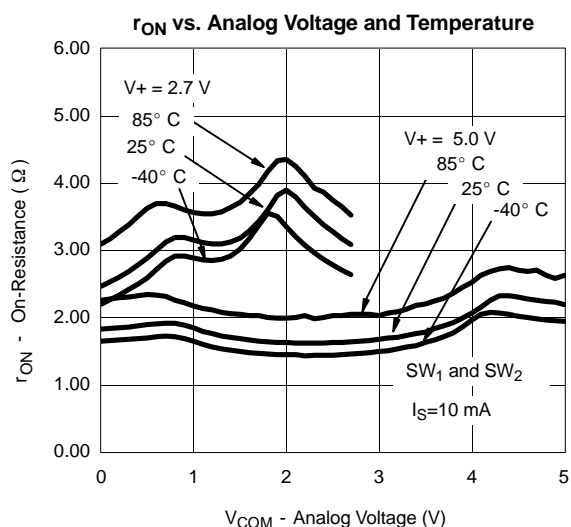
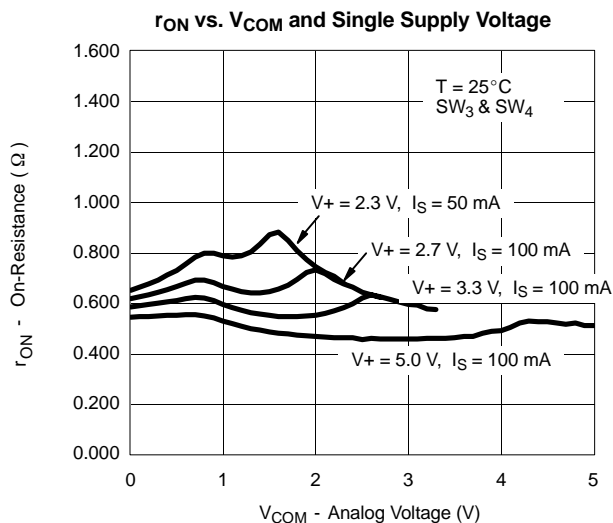
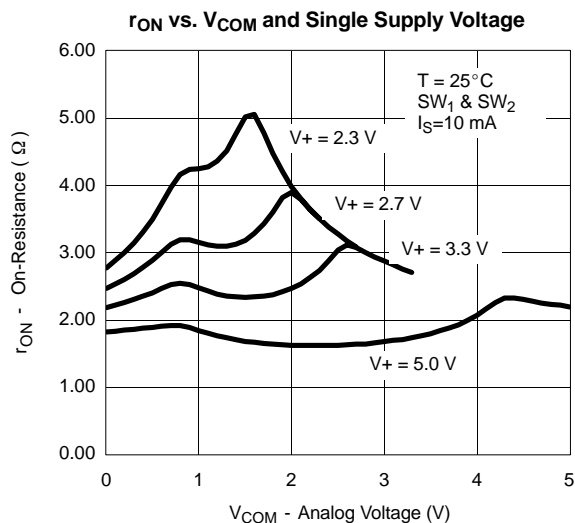


SPECIFICATIONS (V+ = 3 V)										
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ±10%, VIN = 0.4 or 1.6 V ^e	Temp ^a	Limits -40 to 85°C			Unit			
				Min ^b	Typ ^c	Max ^b				
Dynamic Characteristics										
Turn-On Time	t _{ON} , (SW ₁ , SW ₂)	V _{NO} or V _{NC} = 2.0 V, R _L = 300 Ω, C _L = 35 pF (Figure 1,2)	Room Full		62	85 91	ns			
	t _{ON} , (SW ₃ , SW ₄)		Room Full		46	74 79				
Turn-Off Time	t _{ON} , (SW ₁ , SW ₂)		Room Full		12	35 36				
	t _{ON} , (SW ₃ , SW ₄)		Room Full		21	46 48				
Break-Before-Make Time	t _d , (SW ₁ , SW ₂)		Full	5	45					
	t _d , (SW ₃ , SW ₄)		Full	5	26					
Charge Injection ^d	Q _{INJ} , (SW ₁ , SW ₂)		C _L = 1 nF, V _{GEN} = 0 V, R _{GEN} = 0 Ω (Figure 3)	Room		2			pC	
	Q _{INJ} , (SW ₃ , SW ₄)					1				
Off-Isolation ^d	OIRR, (SW ₁ , SW ₂)		R _L = 50 Ω, C _L = 5 pF, f = 1 MHz (Figure 4)	Room		-68			dB	
	OIRR, (SW ₃ , SW ₄)					-51				
Crosstalk ^d	X _{TALK} , (SW ₁ , SW ₂)					-69				
	X _{TALK} , (SW ₃ , SW ₄)					-51				
N _O , N _C Off Capacitance ^d	C _{OFF} , (SW ₁ , SW ₂)	V _{IN} = 0 or V+, f = 1 MHz	Room		12		pF			
	C _{OFF} , (SW ₃ , SW ₄)				43					
Channel-On Capacitance ^d	C _{ON} , (SW ₁ , SW ₂)					86				
	C _{ON} , (SW ₃ , SW ₄)					283				
Power Supply										
Power Supply Range	V+				2.0				5.5	V
Power Supply Current	I+	V _{OE} = 0 or V+				1.0	μA			

Notes:

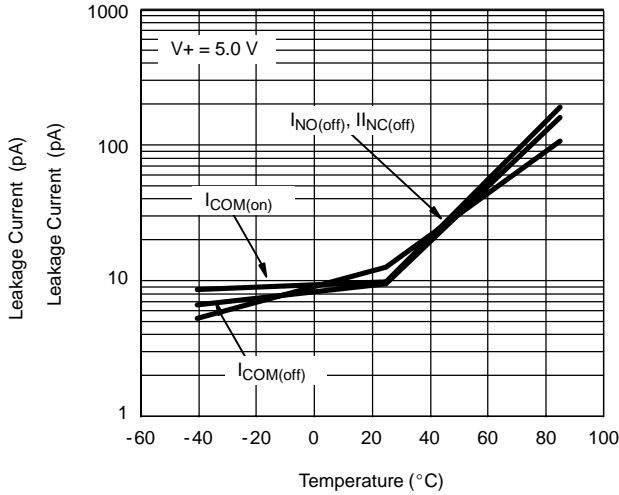
- a. Room = 25°C, Full = as determined by the operating suffix.
- b. Typical values are for design aid only, not guaranteed nor subject to production testing.
- c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- d. Guarantee by design, nor subjected to production test.
- e. V_{IN} = input voltage to perform proper function.
- f. Guaranteed by 5-V leakage testing, not production tested.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

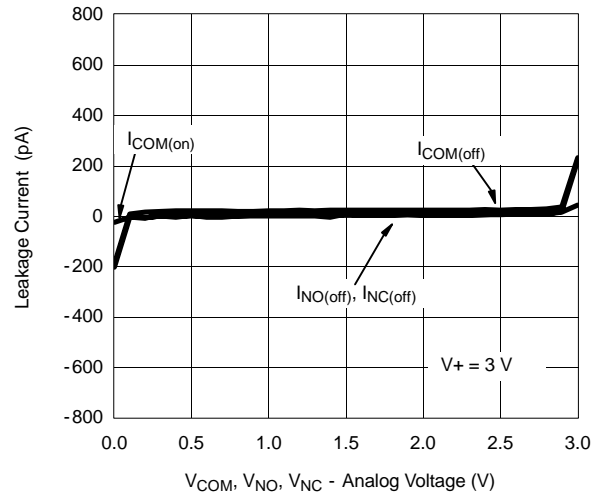


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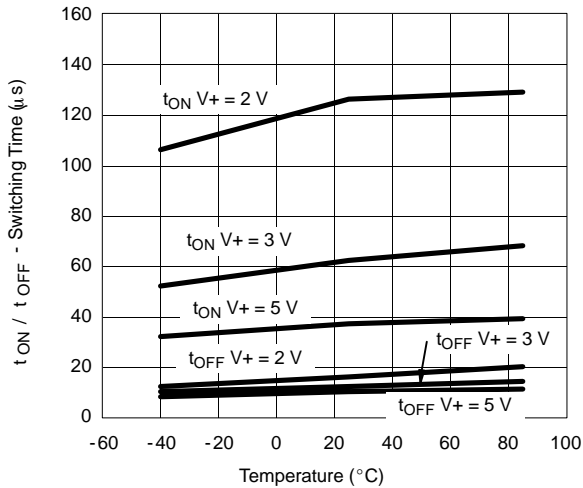
Leakage Current vs. Temperature



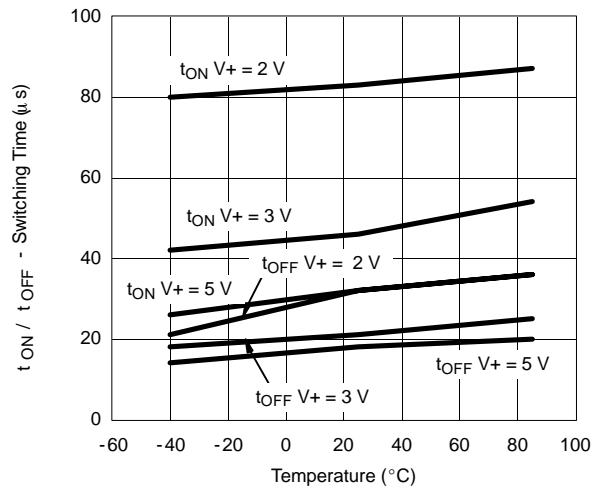
Leakage vs. Analog Voltage



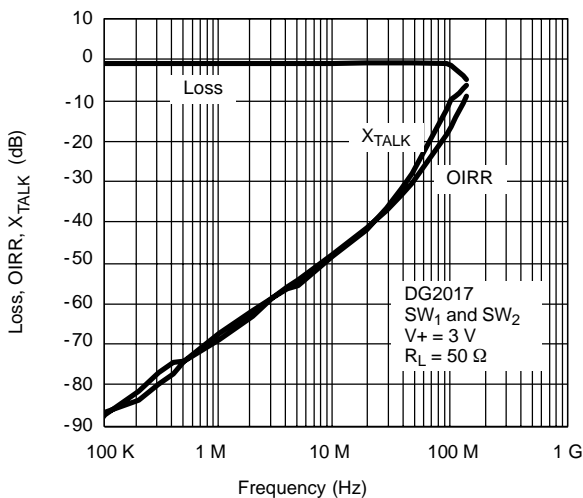
Switching Time vs. Temperature



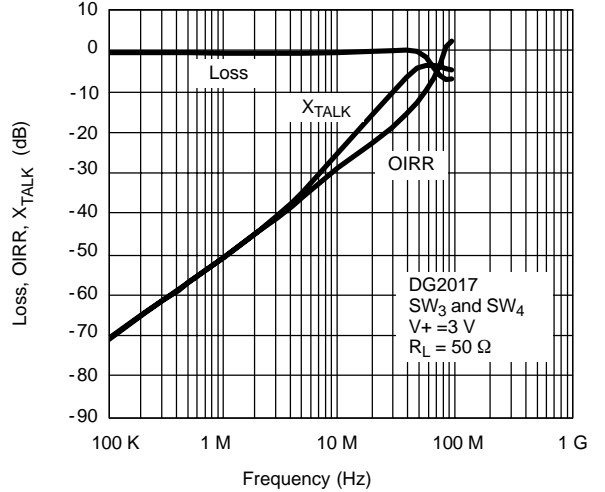
Switching Time vs. Temperature



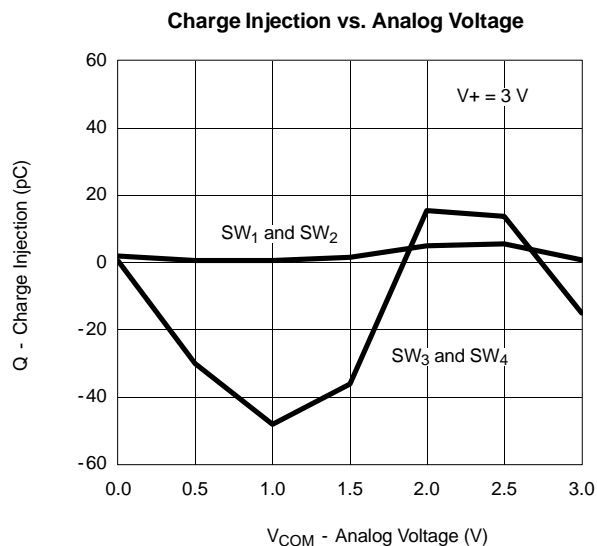
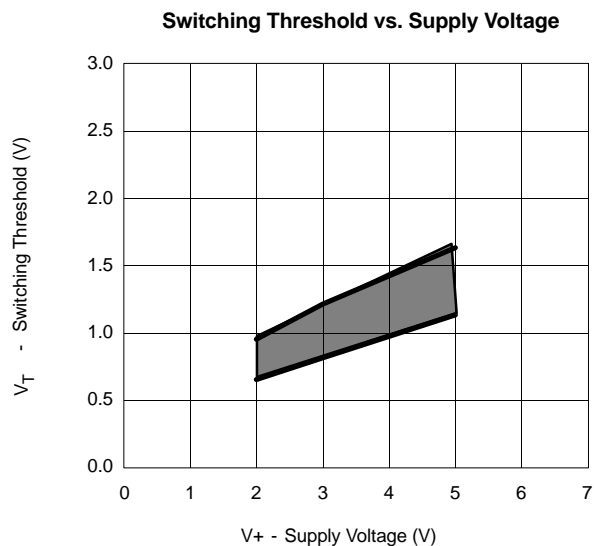
Insertion Loss, Off-Isolation Crosstalk vs. Frequency



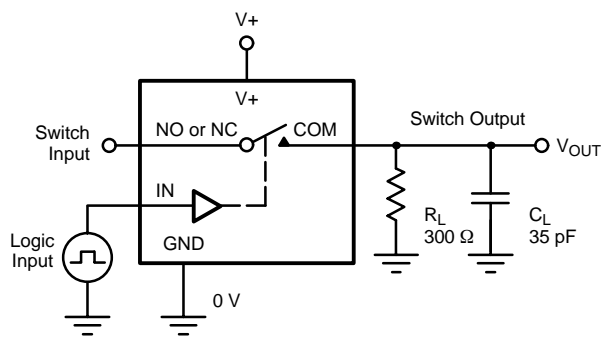
Insertion Loss, Off-Isolation Crosstalk vs. Frequency



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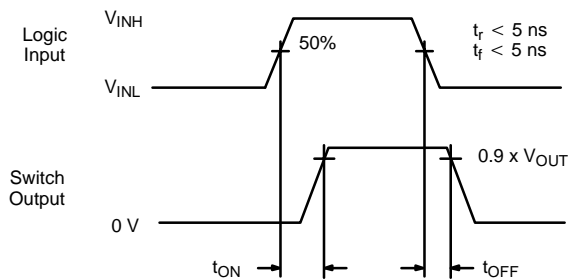


TEST CIRCUITS



C_L (includes fixture and stray capacitance)

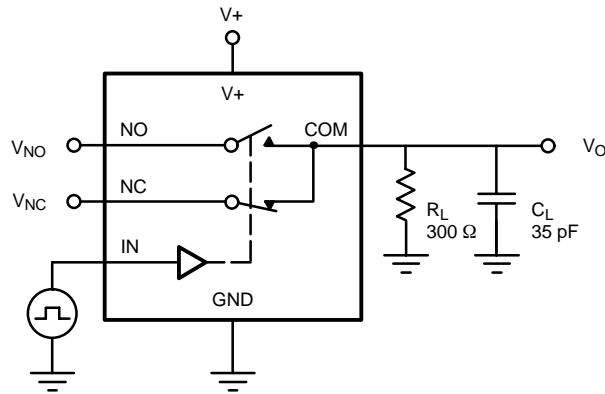
$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On
 Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time

TEST CIRCUITS



C_L (includes fixture and stray capacitance)

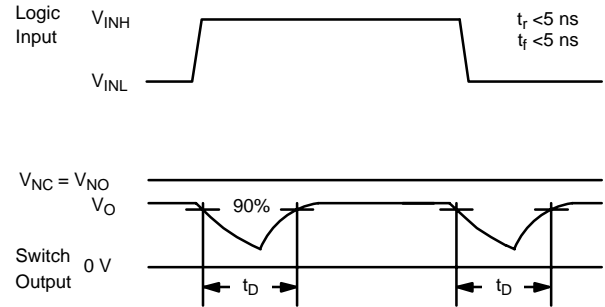
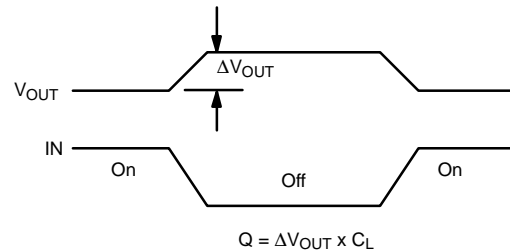
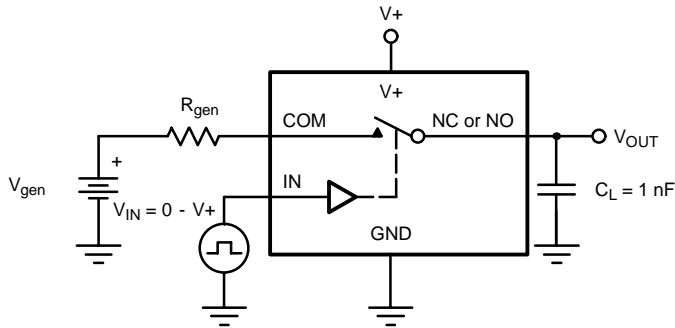
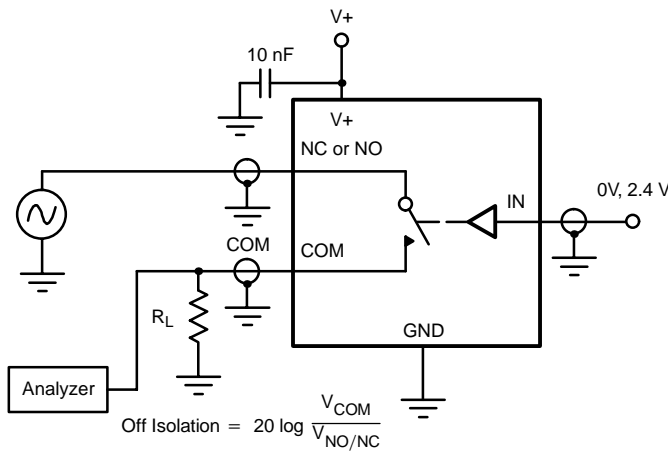


Figure 2. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection



$$\text{Off Isolation} = 20 \log \frac{V_{COM}}{V_{NO/NC}}$$

Figure 4. Off-Isolation

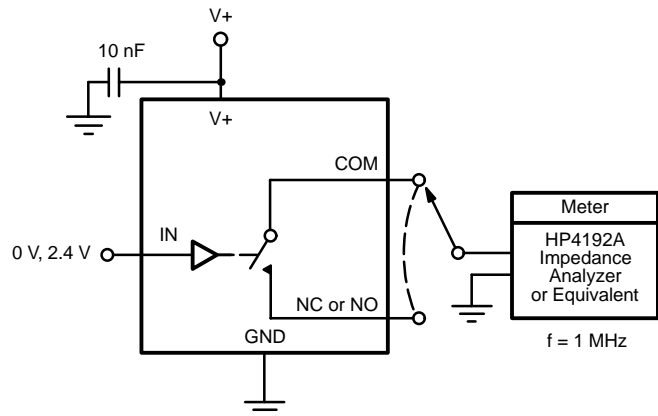


Figure 5. Channel Off/On Capacitance