



High-Speed, Low r_{ON} , SPST Analog Switch (1-Bit Bus Switch with Level-Shifter)

FEATURES

- SC-70 5-Lead Package
- 5- Ω Switch Connection Between Two Ports
- Minimal Propagation Delay Through The Switch
- Low I_{CC}
- Zero Bounce In Flow-Through Mode
- Control Inputs Compatible with TTL Level

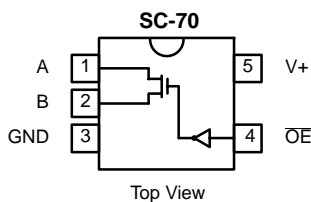
DESCRIPTION

The DG2302 is a high-speed, 1-bit, low power, TTL-compatible bus switch. Using sub-micron CMOS technology, DG2302 achieves low on-resistance and negligible propagation delay.

The DG2302 consist of a bi-directional input/output pins A and

B. When the output enable (\overline{OE}) is low, the input/output pins are connected. When the \overline{OE} is high, the switch is open and a high-impedance state exists between input/output pins A and B.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Device Marking: E5

TRUTH TABLE		
\overline{OE}	B	Function
L	A	Connect
H	HiZ State	Disconnect

ORDERING INFORMATION		
Temp Range	Package	Part Number
-40 to 85°C	SC70-5	DG2302DL



ABSOLUTE MAXIMUM RATINGS

Reference to GND

V+	-0.3 to +6 V
OE, A, B ^a	-0.3 to (V+ + 0.3 V)
Continuous Current (Any terminal)	±50 mA
Peak Current (Pulsed at 1 ms, 10% duty cycle)	±200 mA
Storage Temperature (D Suffix)	-65 to 150°C

Power Dissipation (Packages)^b

5-Pin SC70 ^c	250 mW
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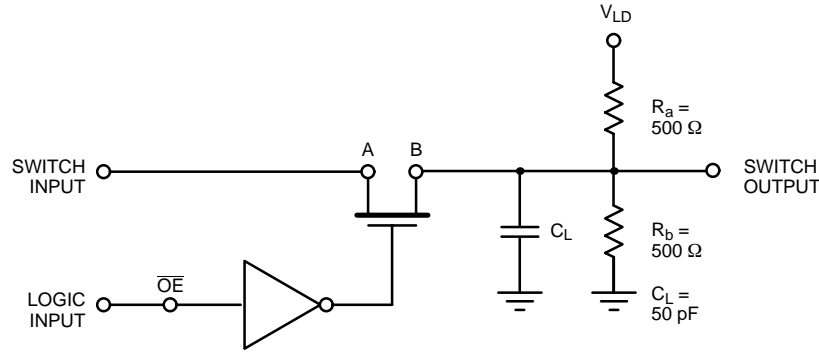
- Notes:
- Signals on A, or B or OE exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
 - All leads welded or soldered to PC Board.
 - Derate 3.1 mW/°C above 70°C

SPECIFICATIONS (V+ = 5.0 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 5 V, ±10%, VIN = 0.8 or 2.0 V ^e	Temp ^a	Limits -40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
DC Characteristics							
On-Resistance	r _{ON}	V+ = 4.5 V, V _A = 0 V, I _B = 64 mA	Full			7	Ω
		V+ = 4.5 V, V _A = 0 V, I _B = 30 mA	Full			7	
		V+ = 4.5 V, V _A = 2.4 V, I _B = 15 mA	Full			50	
Switch Off Leakage Current	I _(off)	V+ = 5.5 V, V _A = 1 V/4.5 V, V _B = 4.5 V/1 V	Full	-10		10	μA
Switch-On Leakage Current	I _(on)	V+ = 5.5 V, V _A = V _B = 1 V/4.5 V	Full	-10		10	
Input High Voltage	V _{IH}		Full	2.0			V
Input Low Voltage	V _{IL}		Full			0.8	
Input Current	I _{IL} or I _{IH}	V _{OE} = 0 or V+	Full	-1		1	μA
Dynamic Characteristics							
Prop Delay Bus-to-Bus ^f	t _{PHL}	V _{LD} = Open (Figure 1 and 2)	Full			1	ns
	t _{PLH}		Full			1	
Output Enable Time ^d	t _{PZL}	V _{LD} = 7 V, V+ = 4.5 V to 5.5 V (Figure 1 and 2)	Full		5.0		
	t _{PZH}	V _{LD} = Open, V+ = 4.5 V to 5.5 V (Figure 1 and 2)	Full		5.0		
Output Disable Time ^d	t _{PLZ}	V _{LD} = 7 V, V+ = 4.5 V to 5.5 V (Figure 1 and 2)	Full		3.9		
	t _{PHZ}	V _{LD} = Open, V+ = 4.5 V to 5.5 V (Figure 1 and 2)	Full		1.0		
Input Capacitance	C _{in}		Room		3.5		pF
Channel-Off Capacitance ^d	C _(off)	V _{OE} = 0 or V+, f = 1 MHz	Room		5		
Channel-On Capacitance ^d	C _{ON}		Room		11		
Power Supply							
Power Supply Range	V+			4.0		5.5	V
Power Supply Current	I+	V _{OE} = 0			0.9	1.5	mA
		V _{OE} = V+				1.0	μA

Notes:

- Room = 25°C, Full = as determined by the operating suffix.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Typical values are for design aid only, not guaranteed nor subject to production testing.
- Guarantee by design, nor subjected to production test.
- V_{IN} = input voltage to perform proper function.
- Guaranteed by design and not production tested. The bus switch propagation delay is a function of the RC time constant contributed by the on-resistance and the specified load capacitance with an ideal voltage source (zero output impedance) driving the switch.

AC LOADING AND WAVEFORMS



Input driven by 50-Ω source terminated in 50 Ω
 CL includes load and stray capacitance
 Input PRR = 1.0 MHz, $t_w = 50$ ns

Figure 1. AC Test Circuit

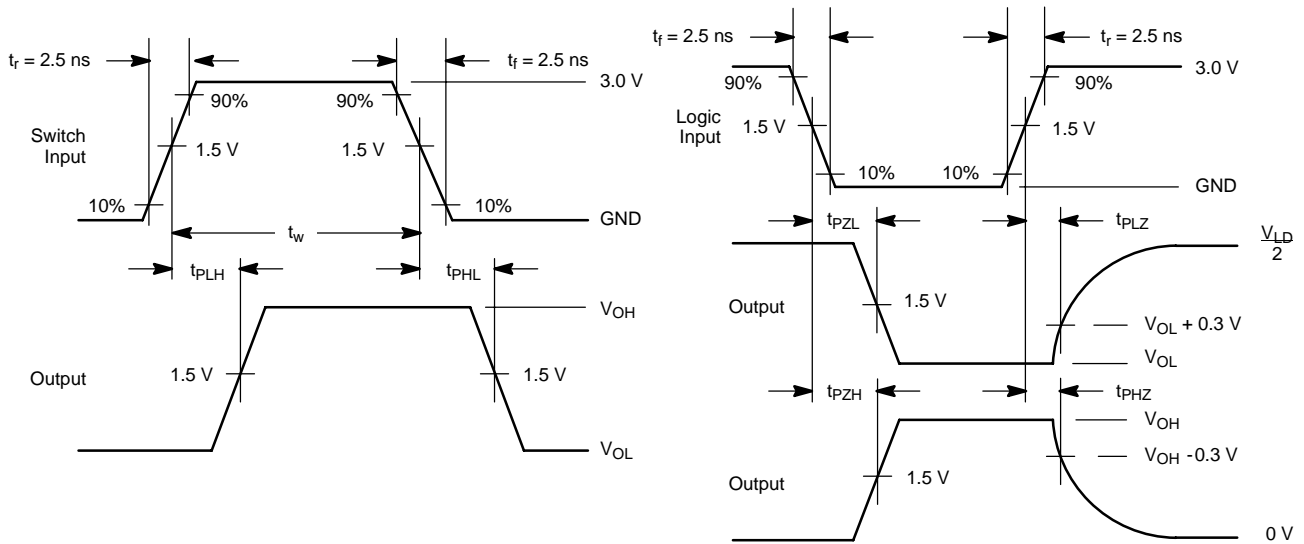


Figure 2. AC Waveforms



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

