



0.4-Ω Low-Voltage Dual SPDT Analog Switch

FEATURES

- Low Voltage Operation (1.8 V to 5.5 V)
- Low On-Resistance - r_{ON} : 0.4 Ω @ 2.7 V
- -69 dB OIRR @ 2.7 V, 100 kHz
- MSOP-10 Package
- ESD Protection >2000 V

BENEFITS

- Reduced Power Consumption
- High Accuracy
- Reduce Board Space
- 1.6-V Logic Compatible
- High Bandwidth

APPLICATIONS

- Cellular Phones
- Speaker Headset Switching
- Audio and Video Signal Routing
- PCMCIA Cards
- Battery Operated Systems
- Relay Replacement

DESCRIPTION

The DG2531/DG2532 is a sub 1-Ω (0.4 Ω @ 2.7 V) dual SPDT analog switches designed for low voltage applications.

The DG2531/DG2532 has on-resistance matching (less than 0.05 Ω @ 2.7 V) and flatness (less than 0.2 Ω @ 2.7 V) that are guaranteed over the entire voltage range. Additionally, low logic thresholds makes the DG2531/DG2532 an ideal interface to low voltage DSP control signals.

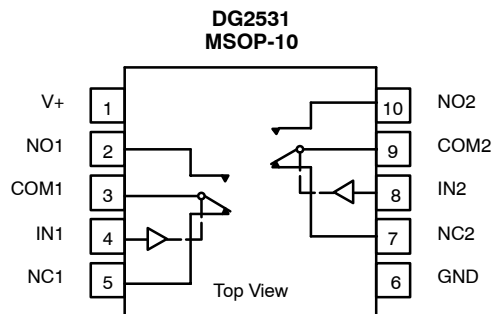
The DG2531/DG2532 has fast switching speed (on/off time @ 40 and 35 ns) with break-before-make guaranteed. In the On

condition, all switching elements conduct equally in both directions. Off-isolation and crosstalk is -69 dB @ 100 kHz.

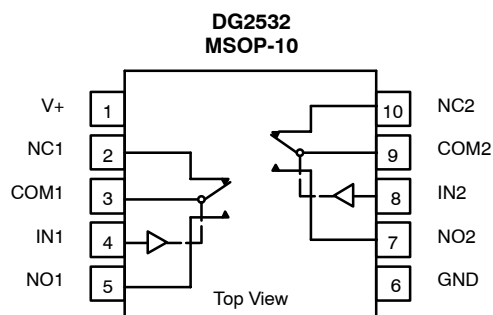
The DG2531/DG2532 is built on Vishay Siliconix's high-density low voltage CMOS process. An epitaxial layer is built in to prevent latchup. The DG2531/DG2532 contains the additional benefit of 2,000 V ESD protection.

Packaged in space saving MSOP-10, the DG2531/DG2532 is a high performance, low r_{ON} switches for battery powered applications.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



| TRUTH TABLE | | |
|-------------|-------------|-------------|
| Logic | NC1 and NC2 | NO1 and NO2 |
| 0 | ON | OFF |
| 1 | OFF | ON |



| ORDERING INFORMATION | | |
|----------------------|---------|----------------------|
| Temp Range | Package | Part Number |
| -40 to 85°C | MSOP-10 | DG2531DQ DG2532DQ |

ABSOLUTE MAXIMUM RATINGS

Reference to GND

V+ -0.3 to +6 V

IN, COM, NC, NO^a -0.3 to (V+ + 0.3 V)

Continuous Current (NO, NC, COM) ± 300 mA

Peak Current ± 500 mA
(Pulsed at 1 ms, 10% duty cycle)

Storage Temperature (D Suffix) -65 to 150°C

ESD per Method 3015.7 >2 kV

Power Dissipation (Packages)^b

MSOP-10^c 320 mW

- Notes:
- Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
 - All leads welded or soldered to PC Board.
 - Derate 4.0 mW/°C above 70°C

Permanent damage to the device may occur when the "Absolute Maximum Ratings" are exceeded. These stress ratings do not indicate conditions for which the device is intended to be functional. Functionality is only guaranteed to the conditions specified by the parametric table within the document .

| SPECIFICATIONS (V+ = 3 V) | | | | | | | | | |
|--|---|--|-------------------|-----------------------|------------------|------------------|------|-----|---|
| Parameter | Symbol | Test Conditions Otherwise Unless Specified V+ = 3 V, ±10%, V _{IN} = 0.5 or 1.4 V ^e | Temp ^a | Limits -40 to 85°C | | | Unit | | |
| | | | | Min ^b | Typ ^c | Max ^b | | | |
| Analog Switch | | | | | | | | | |
| Analog Signal Range ^d | V _{NO} , V _{NC} , V _{COM} | | Full | 0 | | V+ | V | | |
| On-Resistance | r _{ON} | V+ = 2.7 V, V _{COM} = 0.6/1.5 V I _{NO} , I _{NC} = 100 mA | Room Full | | 0.4 | 0.6 0.7 | Ω | | |
| r _{ON} Flatness ^d | r _{ON} Flatness | | Room | | 0.12 | 0.2 | | | |
| On-Resistance Match Between Channels ^d | Δr _{DS(on)} | | Room | | | 0.05 | | | |
| Switch Off Leakage Current | I _{NO(off)} , I _{NC(off)} | V+ = 3.3 V, V _{NO} , V _{NC} = 0.3 V/3 V V _{COM} = 3 V/0.3 V | Room Full | -1 -10 | | 1 10 | nA | | |
| | I _{COM(off)} | | Room Full | -1 -10 | | 1 10 | | | |
| Channel-On Leakage Current | I _{COM(on)} | V+ = 3.3 V, V _{NO} , V _{NC} = V _{COM} = 0.3 V/3 V | Room Full | -1 -10 | | 1 10 | | | |
| Digital Control | | | | | | | | | |
| Input High Voltage ^d | V _{INH} | | Full | 1.4 | | | V | | |
| Input Low Voltage | V _{INL} | | Full | | | 0.5 | | | |
| Input Capacitance | C _{in} | | Full | | 7 | | pF | | |
| Input Current | I _{INL} or I _{INH} | V _{IN} = 0 or V+ | Full | 1 | | 1 | μA | | |
| Dynamic Characteristics | | | | | | | | | |
| Turn-On Time | t _{ON} | V _{NO} or V _{NC} = 2.0 V, R _L = 50 Ω, C _L = 35 pF | Room Full | | 40 | 70 77 | ns | | |
| Turn-Off Time | t _{OFF} | | Room Full | | 35 | 65 72 | | | |
| Break-Before-Make Time | t _d | V _{NO} or V _{NC} = 2.0 V, R _L = 50 Ω, C _L = 35 pF | Full | 1 | 4 | | | | |
| Charge Injection ^d | Q _{INJ} | C _L = 1 nF, V _{GEN} = 1.5 V, R _{GEN} = 0 Ω | Room | | 54 | | pC | | |
| Off-Isolation ^d | OIRR | R _L = 50 Ω, C _L = 5 pF, f = 100 KHz | Room | | -69 | | dB | | |
| Crosstalk ^d | X _{TALK} | | Room | | -69 | | | | |
| N _O , N _C Off Capacitance ^d | C _{NO(off)} | V _{IN} = 0 or V+, f = 1 MHz | Room | | 143 | | pF | | |
| | C _{NC(off)} | | Room | | 143 | | | | |
| Channel-On Capacitance ^d | C _{NO(on)} | | Room | | 403 | | | | |
| | C _{NC(on)} | | Room | | 403 | | | | |
| Power Supply | | | | | | | | | |
| Power Supply Range | V+ | | | | 1.8 | | | 5.5 | V |
| Power Supply Current | I+ | V _{IN} = 0 or V+ | Full | | | 1.0 | μA | | |

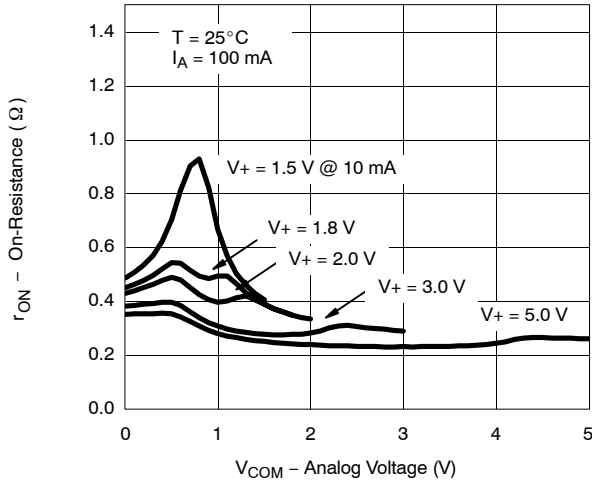
Notes:

- Room = 25°C, Full = as determined by the operating suffix.
- Typical values are for design aid only, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guarantee by design, nor subjected to production test.
- V_{IN} = input voltage to perform proper function.

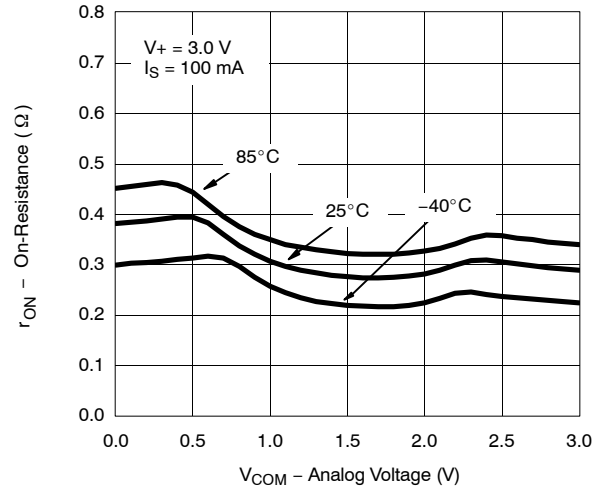


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

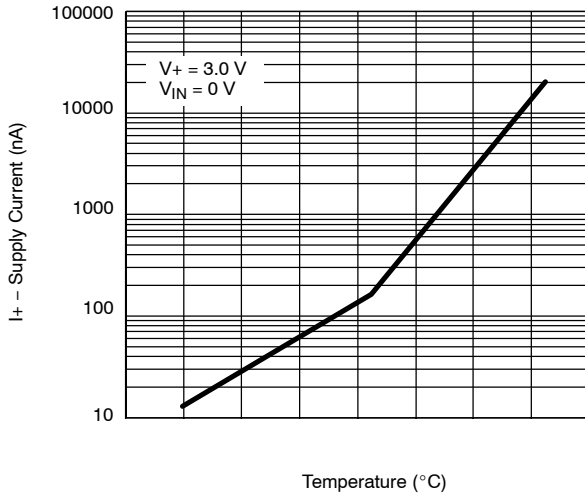
r_{ON} vs. V_{COM} and Supply Voltage



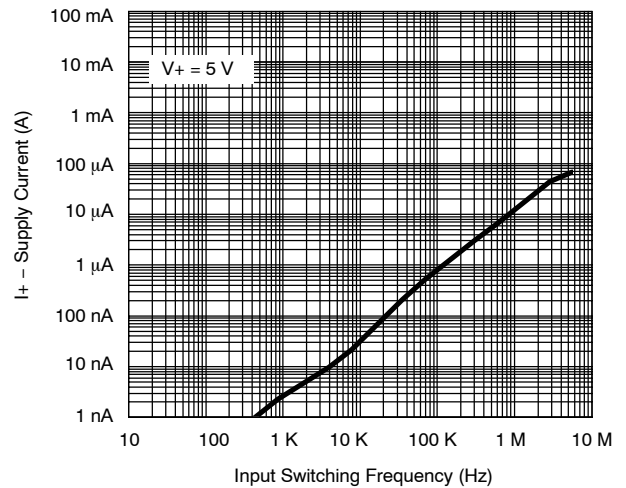
r_{ON} vs. Analog Voltage and Temperature (NC1)



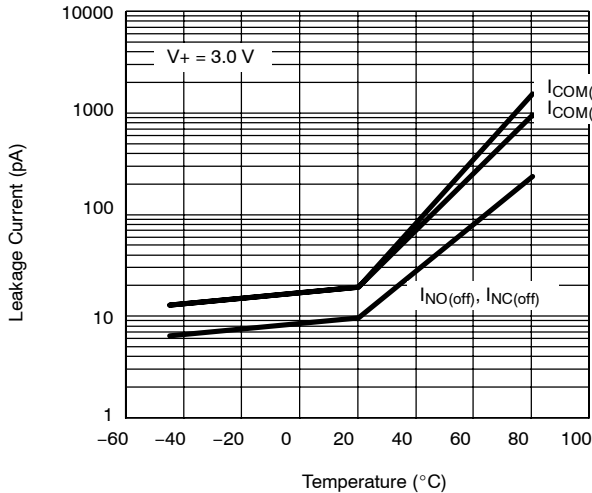
Supply Current vs. Temperature



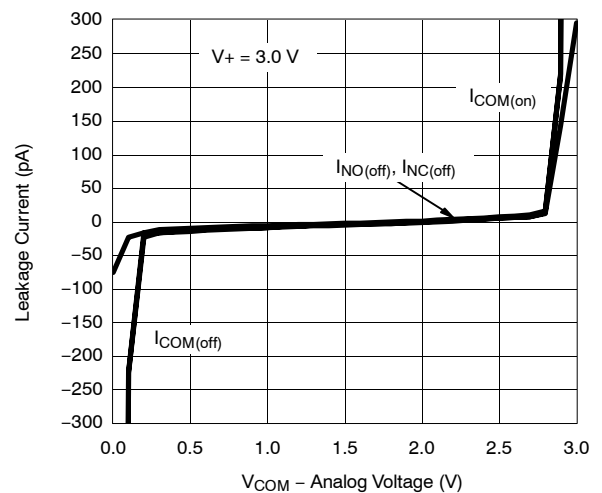
Supply Current vs. Input Switching Frequency



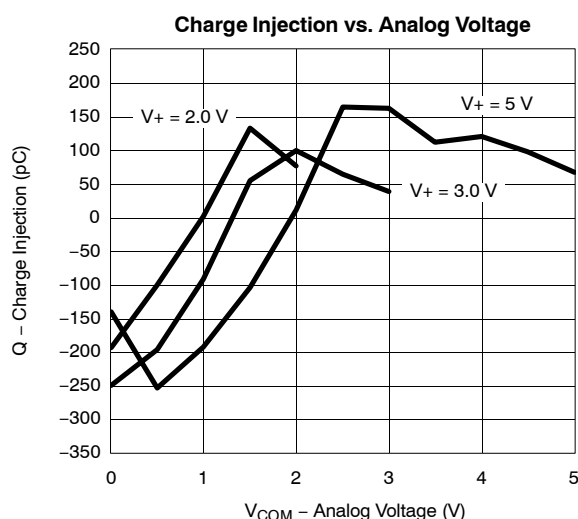
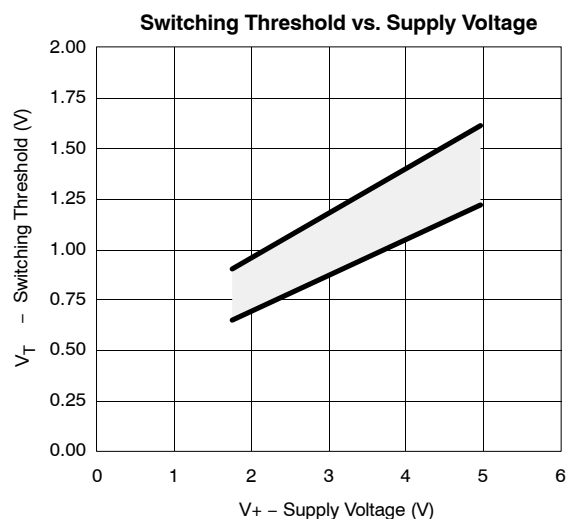
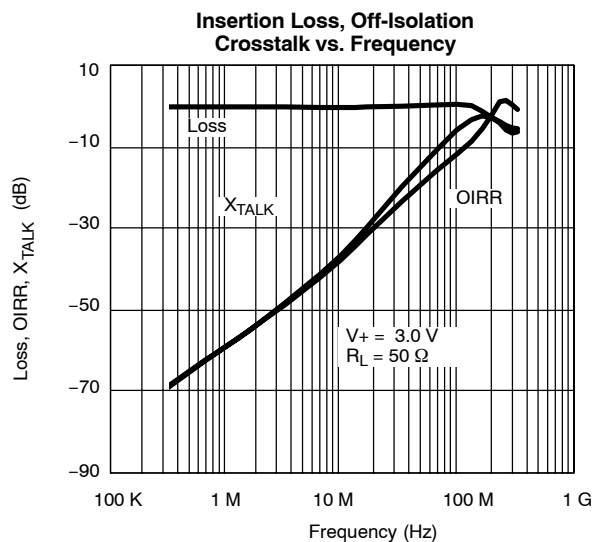
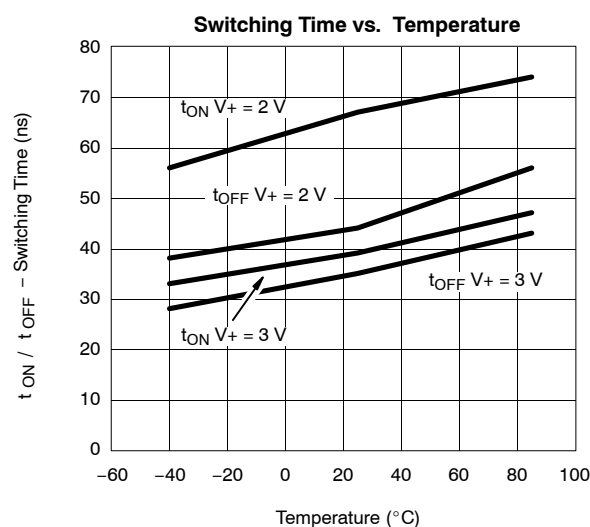
Leakage Current vs. Temperature



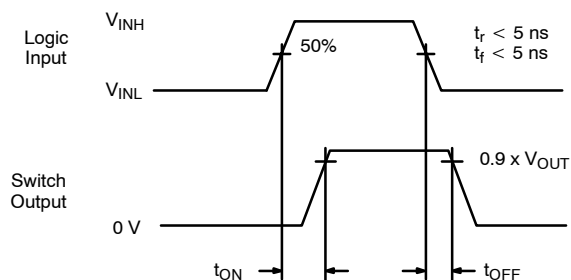
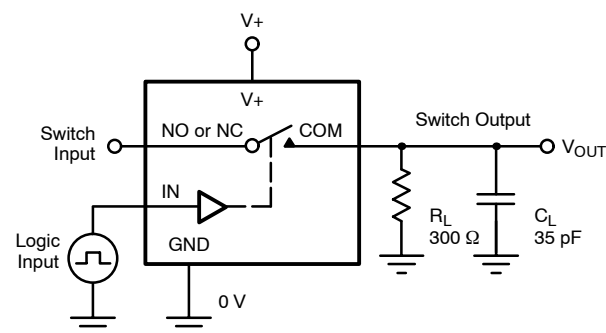
Leakage vs. Analog Voltage



TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



TEST CIRCUITS



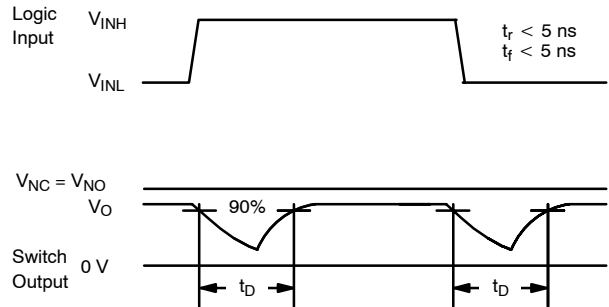
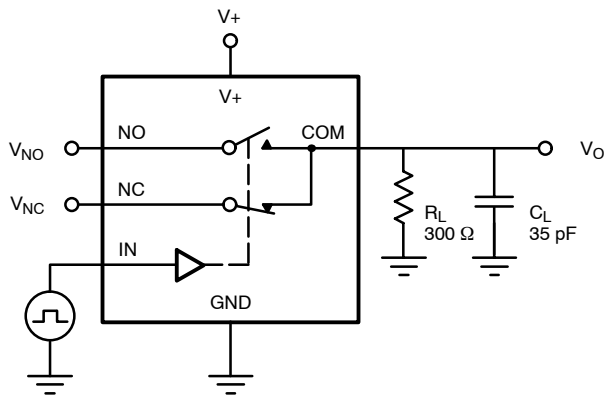
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$

Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

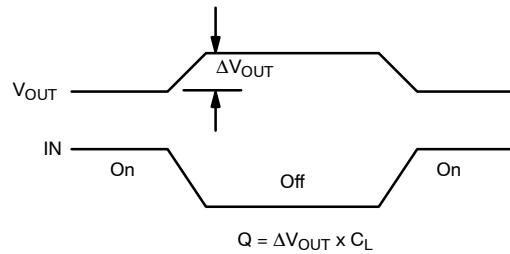
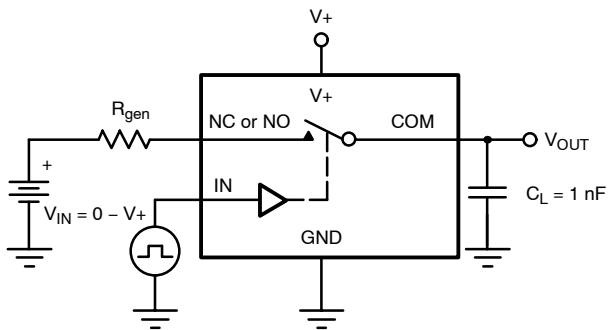
FIGURE 1. Switching Time

TEST CIRCUITS



C_L (includes fixture and stray capacitance)

FIGURE 2. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

FIGURE 3. Charge Injection

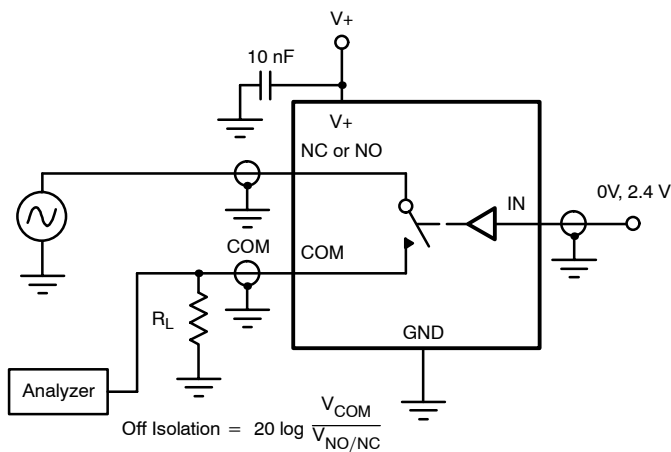


FIGURE 4. Off-Isolation

$$\text{Off Isolation} = 20 \log \frac{V_{\text{COM}}}{V_{\text{NO/NC}}}$$

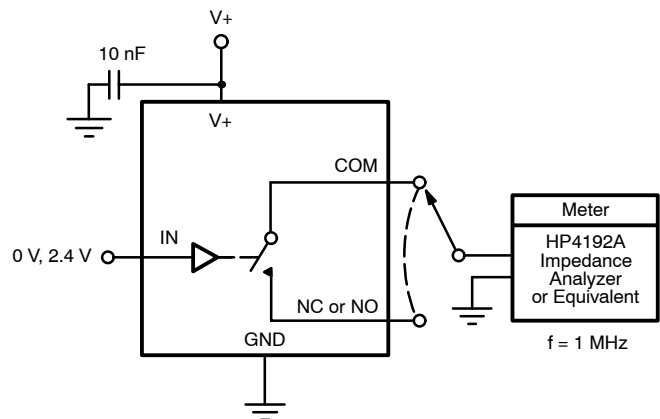


FIGURE 5. Channel Off/On Capacitance