

## > 500 MHz, - 3 dB Bandwidth; Dual SPDT Analog Switch

### DESCRIPTION

DG2721 is a low  $R_{on}$ , high bandwidth analog switch configured in dual SPDT.

It achieves  $5.7 \Omega$  switch on resistance, greater than 500 MHz - 3 dB bandwidth with 5 pF load, and a channel to channel crosstalk and Isolation at - 49 dB.

Fabricated with high density sub micro CMOS process, the DG2721 provides low parasitic capacitance, handles bidirectional signal flow with minimized phase distortion. Guaranteed 1.3 V logic high threshold makes it possible to interface directly with low voltage MCUs.

The DG2721 is designed for a wide range of operating voltages from 2.7 V to 4.3 V that can be driven directly from one cell Li-ion battery. On-chip protection circuit protects against fault events when signals at "com" pins goes beyond  $V+$ .

Latch up current is greater than 300 mA, as per JESD78, and its ESD tolerance exceeds 8 kV.

Packaged in ultra small miniQFN-10 (1.4 mm x 1.8 mm x 0.55 mm), it is ideal for portable high speed mix signal switching application.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with lead (Pb)-free device termination. The miniQFN-10 package has a nickel-palladium-gold device termination and is represented by the lead (Pb)-free "-E4" suffix to the ordering part number. The nickel-palladium-gold device terminations meet all JEDEC standards for reflow and MSL rating.

As a further sign of Vishay Siliconix's commitment, the DG2721 is fully RoHS compliant.

### FEATURES

- Wide operation voltage range
- Low on-resistance,  $5.7 \Omega$  (typical at 3 V)
- Low capacitance, 5.6 pF (typical)
- - 3 dB high bandwidth with 5 pF load: > 500 MHz (typical)
- Low bit to bit skew: 40 pS (typical)
- Low power consumption
- Low logic threshold: V
- Power down protection:  $COM_1$  and  $COM_2$  pins can tolerate up to 5 V when  $V+ = 0$  V
- Logic ( $IN_1$  and  $IN_2$ ) above  $V+$  tolerance
- Latch-up current greater than 300 mA per JESD78
- 8 kV ESD protection (HBM)
- Lead (Pb)-free low profile miniQFN-10 (1.4 mm x 1.8 mm x 0.55 mm)

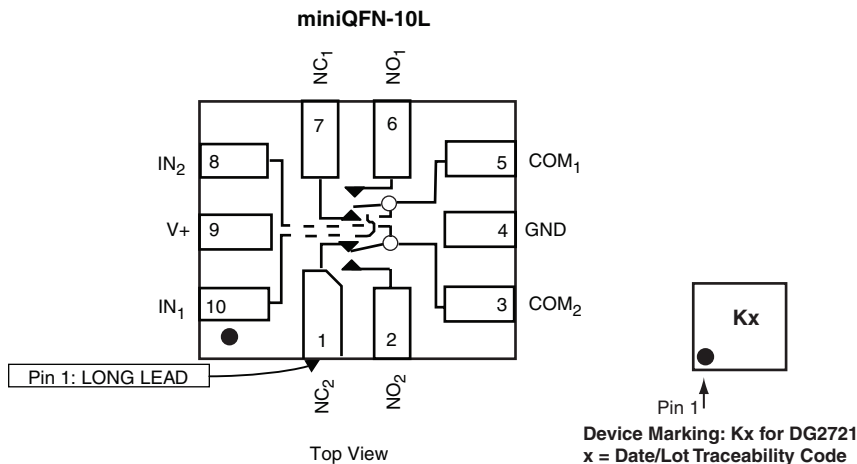


**RoHS**  
COMPLIANT

### APPLICATIONS

- Cellular phones
- Portable media players
- PDA
- Digital camera
- GPS
- Notebook computer
- TV, monitor, and set top box
- Radio

### FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION





ORDERING INFORMATION		
Temp. Range	Package	Part Number
- 40 °C to 85 °C	miniQFN-10	DG2721DN-T1-E4

TRUTH TABLE		
IN <sub>1</sub> (Pin 10)	IN <sub>2</sub> (Pin 8)	Function
X	0	COM2 = NC <sub>2</sub>
X	1	COM2 = NO <sub>2</sub>
0	X	COM1 = NC <sub>1</sub>
1	X	COM1 = NO <sub>1</sub>

PIN DESCRIPTIONS	
Pin Name	Description
IN <sub>1</sub>	Select Input COM <sub>1</sub>
IN <sub>2</sub>	Select Input COM <sub>2</sub>
NC <sub>1/2</sub> , NO <sub>1/2</sub> , COM <sub>1/2</sub>	Data Channel

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted			
Parameter		Limit	Unit
Reference to GND	V+	- 0.3 to 5.5	V
	IN <sub>x</sub> , NC <sub>x</sub> , NO <sub>x</sub> , COM <sub>x</sub> <sup>a</sup>	- 0.3 to (V+ + 0.3)	
Current (Any Terminal except IN <sub>x</sub> , NC <sub>x</sub> , NO <sub>x</sub> , COM <sub>x</sub> )		30	mA
Continuous Current (IN <sub>x</sub> , NC <sub>x</sub> , NO <sub>x</sub> , COM <sub>x</sub> )		± 250	
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 500	
Storage Temperature (D Suffix)		- 65 to 150	°C
Power Dissipation (Packages) <sup>b</sup>	miniQFN-10 <sup>c</sup>	208	mW
ESD (Human Body Model)			
All Pins		4	kV
I/O to GND		8	
Latch-up (Current Injection)		350	mA

Notes:

- a. Signals on IN<sub>x</sub>, NC<sub>x</sub>, NO<sub>x</sub>, COM<sub>x</sub> exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC board.
- c. Derate 2.6 mW/°C above 70 °C.



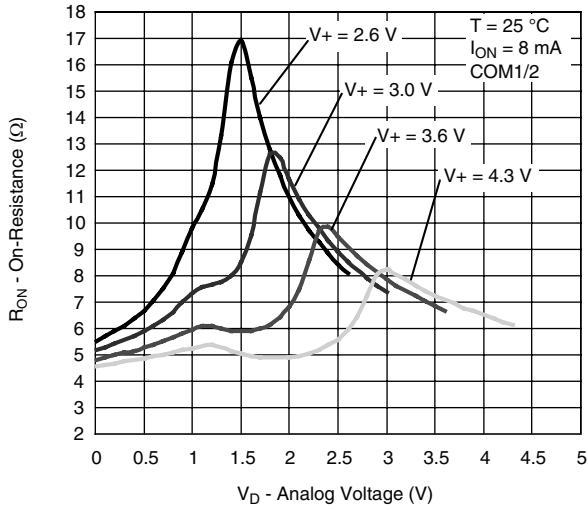
SPECIFICATIONS $V_+ = 3.0\text{ V}$							
Parameter	Symbol	Test Conditions Otherwise Unless Specified	Temp. <sup>a</sup>	Limits - 40 °C to 85 °C			Unit
				Min. <sup>b</sup>	Typ. <sup>c</sup>	Max. <sup>b</sup>	
<b>Analog Switch</b>							
Analog Signal Range <sup>d</sup>	$V_{ANALOG}$	$R_{DS(on)}$	Full	0		$V_+$	V
On-Resistance	$R_{DS(on)}$	$V_+ = 3.0\text{ V}$ , $I_{COM} = 8\text{ mA}$ , $V_{NC/NO} = 0.4\text{ V}$	Room		5.7	7	Ω
			Full			9	
On-Resistance Match <sup>d</sup>	$\Delta R_{ON}$	$V_+ = 3.0\text{ V}$ , $I_{COM} = 8\text{ mA}$ , $V_{NC/NO} = 0.4\text{ V}$	Room		0.35		
On-Resistance Resistance Flatness <sup>d</sup>	$R_{ON}$ Flatness	$V_+ = 3.0\text{ V}$ , $I_{COM} = 8\text{ mA}$ , $V_{NC/NO} = 0.0\text{ V}$ , $1.0\text{ V}$	Room		2		
Switch Off Leakage Current	$I_{(off)}$	$V_+ = 4.3\text{ V}$ , $V_{NC/NO} = 0.3\text{ V}$ , $3.0\text{ V}$ , $V_{COM} = 3.0\text{ V}$ , $0.3\text{ V}$	Full	- 100		100	nA
Channel On Leakage Current	$I_{(on)}$	$V_+ = 4.3\text{ V}$ , $V_{NC/NO} = 0.3\text{ V}$ , $4.0\text{ V}$ , $V_{COM} = 4.0\text{ V}$ , $0.3\text{ V}$	Full	- 200		200	
<b>Digital Control</b>							
Input Voltage High	$V_{INH}$	$V_+ = 3.0\text{ V}$ to $3.6\text{ V}$	Full	1.3			V
		$V_+ = 4.3\text{ V}$	Full	1.7			
Input Voltage Low	$V_{INL}$	$V_+ = 3.0\text{ V}$ to $4.3\text{ V}$	Full			0.5	
Input Capacitance	$C_{IN}$		Full		5.6		pF
Input Current	$I_{INL}$ or $I_{INH}$	$V_{IN} = 0$ or $V_+$	Full	- 1		1	μA
<b>Dynamic Characteristics</b>							
Break-Before-Make Time <sup>e, d</sup>	$t_{BBM}$	$V_+ = 3.0\text{ V}$ , $V_{COM} = 1.5\text{ V}$ , $R_L = 50\text{ }\Omega$ , $C_L = 35\text{ pF}$	Room		5		ns
			Full				
Turn-On Time <sup>e, d</sup>	$t_{ON}$		Room			30	
			Full				
Turn-Off Time <sup>e, d</sup>	$t_{OFF}$		Room			25	
			Full				
Charge Injection <sup>d</sup>	$Q_{INJ}$	$C_L = 1\text{ nF}$ , $R_{GEN} = 0\text{ }\Omega$ , $V_{GEN} = 0\text{ V}$	Room		0.5		pC
Off-Isolation <sup>d</sup>	OIRR	$V_+ = 3.0\text{ V}$ to $3.6\text{ V}$ , $R_L = 50\text{ }\Omega$ , $C_L = 5\text{ pF}$ , $f = 240\text{ MHz}$			- 30		dB
Crosstalk <sup>d</sup>	$X_{TALK}$				- 49		
Bandwidth <sup>d</sup>	BW	$V_+ = 3.0\text{ V}$ to $3.6\text{ V}$ , $R_L = 50\text{ }\Omega$ , $C_L = 5\text{ pF}$ , - 3 dB			> 500		MHz
Channel-Off Capacitance <sup>d</sup>	$C_{NO(off)}$	$V_+ = 3.3\text{ V}$ , $f = 1\text{ MHz}$			4		pF
	$C_{NC(off)}$				4		
Channel-On Capacitance <sup>d</sup>	$C_{COM(on)}$				11		
Channel-to-Channel Skew <sup>d</sup>	$t_{SK(O)}$			50			
Skew Off Opposite Transitions of the Same Output <sup>d</sup>	$t_{SK(p)}$	$V_+ = 3.0\text{ V}$ to $3.6\text{ V}$ , $R_L = 50\text{ }\Omega$ , $C_L = 5\text{ pF}$			20	ps	
Total Jitter <sup>d</sup>	$t_J$				200		
<b>Power Supply</b>							
Power Supply Range	$V_+$			2.6		4.3	V
Power Supply Current	$I_+$	$V_{IN} = 0\text{ V}$ , or $V_+$	Full			2	μA

Notes:

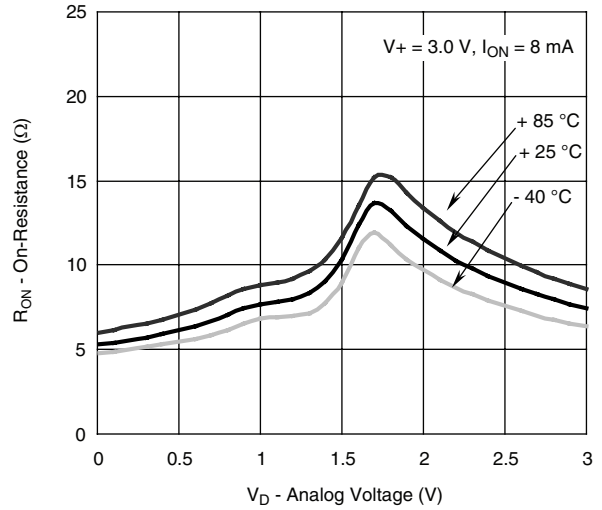
- a. Room = 25 °C, Full = as determined by the operating suffix.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Typical values are for design aid only, not guaranteed nor subject to production testing.
- d. Guarantee by design, not subjected to production test.
- e.  $V_{IN}$  = input voltage to perform proper function.
- f. Crosstalk measured between channels.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

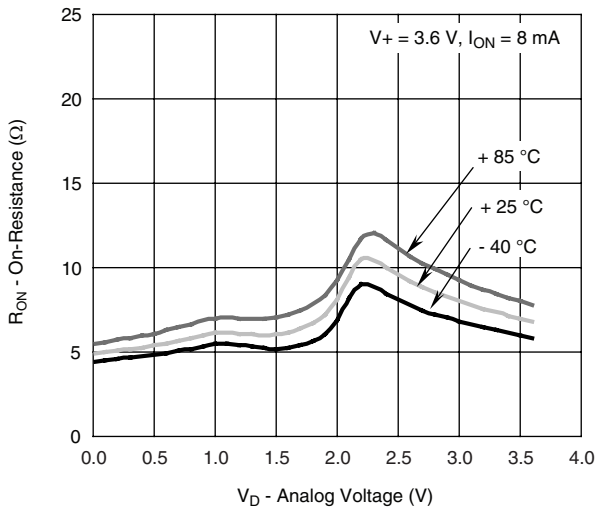
**TYPICAL CHARACTERISTICS**  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted



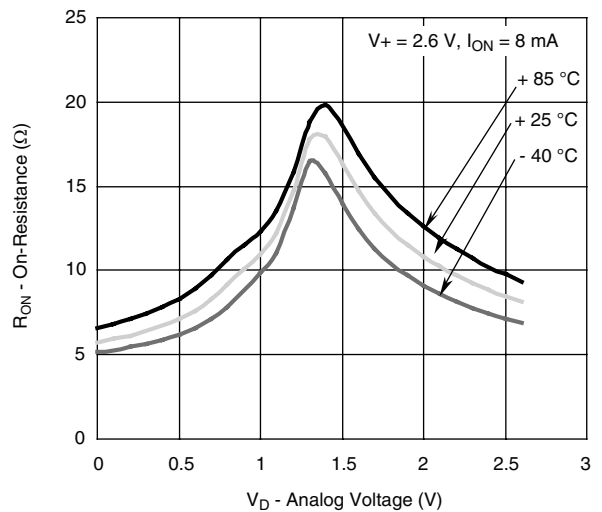
**On-Resistance vs.  $V_D$  and Single Supply Voltage**



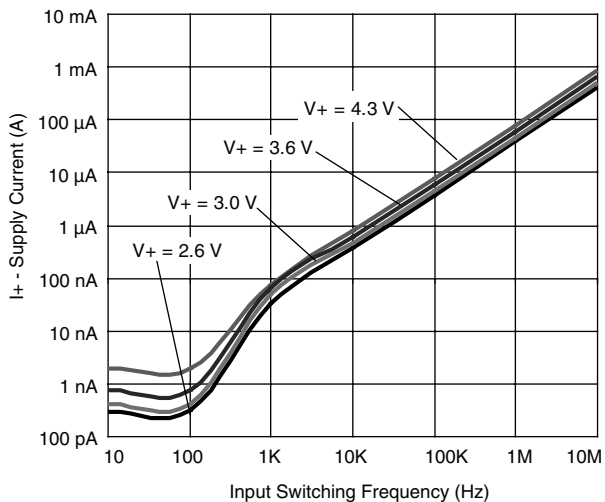
**On-Resistance vs. Analog Voltage and Temperature**



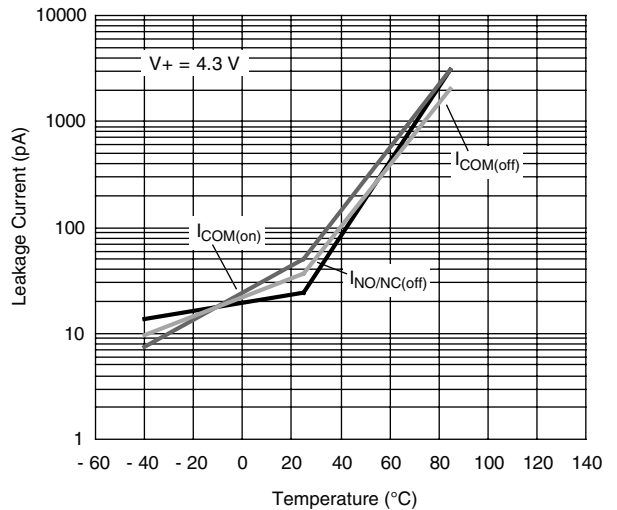
**On-Resistance vs. Analog Voltage and Temperature**



**On-Resistance vs. Analog Voltage and Temperature**

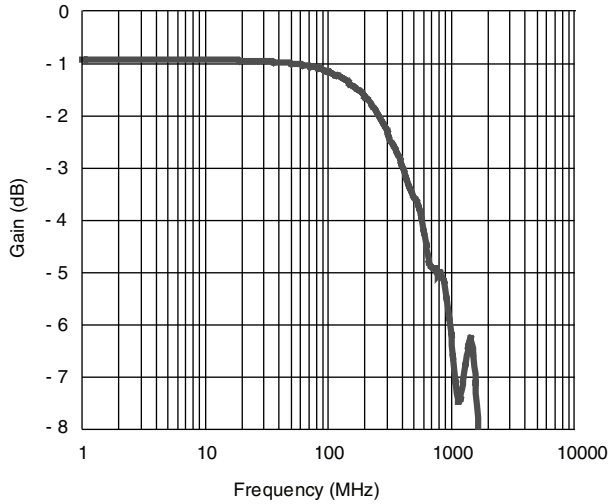


**Supply Current vs. Input Switching Frequency**

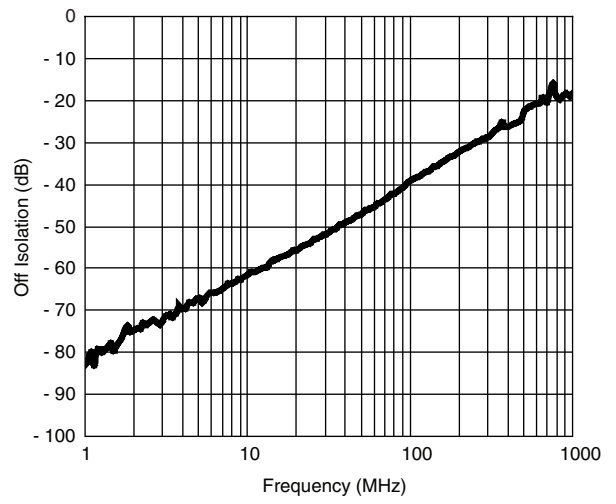


**Leakage Current vs. Temperature**

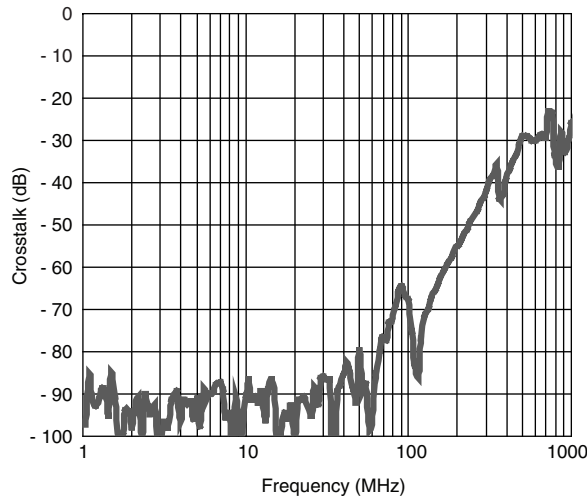
**TYPICAL CHARACTERISTICS**  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted



Gain vs. Frequency,  $C_L = 5\text{ pF}$ ,  $V_+ = 3.3\text{ V}$

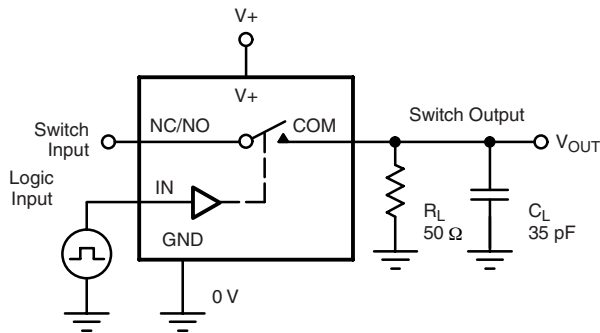


Off Isolation,  $V_+ = 3.3\text{ V}$



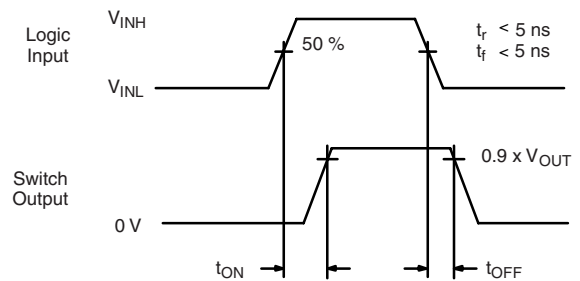
Crosstalk,  $V_+ = 3.3\text{ V}$

**TEST CIRCUITS**



$C_L$  (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM} \left( \frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On  
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time

TEST CIRCUITS

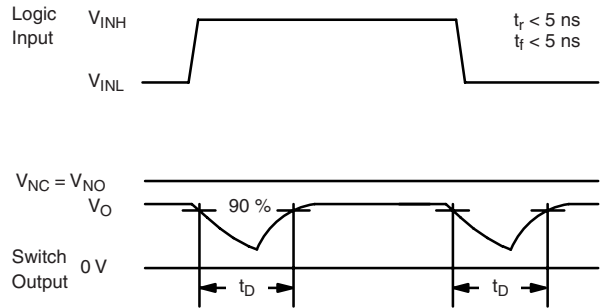
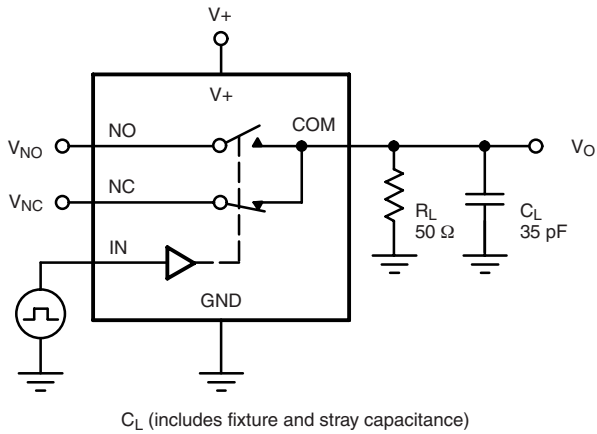
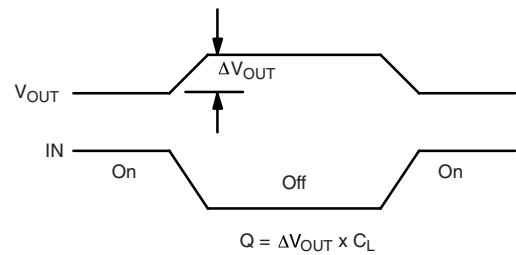
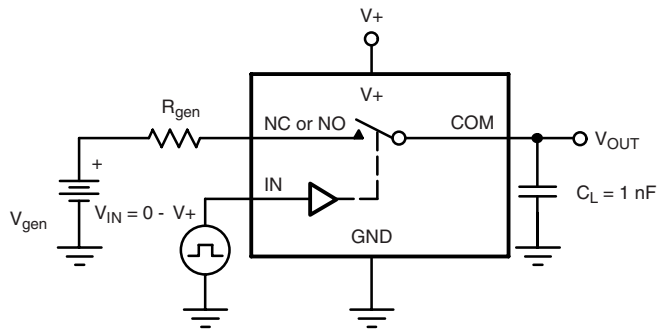


Figure 2. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

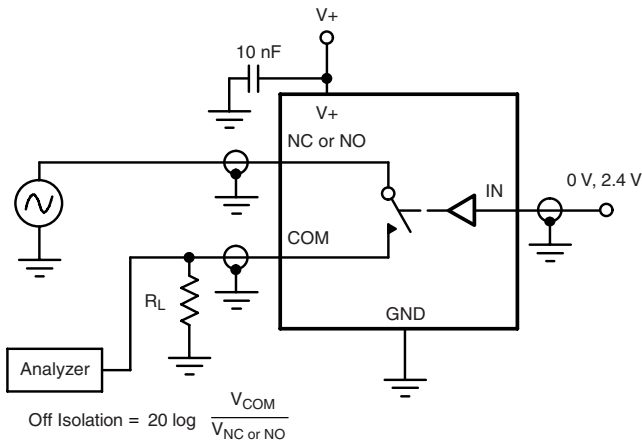


Figure 4. Off-Isolation

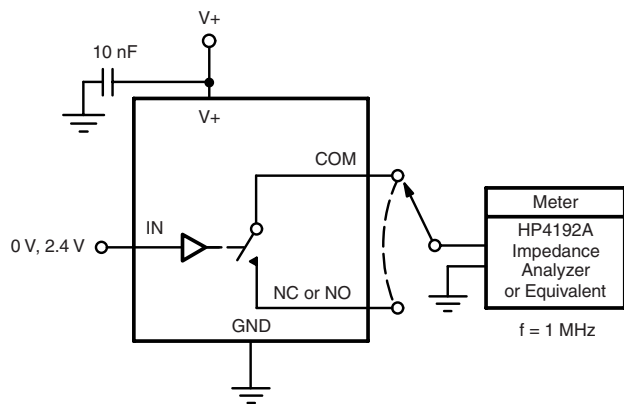
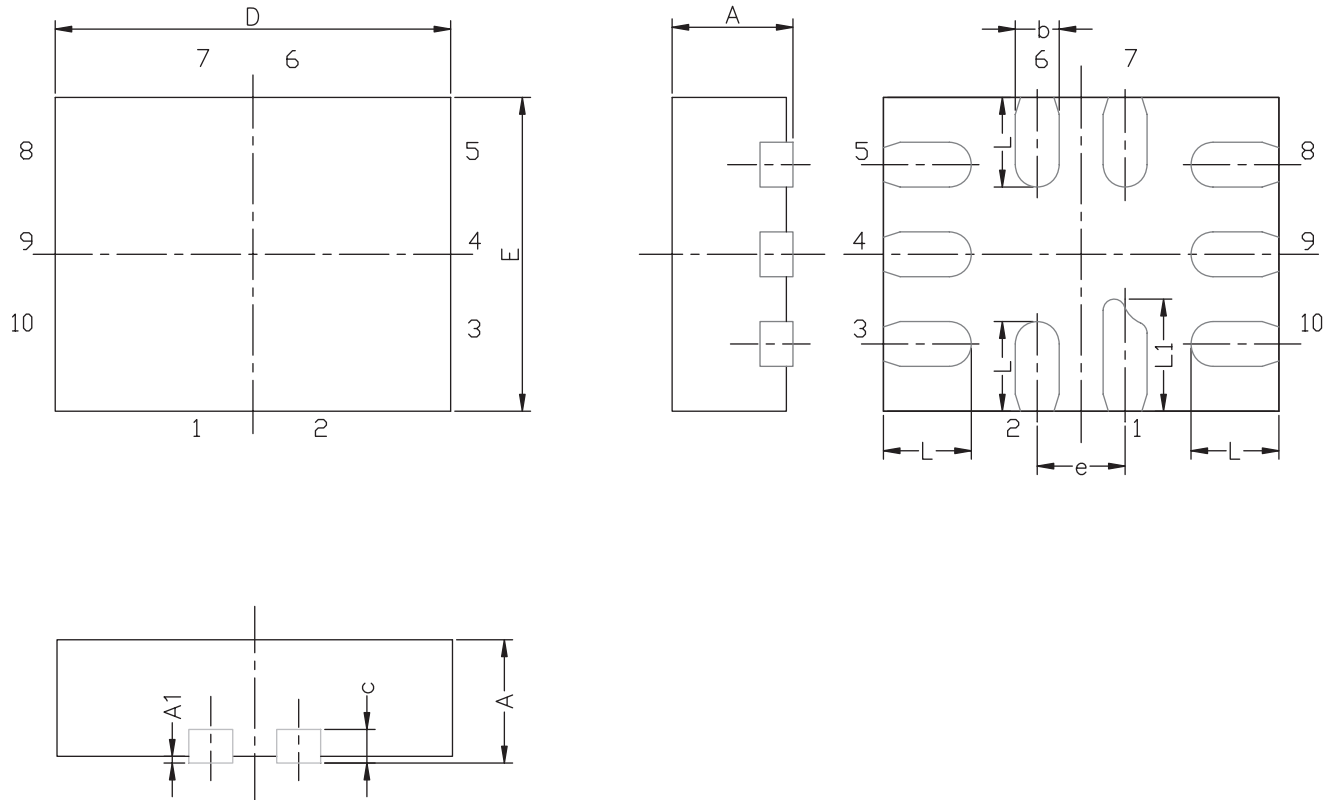


Figure 5. Channel Off/On Capacitance

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## MINI QFN-10L CASE OUTLINE



DIM	MILLIMETERS			INCHES		
	MIN.	NAM.	MAX.	MIN.	NAM.	MAX.
A	0.50	0.55	0.60	0.0197	0.0217	0.0236
A1	0.00	-	0.05	0.000	-	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
c	0.15 REF			0.006 REF		
D	1.75	1.80	1.85	0.069	0.071	0.073
E	1.35	1.40	1.45	0.053	0.055	0.057
e	0.40 BSC			0.016 BSC		
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.45	0.50	0.55	0.0177	0.0197	0.0217

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DWG: 5957



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