Low On-Resistance Wideband/Video Switches

FEATURES

- Wide Bandwidth: 500 MHz
- Low Crosstalk at 5 MHz: –85 dB
- Low $r_{DS(on)}$: 5 Ω, DG642
- TTL Logic Compatible
- Fast Switching: t_{ON} 50 ns
- Single Supply Compatibility
- High Current: 100 mA, DG642

BENEFITS

- High Precision
- Improved Frequency Response
- Low Insertion Loss
- Improved System Performance
- Reduced Board Space
- Low Power Consumption

APPLICATIONS

- RF and Video Switching
- RGB Switching
- Video Routing
- Cellular Communications
- ATE
- Radar/FLIR Systems
- Satellite Receivers
- Programmable Filters

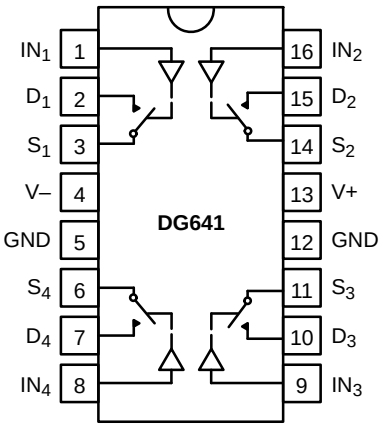
DESCRIPTION

The DG641/642/643 are high performance monolithic video switches designed for switching wide bandwidth analog and digital signals. DG641 is a quad SPST, DG642 is a single SPDT, and DG643 is a dual SPDT function. These devices have exceptionally low on-resistances (5 Ω typ—DG642), low capacitance and high current handling capability.

To achieve TTL compatibility, low channel capacitances and fast switching times, the DG641/642/643 are built on the Vishay Siliconix proprietary D/CMOS process. Each switch conducts equally well in both directions when on, and blocks up to 14 V_{p-p} when off. An epitaxial layer prevents latchup.

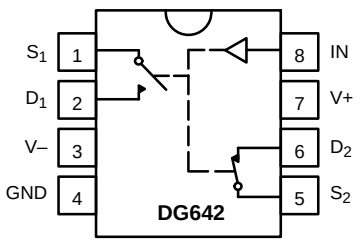
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

Dual-In-Line and SOIC



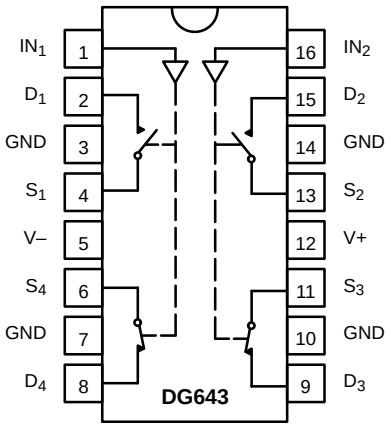
Top View

Dual-In-Line and SOIC



Top View

Dual-In-Line and SOIC



Top View

TRUTH TABLE—DG641	
Logic	**Switch**
0	OFF
1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

TRUTH TABLE—DG642		
Logic	**SW_1**	**SW_2**
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

TRUTH TABLE—DG643		
Logic	**SW_1, SW_2**	**SW_3, SW_4**
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
DG641		
–40 to 85°C	16-Pin Plastic DIP	DG641DJ
	16-Pin Narrow SOIC	DG641DY
DG642		
–40 to 85°C	8-Pin Plastic DIP	DG642DJ
	8-Pin Narrow SOIC	DG642DY
DG643		
–40 to 85°C	16-Pin Plastic DIP	DG643DJ
	16-Pin Narrow SOIC	DG643DY

ABSOLUTE MAXIMUM RATINGS

V+ to V– . . . . . –0.3 V to 21 V
V+ to GND . . . . . –0.3 V to 21 V
V– to GND . . . . . –19 V to +0.3 V
Digital Inputs . . . . . (V–) –0.3 V to (V+) +0.3 V
or 20 mA, whichever occurs first
V_S, V_D . . . . . (V–) –0.3 V to (V–) +14 V
or 20 mA, whichever occurs first
Continuous Current (Any Terminal Except S or D) . . . . . 20 mA
Continuous Current S or D: DG641/643 . . . . . 75 mA
DG642 . . . . . 100 mA
Current, S or D (Pulsed 1 ms, 10% duty cycle max)
DG641/643 . . . . . 200 mA
DG642 . . . . . 300 mA

Storage Temperature . . . . . –65 to 125°C
Power Dissipation (Package)[b]
8-Pin Plastic DIP and Narrow SOIC[c] . . . . . 300 mW
16-Pin Plastic DIP[d] . . . . . 470 mW
16-Pin Narrow SOIC[e] . . . . . 600 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 7.6 mW/°C above 75°C
d. Derate 6 mW/°C above 75°C
e. Derate 80 mW/°C above 75°C

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

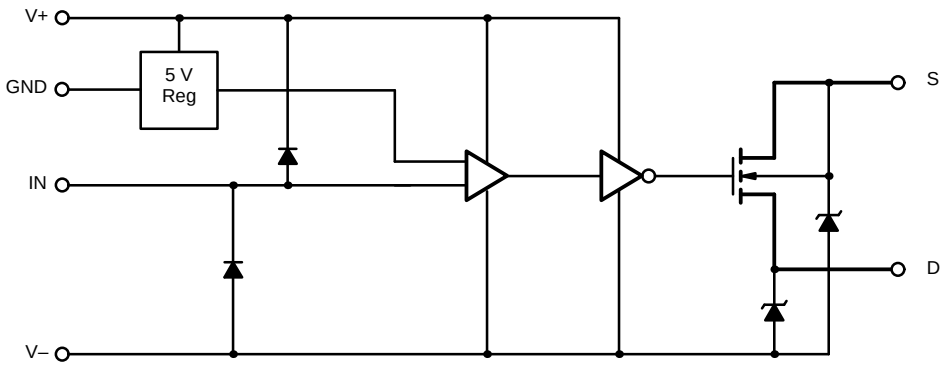


FIGURE 1.

SPECIFICATIONS FOR DG641 AND DG643

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V– = –3 V V_{INH} = 2.4 V, V_{INL} = 0.8 V[e]	Temp[a]	Limits –40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[dd]	V_{ANALOG}	V– = –5 V, V+ = 12 V	Full	–5		8	V
		V– = GND, V+ = 12 V	Full	0		8	
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = –10 mA, V_D = 0 V	Room Full		8	15 20	Ω
$r_{DS(on)}$ Match	$\Delta r_{DS(on)}$		Room		1	2	
Source Off Leakage Current	$I_{S(off)}$	V_S = 0 V, V_D = 10 V	Room Full	–10 –100	–0.02	10 100	nA
Drain Off Leakage Current	$I_{D(off)}$	V_S = 10 V, V_D = 0V	Room Full	–10 –100	–0.02	10 100	
Channel On Leakage Current	$I_{D(on)}$	V_S = V_D = 0 V	Room Full	–10 –100	–0.1	10 100	
Digital Control							
Input Voltage High	V_{INH}		Full	2.4			V
Input Voltage Low	V_{INL}		Full			0.8	
Input Current	I_{IN}	V_{IN} = GND or V+	Room Full	–1 –20	0.05	1 20	µA
Dynamic Characteristics							
On State Input Capacitance[d]	$C_{S(on)}$	V_S = V_D = 0 V	Room		10	20	pF
Off State Input Capacitance[d]	$C_{S(off)}$	V_S = 0 V	Room		4	12	
Off State Output Capacitance[d]	$C_{D(off)}$	V_D = 0 V	Room		4	12	
Bandwidth	BW	R_L = 50 Ω, See Figure 6	Room		500		MHz
Turn On Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF, See Figure 2	Room Full		50	70 140	ns
Turn Off Time	t_{OFF}		Room Full		28	50 85	
Charge Injection	Q	C_L = 1000 pF, V_D = 0 V, See Figure 3	Room		–19		pC
Off Isolation	OIRR	R_{IN} = 75 Ω, R_L = 75 Ω, f = 5 MHz See Figure 4	Room		–60		dB
All Hostile Crosstalk	$X_{TALK(AH)}$	R_{IN} = 10 Ω, R_L = 75 Ω, f = 5 MHz See Figure 5	Room		–87		
Power Supplies							
Positive Supply Current	I+	V_{IN} = 0 V or V_{IN} = 5 V	Room Full		3.5	6 9	mA
Negative Supply Current	I–		Room Full	–6 –9	–3		

Notes:
a. Room = 25°C, Full = as determined by the operating temperature suffix.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guaranteed by design, not subject to production test.
e. V_{IN} = input voltage to perform proper function.

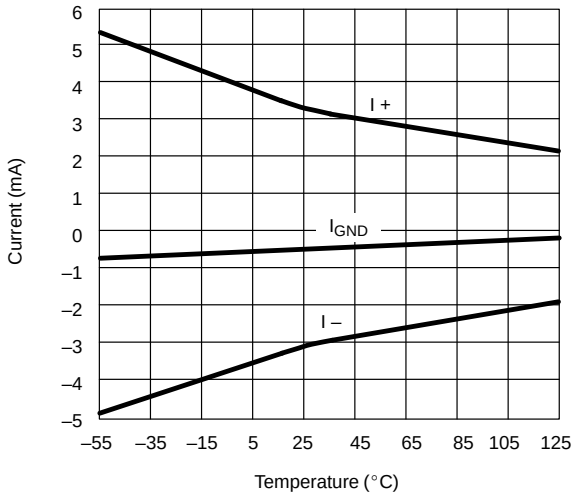
SPECIFICATIONS FOR DG642

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V– = –3 V V_{INH} = 2.4 V, V_{INL} = 0.8 V[e]	Temp[a]	Limits –40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}	V– = –5 V, V+ = 12 V	Full	–5		8	V
		V– = GND, V+ = 12 V	Full	0		8	
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = –10 mA, V_D = 0 V	Room Full		5	8 9	Ω
$r_{DS(on)}$ Match	$\Delta r_{DS(on)}$		Room		0.5	1	
Source Off Leakage Current	$I_{S(off)}$	V_S = 0 V, V_D = 10 V	Room Full	–10 –200	–0.04	10 200	nA
Drain Off Leakage Current	$I_{D(off)}$	V_S = 10 V, V_D = 0V	Room Full	–10 –200	–0.04	10 200	
Channel On Leakage Current	$I_{D(on)}$	V_S = V_D = 0 V	Room Full	–10 –200	–0.2	10 200	
Digital Control							
Input Voltage High	V_{INH}		Full	2.4			V
Input Voltage Low	V_{INL}		Full			0.8	
Input Current	I_{IN}	V_{IN} = GND or V+	Room Full	–1 –20	0.05	1 20	µA
Dynamic Characteristics							
On State Input Capacitance[d]	$C_{S(on)}$	V_S = V_D = 0 V	Room		19	40	pF
Off State Input Capacitance[d]	$C_{S(off)}$	V_S = 0 V	Room		8	20	
Off State Output Capacitance[d]	$C_{D(off)}$	V_D = 0 V	Room		8	20	
Bandwidth	BW	R_L = 50 Ω, See Figure 6	Room		500		MHz
Turn On Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF, See Figure 2	Room Full		60	100 160	ns
Turn Off Time	t_{OFF}		Room Full		40	60 100	
Charge Injection	Q	C_L = 1000 pF, V_D = 0 V, See Figure 3	Room		–40		pC
Off Isolation		R_{IN} = 75 Ω, R_L = 75 Ω, f = 5 MHz See Figure 4	Room		–63		dB
All Hostile Crosstalk	$X_{TALK(AH)}$	R_{IN} = 10 Ω, R_L = 75 Ω, f = 5 MHz See Figure 5	Room		–85		
Power Supplies							
Positive Supply Current	I+	V_{IN} = 0 V or V_{IN} = 5 V	Room Full		3.5	6 9	mA
Negative Supply Current	I–		Room Full	–6 –9	–3		

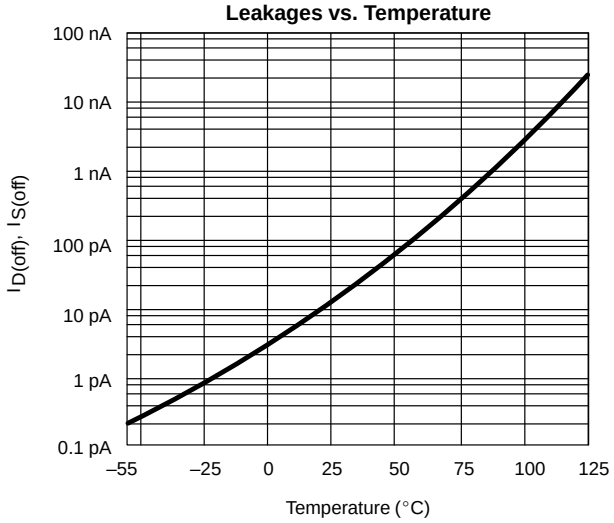
Notes:
a. Room = 25°C, Full = as determined by the operating temperature suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. Guaranteed by design, not subject to production test.
e. V_{IN} = input voltage to perform proper function.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

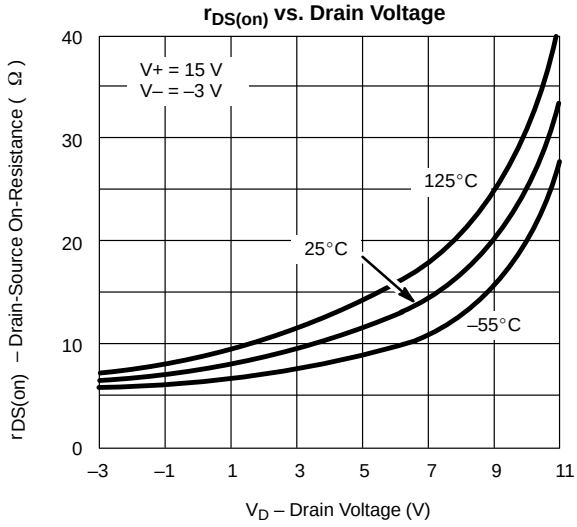
Supply Current vs. Temperature



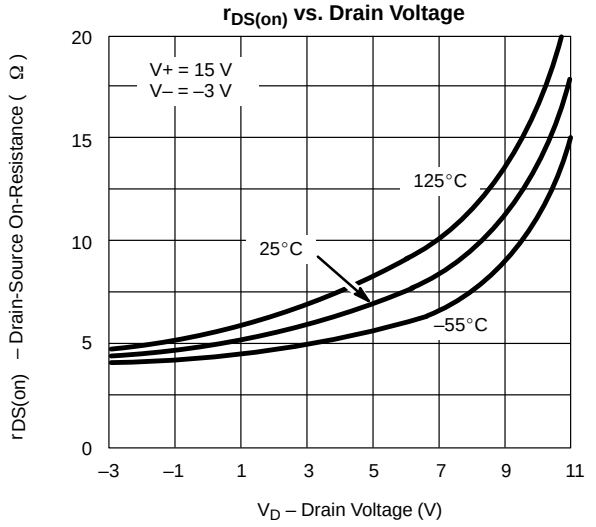
Leakages vs. Temperature



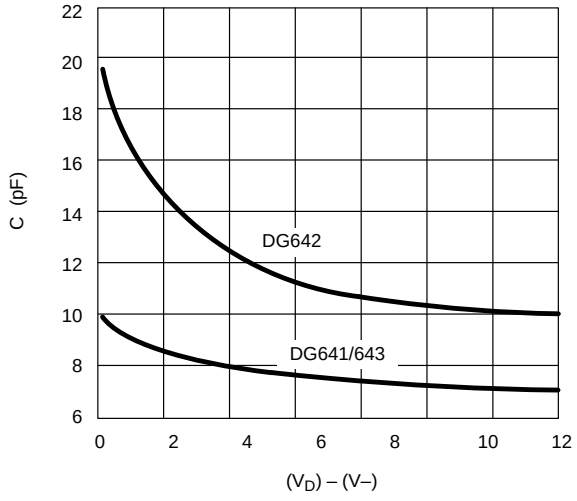
DG641/643
$r_{DS(on)}$ vs. Drain Voltage



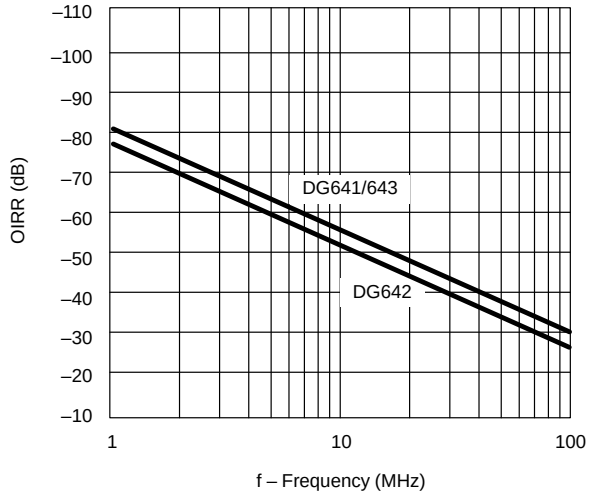
DG642
$r_{DS(on)}$ vs. Drain Voltage



On Capacitance

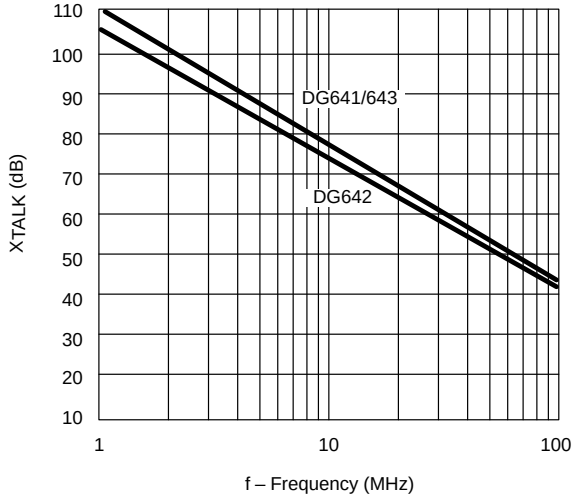


Off Isolation

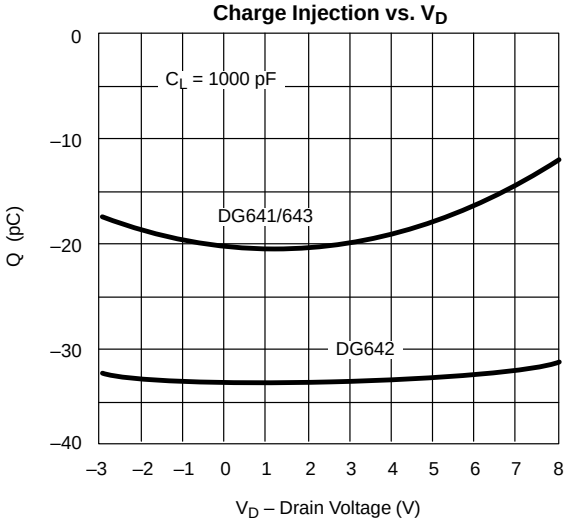


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

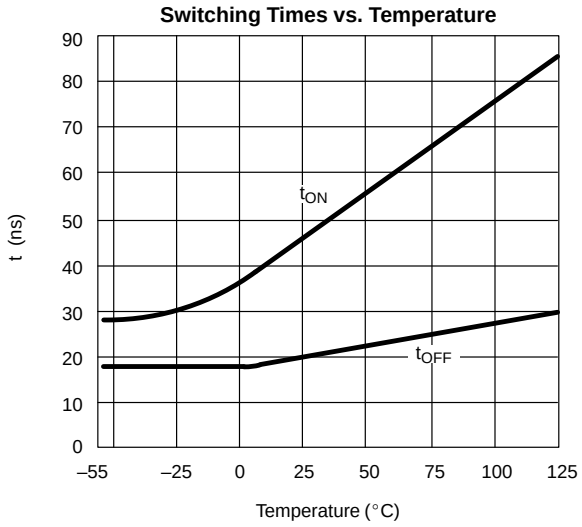
All Hostile Crosstalk



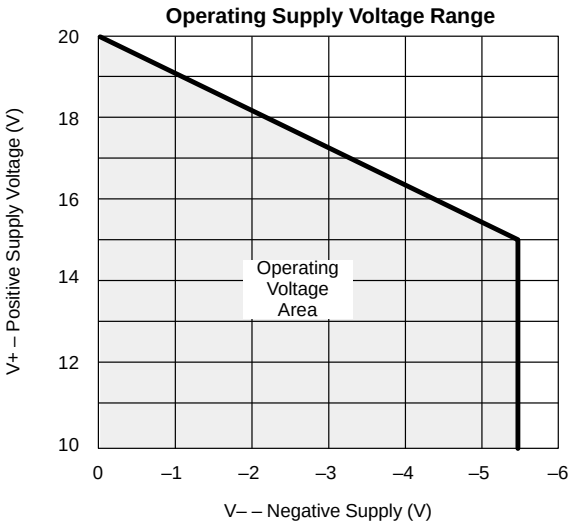
Charge Injection vs. V_D



Switching Times vs. Temperature



Operating Supply Voltage Range



TEST CIRCUITS

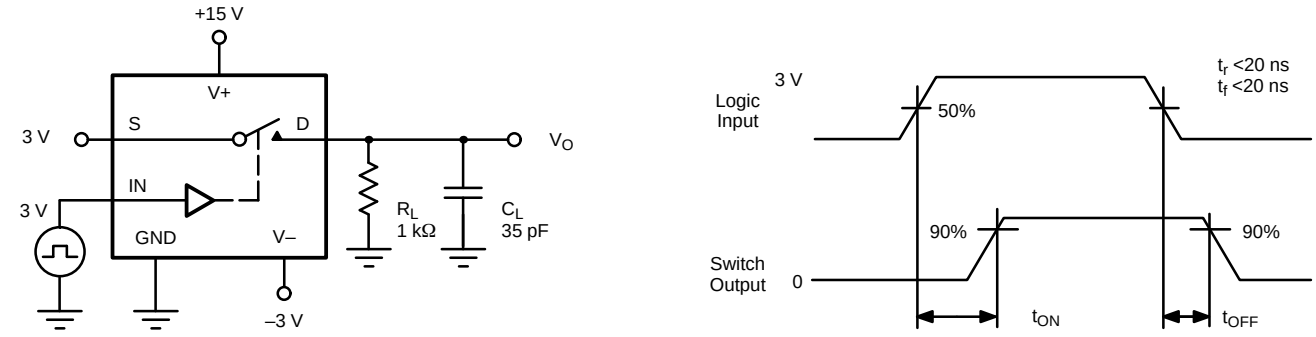


FIGURE 2. Switching Time

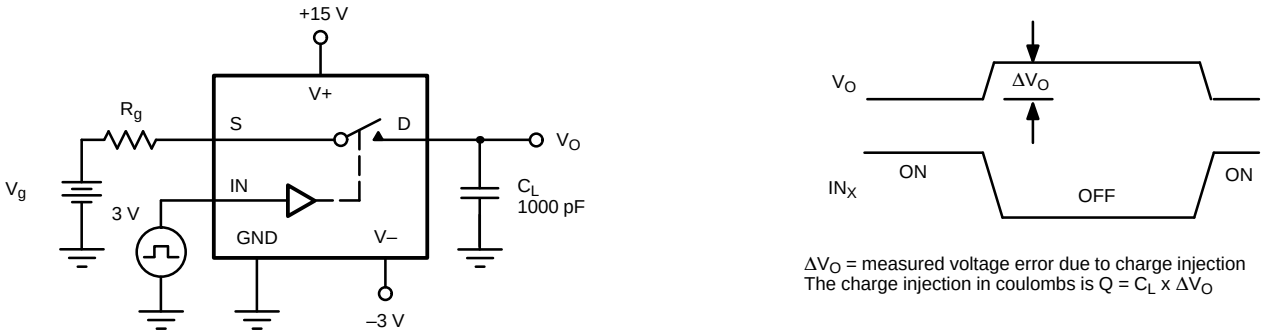


FIGURE 3. Charge Injection

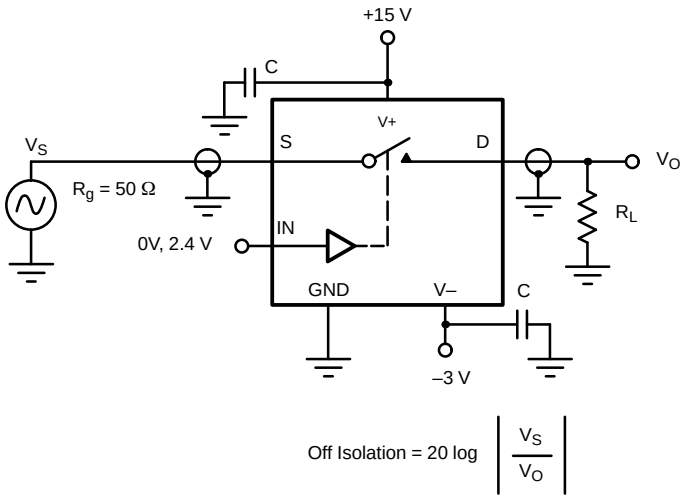


FIGURE 4. Off Isolation

TEST CIRCUITS

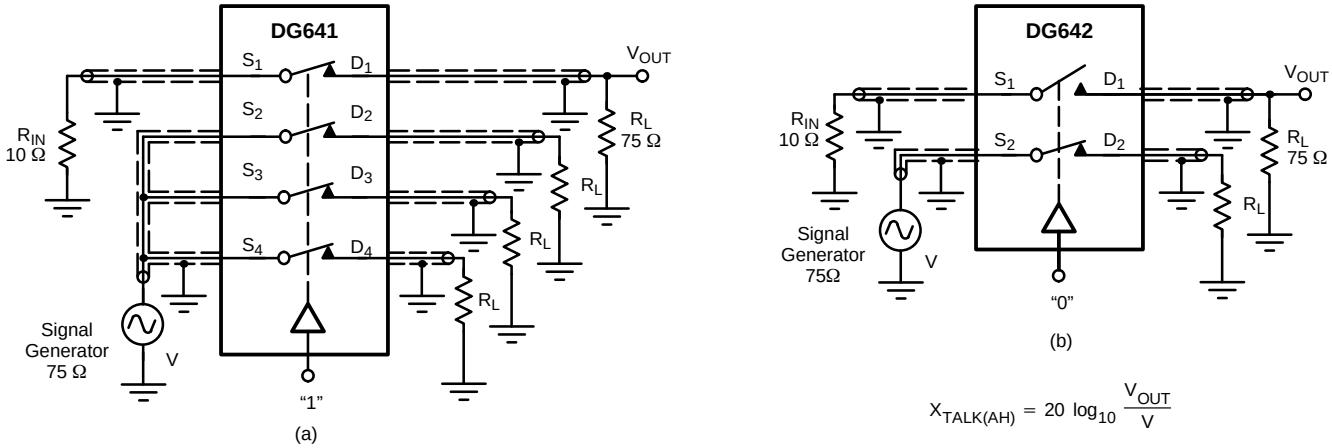


FIGURE 5. All Hostile Crosstalk – $X_{TALK(AH)}$

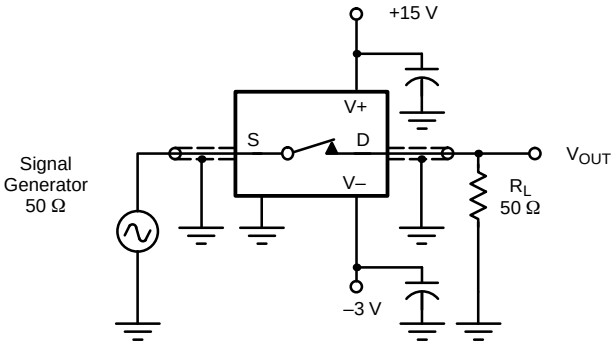


FIGURE 6. Bandwidth

APPLICATIONS

Device Description

The DG641/642/643 switches offer true bidirectional switching of high frequency analog or digital signals with minimum signal crosstalk, low insertion loss, and negligible non-linearity distortion and group delay.

Built on the Siliconix D/CMOS process, these switches provide excellent off-isolation with a bandwidth of around 500 MHz. The silicon-gate D/CMOS processing also yields fast switching speeds.

An on-chip regulator circuit maintains TTL input compatibility over the whole operating supply voltage range shown, easing control logic interfacing.

Circuit layout is facilitated by the interchangeability of source and drain terminals.

Frequency Response

A single switch on-channel exhibits both resistance [$r_{DS(on)}$] and capacitance [$C_{S(on)}$]. This RC combination has an attenuation effect on the analog signal – which is frequency dependent (like an RC low-pass filter). The –3 dB bandwidth of the DG641/642/643 is typically 500 MHz (into 50 Ω).

APPLICATIONS

Power Supplies

Power supply flexibility is a useful feature of the DG641/642/643 series. It can be operated from a single positive supply (V+) if required (V– connected to ground).

Note that the analog signal must not exceed V– by more than –0.3 V to prevent forward biasing the substrate p-n junction. The use of a V– supply has a number of advantages:

1. It allows flexibility in analog signal handling, i.e., with V– = –5 V and V+ = 12 V; up to ±5-V ac signals can be controlled.
2. The value of on capacitance [$C_{S(on)}$] may be reduced. A property known as 'the body-effect' on the DMOS switch devices causes various parametric effects to occur. One of these effects is the reduction in $C_{S(on)}$ for an increasing V body-source. Note however that to increase V– normally requires V+ to be reduced (since V+ to V– = 21 V max.). A reduction in V+ causes an increase in $r_{DS(on)}$, hence a compromise has to be achieved. It is also useful to note that tests indicate that optimum video linearity performance (e.g., differential phase and gain) occurs when V– is around –3 V.
3. V– eliminates the need to bias the analog signal using potential dividers and large coupling capacitors.

Decoupling

It is an established rf design practice to incorporate sufficient bypass capacitors in the circuit to decouple the power supplies to all active devices in the circuit. The dynamic performance of the DG641/642/643 series is adversely affected by poor decoupling of power supply pins. Also, of even more significance, since the substrate of the device is connected to the negative supply, adequate decoupling of this pin is essential. Suitable decoupling capacitors are 1- to 10-μF tantalum bead, plus 10- to 100-nF ceramic or polyester.

Rules:

1. Decoupling capacitors should be incorporated on all power supply pins (V+, V–). (See Figure 7).
2. They should be mounted as close as possible to the device pins.
3. Capacitors should be of a suitable type with good high frequency characteristics – tantalum bead and/or ceramic disc types are adequate.

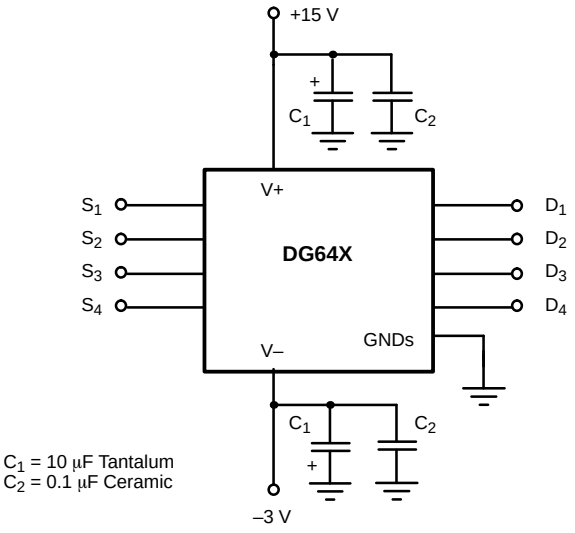


FIGURE 7. Supply Decoupling

Board Layout

PCB layout rules for good high frequency performance must also be observed to achieve the performance boasted by these analog switches. Some tips for minimizing stray effects are:

1. Use extensive ground planes on double sided PCB, separating adjacent signal paths. Multilayer PCB is even better.
2. Keep signal paths as short as practically possible, with all channel paths of near equal length.
3. Careful arrangement of ground connections is also very important. Star connected system grounds eliminate signal current, flowing through ground path parasitic resistance, from coupling between channels.

Figure 8 shows a 4-channel video multiplexer using a DG641.

In Figure 9, two coax cables terminated on 75 Ω bring two video signals to the DG642 switch. The two drains tied together lower the on-state capacitance. An Si582 video amplifier drives a double terminated 75-Ω cable. The double terminated coax cable eliminates line reflections.

APPLICATIONS

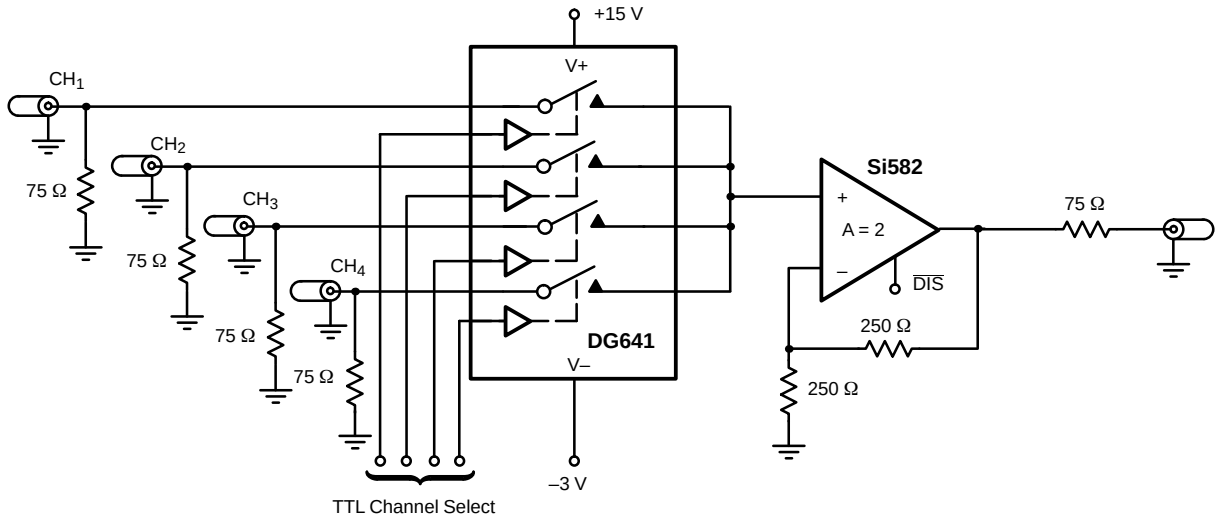


FIGURE 8. 4 by 1 Video Multiplexing Using the DG641

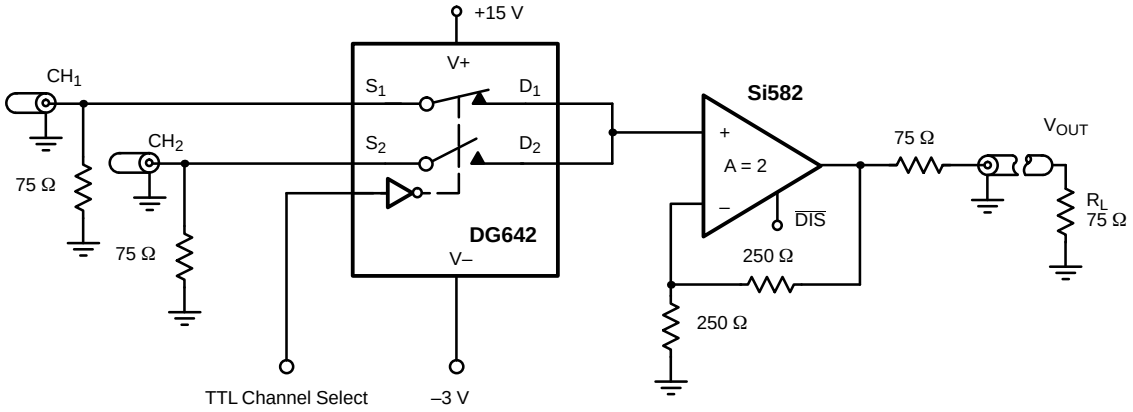


FIGURE 9. 2-Channel Video Selector Using the DG642

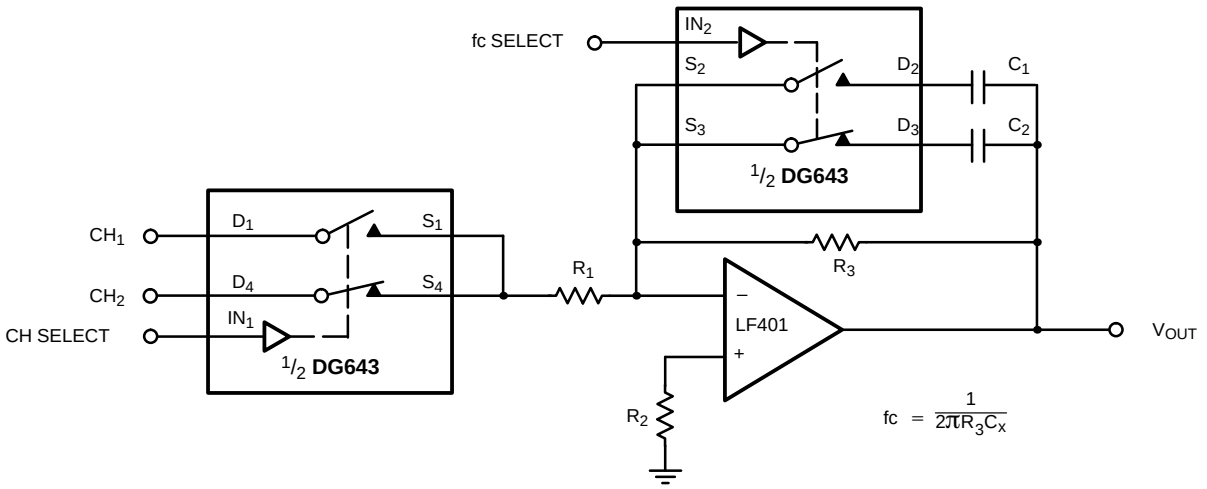


FIGURE 10. Active Low Pass Filter with Selectable Inputs and Break Frequencies