Memory/Clock Drivers

DH3467C quad PNP core driver

general description

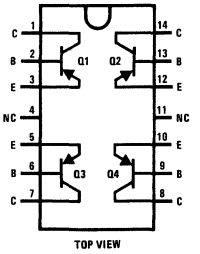
The DH3467C consists of four 2N3467 type PNP transistors mounted in a 14-pin molded dual-in-line package. The device is primarily intended for core memory application requiring operating currents in the ampere range, high stand-off voltage, and fast turn-on and turn-off times.

typical characteristics

Turn-ON Time	18 ns
Turn-OFF Time	45 ns
Collector Current	1A
Collector-Base Breakdown Voltage	120V typ.
Collector Saturation Voltage at I_C = 1A	0.55V
Collector Saturation Voltage at I_C = 0.5A	0.31V

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DH3467CD
See Package 1
Order Number DH3467CN
See Package 22

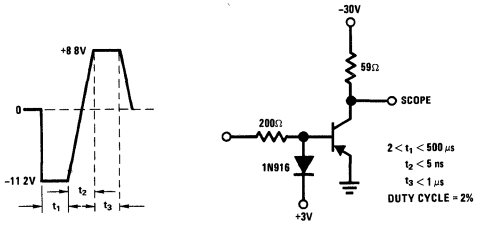


FIGURE 1. Turn-On Equivalent Test Circuit

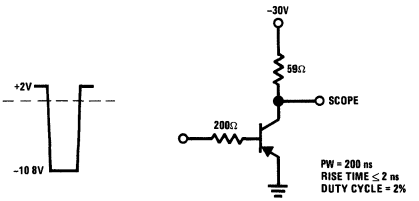


FIGURE 2. Turn-Off Equivalent Test Circuit

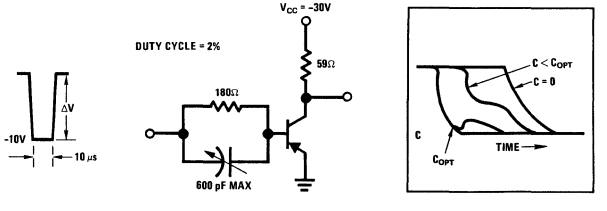


FIGURE 3. Q_T Test Circuit

absolute maximum ratings

Collector to Base Voltage	40V
Collector to Emitter Voltage	40V
Collector to Emitter Voltage (Note 1)	40V
Emitter to Base Voltage	5V
Collector Current – Continuous	1.0A
Power Dissipation (T_A = 25°C) (each device)	0.85W
Power Dissipation (T_A = 25°C) (total package)	2.5W
Operating Junction Temperature	150°C Max
Operating Temperature Range	0°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

electrical characteristics (T_A = 25°C, unless otherwise specified)

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Collector to Base Breakdown Voltage (BV_{CBO})	I_C = 10 μA I_E = 0	−40		V
Emitter to Base Breakdown Voltage (BV_{EBO})	I_E = 10 μA I_C = 0	−5 0		V
Collector to Emitter Breakdown Voltage (Note 1) (BV_{CEO})	I_C = 10 mA I_B = 0	−40		V
DC Pulse Current Gain (Note 1) (h_{FE})	I_C = 150 mA V_{CE} = −1.0V	40		
DC Pulse Current Gain (Note 1) (h_{FE})	I_C = 500 mA V_{CE} = −1 0V	40	120	
DC Pulse Current Gain (Note 1) (h_{FE})	I_C = 1.0A V_{CE} = −5 0V	40		
Pulsed Collector Saturation Voltage (Note 1) ($V_{CE(sat)}$)	I_C = 150 mA I_B = 15 mA		−0.30	V
Pulsed Collector Saturation Voltage (Note 1) ($V_{CE(sat)}$)	I_C = 500 mA I_B = 50 mA		−0.50	V
Pulsed Collector Saturation Voltage (Note 1) ($V_{CE(sat)}$)	I_C = 1 0A I_B = 100 mA		−1.0	V
Pulsed Base Saturation Voltage (Note 1) ($V_{BE(sat)}$)	I_C = 150 mA I_B = 15 mA		−1.0	V
Pulsed Base Saturation Voltage (Note 1) ($V_{BE(sat)}$)	I_C = 500 mA I_B = 50 mA	−0.8	−1.2	V
Pulsed Base Saturation Voltage (Note 1) ($V_{BE(sat)}$)	I_C = 1.0A I_B = 100 mA		−1.6	V
Collector Cutoff Current (I_{CBO})	V_{CB} = −30V I_B = 0		100	nA
Collector Cutoff Current ($I_{CBO(100°C)}$)	V_{CB} = −30V I_B = 0		15	μA
Collector Cutoff Current (I_{CEX})	V_{CB} = −30V V_{EB} = −3.0V		100	nA
Base Cutoff Current (I_{BL})	V_{CB} = −30V V_{EB} = −3.0V		120	nA
Total Control Charge (Figure 3) (Q_T)	I_C = 500 mA I_B = 50 mA		6 0	nC
Turn On Delay Time (Figure 1) (t_d)	I_C = 500 mA I_{B1} = 50 mA		10	ns
Rise Time (Figure 1) (t_r)	I_C = 500 mA I_{B1} = 50 mA		30	ns
Storage Time (Figure 2) (t_s)	I_C = 500 mA I_{B1} = I_{B2} = 50 mA		60	ns
Fall Time (Figure 2) (t_f)	I_C = 500 mA I_{B1} = I_{B2} = 50 mA		30	ns
Output Capacitance (f = 100 kHz) (C_{ob})	I_E = 0 V_{CB} = −10V		25	pF
Input Capacitance (f = 100 kHz) (C_{ib})	I_C = 0 V_{CB} = −0 5V		100	pF
High Frequency Current Gain (f = 100 MHz) (h_{fe})	I_C = 50 mA V_{CE} = 10V	1.75		

Note 1: Pulsed test, PW = 300μs, duty cycle = 1%