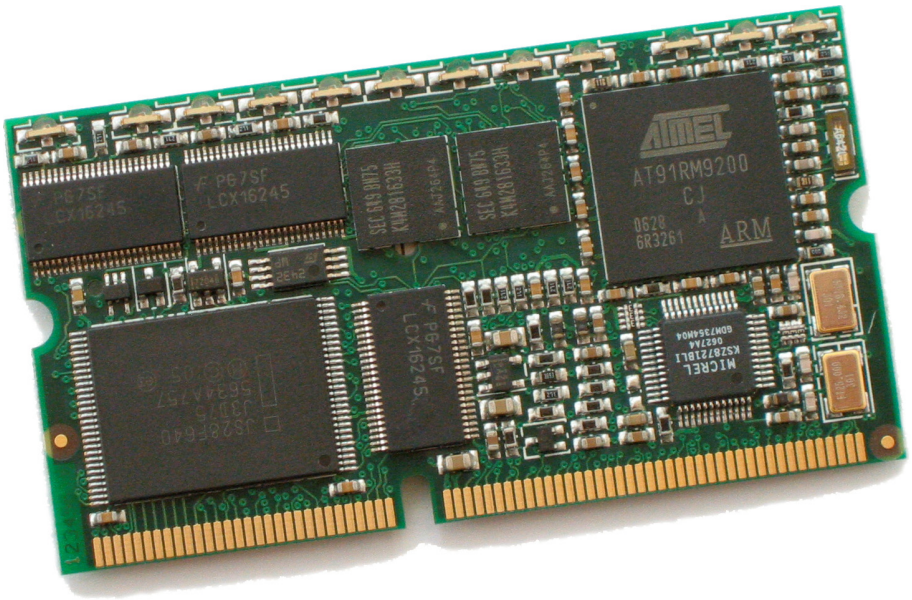

DIMM-RM9200

Hardware Manual

Document Revision V1.06

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4.1 About This Manual

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5 Introduction

5.1 DIMM- RM9200 Architecture

The application-specific portion of a standard embedded application typically requires low pin count components such as relays, power supplies and A/D-converters. An embedded Controller requires components of much higher pin-count and higher density circuit boards. The DIMM- RM9200 concept separates the high-density circuit board of the embedded Controller from the low density, often two-layer, application-specific baseboard.

To address the drawback of a higher price for an embedded controller-like solution, the DIMM-RM9200 performs without discrete peripheral connectors, significantly reducing the cost. In other embedded controller solutions, connectors and their assembly are a significant part of the manufacturing costs. In "low end" solutions, these costs can be as much as 25%. Because the DIMM-RM9200 performs without connectors, these costs are significantly decreased and the controller can be integrated on a smaller board surface. The reduction in the number of steps necessary in manufacturing and assembling the component group is another cost-decreasing factor. The one-sided reflow process, as well as exclusion of the wave-solder process, serves to increase the yield in manufacturing and improve quality.

The required SO-DIMM connector is a very inexpensive, standard component and is available from numerous manufacturers. In designing the DIMM-RM9200, attention was directed toward its use in embedded applications. Because most peripheral interfaces used in such applications are device-internal (in external interfaces, mainly special customized interfaces are used), the serial interface driver components have been excluded from the DIMM-RM9200, leading the interfaces as pure TTL signals to the outside. This further decreases additional costs, while enabling the user to have more flexibility when selecting the interface driver (RS485, RS422, RS232, TTY etc.). The power consumption of the controller architecture is drastically reduced due to the integrated components. This makes the system optimally adaptable with power-saving modes.

The DIMM-RM9200 also has minimized or eliminated some of the most critical disadvantages of the microcontroller:

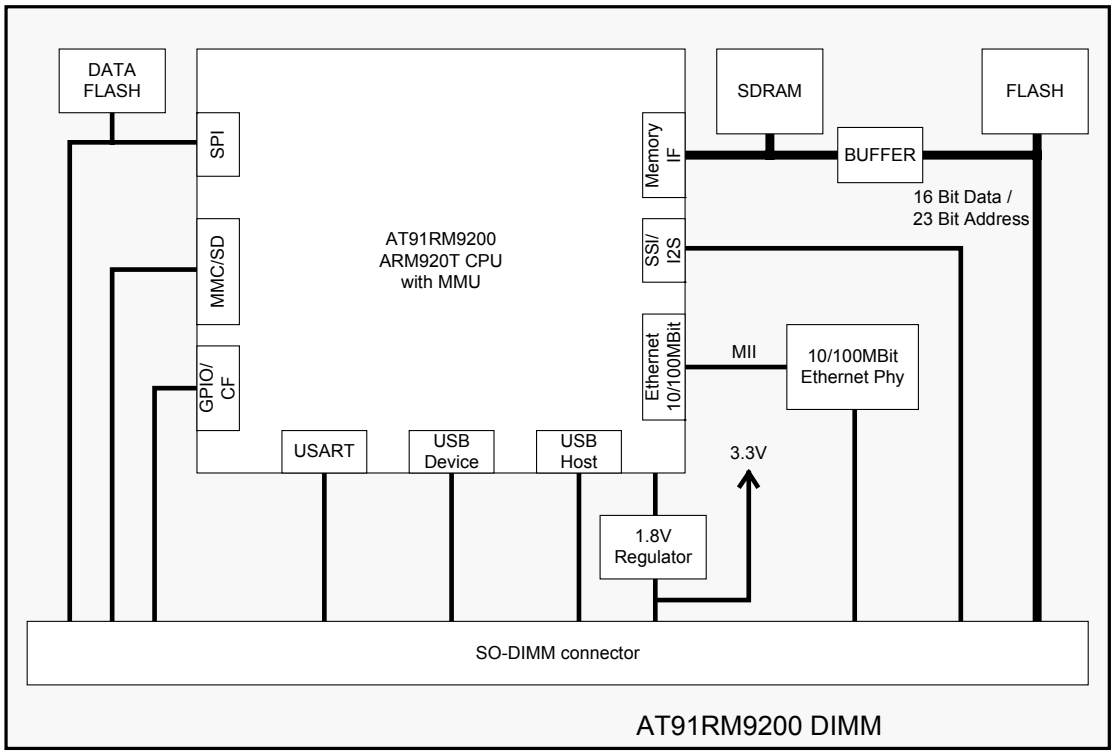
- The DIMM-RM9200 today needs less board surface than most micro-controller applications.
- The embedded controller cost has been drastically decreased by the DIMM-RM9200.
- The DIMM-RM9200 architecture has eliminated the complicated cabling of an embedded PC.

The user receives important advantages by using a DIMM-RM9200. Because of the availability of numerous development platforms, the user can begin the software development immediately on any platform with the AT91RM9200. This is a factor that may influence the success of a product in today's market, where "time to market" is of high importance. As target hardware becomes available, it can be implemented with no obstacles to operation because it will be unnecessary to change the software. With the SO-DIMM-connector, an exchange for other CPU types is possible, increasing the scalability of the ultimate device. In the case of product information and new designs, the CPU may simply be superseded by a new DIMM-module, saving redesign time. Through continuous development of the DIMM modules, the cost for the life span of a product can be reduced, profiting users.

5.2 Feature Summary

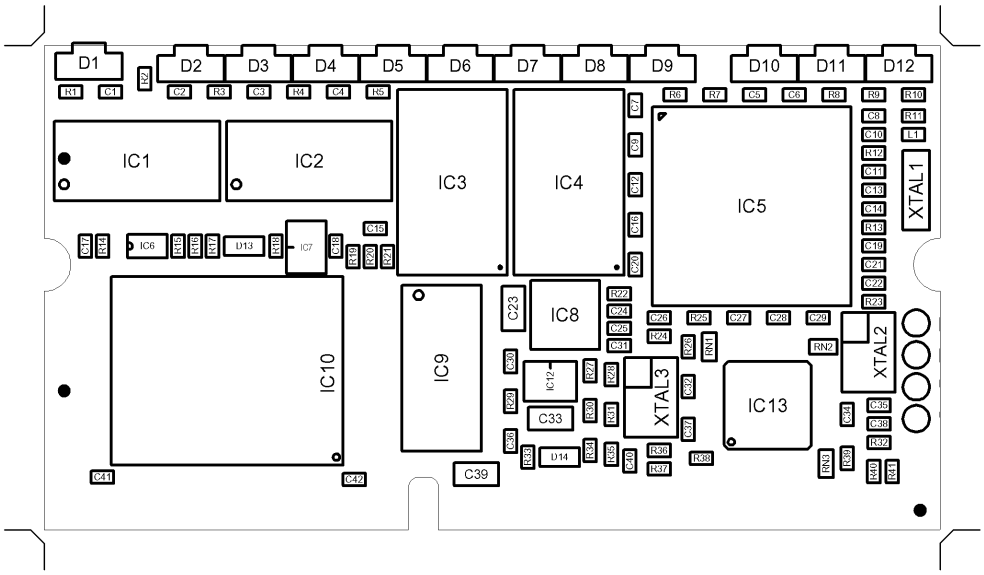
- ATMEL AT91RM9200 microcontroller in BGA package with 190 MHz ARM9 CPU
- UBOOT GPL boot loader
- LINUX operating system / optional WinCE supported
- 32 MB SDRAM memory (optional 64 MB)
- 32-bit SDRAM data bus
- 16 MB Flash memory (optional 32 MB)
- 16-bit Flash data bus
- buffered external 23 bit address / 16 bit data bus
- 10 / 100Mbit Ethernet with on board physical layer and fast MII interface
- 4 serial interfaces
- 2 USB host ports
- 1 USB function port
- optional 2 Mb serial flash for configuration or customer data
- 12 optional LEDs (1 power, 8 user, 3 ethernet) for status display
- on board 1.8V power supply for processor core voltage
- 144-pins SO-DIMM card edge connector
- ultra small size (67.6 mm x 36.5 mm)

5.3 Block Diagram



Picture 1: Module Block Diagram

5.4 Component View



Picture 2: Placeplan

5.5 Functional Description

5.5.1 SO-DIMM connector

All external connections are accessible through the 144-pins SO-DIMM card edge connector. The following external functionality is available:

- 3V3 power supply input
- 1V8 power supply output (max. 50mW)
- buffered address bus with address lines A0 through A22
- buffered data bus with data lines D0 through D15
- buffered read/write strobes and byte select signals
- unbuffered chip selects nCS2 through nCS7
- reset_out, reset_in and interrupts
- serial interfaces
- timer inputs and outputs
- 1 USB host and 2 USB device interfaces
- JTAG interface and dbg_USART, used during production
- 10/100Mbit Ethernet signals

The internal circuitry of the DIMM-RM9200 is based on 3V3 low voltage technology, but the address and data bus SO-DIMM signals are 5 V tolerant. Therefore you can use both 3V3 and 5 V components to interface to the SO-DIMM connector. All other interface signals are 3V3 only.

5.5.2 Power supply

5.5.2.1 External power supply

The DIMM-RM9200 requires an external power supply. You have to power the DIMM-RM9200 with a 3V3 / 0,5 A external power supply, connected to the 3V3 pins on the SO-DIMM connector. When using an external power supply, it is strongly advised to place a low ESR capacitor on the carrier board close to the 3V3 input to reduce interference.

5.5.2.2 On board power supply

The core supply voltage for the AT91RM9200 is generated on board and is available for reference on the 1V8 pin of the SO-DIMM connector. The power consumption of external components, if any, must be limited to 50mW.

5.5.3 Memory Layout

Equipped with either 64Mbit, 128 Mbit or 256 Mbit Intel Strata Flash as well as with two SDRAMs of each 128 Mbit or 256 Mbit the DIMM-RM9200 realizes a total of 8, 16 or 32 Mbyte Flash and 32 or 64 Mbyte SDRAM. Standard variants are 8MByte / 32 MByte Flash / SDRAM respectively 32 / 64 MByte Flash / SDRAM. Using A25 for the chip-internally not bonded A24 address line it is possible to address 32 MByte of Flash-Memory (for the missing A24 problem please take a look in the errata for the ATMEL AT91RM9200).

5.5.3.1 Flash (chip select NCS0)

The flash memory is accessed 16 bits wide with NCS0. The resulting address range for the two standard options are:

16 MByte:	0x1000 0000 - 0x10FF FFFF		(JL28F128J3A)
32 MByte:	0x1000 0000 - 0x10FF FFFF	1.segment (16 Mbyte)	(JL28F256J3C/PF48F4000P0Z)
	0x1100 0000 - 0x11FF FFFF	mirror of 1. segment (16 Mbyte)	
	0x1200 0000 - 0x12FF FFFF	2. segment (16 Mbyte)	

The gap in the flash memory area for the 32MByte device can be avoided by addressing the flash starting at offset 0x1100 0000. This results in the following memory layout:

32 MByte:	0x1100 0000 - 0x11FF FFFF	1.segment (16 Mbyte)	(JL28F256J3C/PF48F4000P0Z)
	0x1200 0000 - 0x12FF FFFF	2. segment (16 Mbyte)	

5.5.3.2 SDRAM (chip select NCS1)

The SDRAM is accessed with 32 bit data bus width at NCS1. This results in the following address range for the standard memory options:

32 MByte:	0x2000 0000 - 0x21FF FFFF	(MT48LC8M16A2)
64 MByte:	0x2000 0000 - 0x23FF FFFF	(MT48LC16M16A2)

5.5.3.3 Serial data flash (chip select NPCS0)

An optional serial data flash of type AT25DB021B will be accessed using the SPI chip select NPCS0. The data flash can be used for storage of configuration data or a bootloader. Booting U-Boot with TFTP feature from the data flash in a network environment, the Strata Flash can be omitted further reducing the system costs.

5.5.3.4 Address / data bus buffer

All chip selects but NCS1 (SDRAM) activate the on-board data-bus buffers. Activity on the external data bus interface thus is reduced to a minimum. The address bus buffers are always activated, allowing for further external logic with fast timing. The buffers are 5V tolerant 3.3V devices (74LCX16245) allowing the connection of either 3.3V or 5V external devices. In addition to the address lines A0..A22 and data lines D0..D15, the signals common to multiple external devices (NOE, NWE, BS1 and BS3) are buffered. The chip select signals NCS2..NCS7 are not buffered.

5.5.3.5 Special notes for watchdog usage

As the DIMM-RM9200 uses Intel StrataFlash for Program storage and as boot device, special care has to be taken, when using the Flash as filesystem storage device (e.g. as JFFS2-Image Source under Linux). The Intel Flashes can be switched into 'Read Status' mode in order to get the status of the chip, e.g. after writing a sector. This command can be disabled by software command 'Read Array' command, or by hardware reset. A problem can arise, if a watchdog reset occurs, while the flash is in 'Read Status' mode. The processor resets and tries to fetch the first instruction from flash. As the flash remains in 'Read Status' command (the watchdog reset is only internal to the AT91RM9200 chip), the program fetch will fail and the system will stall.
In order to circumvent this behavior there is a patch available for the linux kernel, which uses the watchdog interrupt to reset the flash into 'Read Array' mode before asserting a watchdog reset.
However, this is not 100% secure. If you need 100% security, you have to use an external watchdog circuitry.

5.5.4 Ethernet Phy

A Micrel KS8721 or Micrel KS8001 is used as physical layer chip. This low-power transceiver for 10/100BASE-TX performs auto negotiation compliant with IEEE 802.3u and auto crossover function. It is specified for the industrial temperature range. The whole Ethernet interface is formed with the fast Media Independent Interface (MII) and the Media Access Control Layer (MAC) of the Atmel AT91RM9200 combined with the Micrel PHY supplemented through an external RJ45-Modular Jack with integrated inductance. A symmetrical kind of Modular Jack is needed for auto MDIX functionality. A good choice for a transformer is 'PH163539' from YCL. 'J0024D21' from Pulse can be used as ethernet connector with integrated transformer.

6 DIMM-RM9200 Module Pinout

Pin	Interface	Signal	Dir
1	Power	GND	
3	Data	D15	I/O
5	Data	D14	I/O
7	Data	D13	I/O
9	Data	D12	I/O
11	Data	D11	I/O
13	Data	D10	I/O
15	Data	D9	I/O
17	Data	D8	I/O
19	Address	A21	OUT
21	Address	A20	OUT
23	Address	A19	OUT
25	Address	A18	OUT
27	Address	A17	OUT
29	Address	A16	OUT
31	Address	A15	OUT
33	Address	A14	OUT
35	Address	A13	OUT
37	Address	A12	OUT
39	Address	A11	OUT
41	Address	A10	OUT
43	Control	NOE	OUT
45	Control	NWE	OUT
47	Control	nCS2	OUT
49	Control;I/O	PC10/nCS4/CFCS	I/O
51	Control;I/O	PC12/nCS6/CFCE2	I/O
53	Control;I/O	PC6/NWAIT	I/O
55	Control;I/O	PB28/FIQ	I/O
57	Control;I/O	PA26/TWCK/IRQ1	I/O
59	Control	NBOOTMODE	I/O
61	Power	GND	
63	Power	3V3	
65	SPI;I/O	PA3/nPCS0/IRQ5	I/O
67	SPI	PA1/MOSI/PCK0	I/O
69	SPI	PA2/SPCK/IRQ4	I/O
71	SPI	PA0/MISO/PCK3	I/O
73	JTAG	TCK	IN
75	USART1	PB24/nUSART1_CTS	I/O
77	USART0	PD21/nUSART0_RTS	I/O
79	SPI;I/O	PD18/nPCS1	I/O
81	Timer;I/O	PB13/TK2	I/O
83	Timer;I/O	PB27/PCK0	I/O
85	Timer;I/O	PB2/TD0/SCK3	I/O

Pin	Interface	Signal	Dir
2	Power	GND	
4	Power	3V3	
6	Data	D7	I/O
8	Data	D6	I/O
10	Data	D5	I/O
12	Data	D4	I/O
14	Data	D3	I/O
16	Data	D2	I/O
18	Data	D1	I/O
20	Data	D0	I/O
22	Address	A9	OUT
24	Address	A8	OUT
26	Address	A7	OUT
28	Address	A6	OUT
30	Address	A5	OUT
32	Address	A4	OUT
34	Address	A3	OUT
36	Address	A2	OUT
38	Address	A1	OUT
40	Address	A0	OUT
42	Control	NRESET	OUT
44	Control	nBS1	OUT
46	Control	nBS3	OUT
48	Control;I/O	nCS3/SMCS	I/O
50	Control;I/O	PC11/nCS5/CFCE1	I/O
52	Control;I/O	PC13/nCS7	I/O
54	Control;I/O	PB29/IRQ0	I/O
56	Control;I/O	PA25/TWD/IRQ2	I/O
58	Control	nRESET_IN	IN
60	Power	GND	
62	Power	GND	
64	Power	3V3	
66	Power	3V3	
68	USART1	PB20/USART1_TXD	I/O
70	JTAG	TDI	IN
72	USART1	PB21/USART1_RXD	I/O
74	JTAG	TDO	OUT
76	JTAG	TMS	IN
78	USART1	PB22/USART1_SCLK	I/O
80	JTAG	NTRST	IN
82	USART1	PB25/nUSART1_DSR	I/O
84	SPI;I/O	PD19/nPCS2	I/O
86	USART1	PB23/nUSART1_DCD	I/O

Pin	Interface	Signal	Dir
87	Timer;I/O	PB14/TD2	I/O
89	USB	HDPB	I/O
91	USB	HDMB	I/O
93	USB	HDPA	I/O
95	USB	HDMA	I/O
97	USB	DDP	I/O
99	USB	DDM	I/O
101	Timer;I/O	PB12/TF2	I/O
103	Timer;I/O	PB6/TF1/TIOA3	I/O
105	Timer;I/O	PB8/TD1/TIOA4	I/O
107	MMC;I/O	PB5/RF0/MCDA3	I/O
109	MMC;I/O	PA29/MCDA0	I/O
111	MMC;I/O	PA28/MCCDA	I/O
113	I/O	PC5/BFWE	I/O
115	I/O	PC1/BFRDY/SMOE	I/O
117	I/O	PC3/BFBAA/SMWE	I/O
119	Timer;I/O	PA4/PCK1/IRQ5	I/O
121	MMC;I/O	PA9/MCDB0	I/O
123	USART3	PA5/USART3_TXD	I/O
125	Timer;I/O	PA21/TIOA2	I/O
127	MMC;I/O	PA8/MCCDB	I/O
129	Power	GND	
131	USART0; Timer;I/O	PA19/USART0_SCK/ TIOA1	I/O
133	USART2	PA23/USART2_IRDA _TXD	I/O
135	USART0	PA20/nUSART0_CTS	I/O
137	DBG_USART	PA31/DBG_TXD	I/O
139	Power	AVDDR/ETH_CT/RD	
141	Ethernet	ETH_RX+	IN
143	Ethernet	ETH_RX-	IN

Pin	Interface	Signal	Dir
88	USART2	PD23/nUSART2_RTS	I/O
90	Timer;I/O	PB9/RD1/TIOB4	I/O
92	USART1	PD25/nUSART1_DTR	I/O
94	SPI;I/O	PD20/nPCS3	I/O
96	Timer;I/O	PB10/RK1/TIOA5	I/O
98	USART1	PD22/nUSART1_RTS	I/O
100	USART3	PD24/nUSART3_RTS	I/O
102	MMC;I/O	PB4/RK0/MCDA2	I/O
104	Timer;I/O	PB11/RF1/TIOB5	I/O
106	Timer;I/O	PB7/TK1/TIOB3	I/O
108	MMC;I/O	PB3/RD0/MCDA1	I/O
110	DBG_USART	PA30/DBG_RXD	I/O
112	MMC;I/O	PA27/MCCK	I/O
114	I/O	PC4/BFOE	I/O
116	I/O	PC2/BFAVD	I/O
118	I/O	PC0/BFCK	I/O
120	USART2	PA22/USART2_IRDA _RXD	I/O
122	Power	1V8	
124	USART3	PA6/USART3_RXD	I/O
126	I/O	PA10	I/O
128	USART0	PA17/USART0_TXD	I/O
130	USART0	PA18/USART0_RXD	I/O
132	USART2;I/O	PA24/SCK2	I/O
134	Power	3V3	
136	Timer;I/O	PB0/TF0	I/O
138	Timer;I/O	PB1/TK0	I/O
140	Power	AVDDT/ETH_CT/TD	
142	Ethernet	ETH_TX+	OUT
144	Ethernet	ETH_TX-	OUT

Table 1: Module Pinout

7 DIMM-RM9200 Peripherals Pinout

Following section describes the pinout of the peripheral groups of the AT91RM9200 controller available on the DIMM-RM9200.

7.1 USART0

Signal	DIMM-Pin	PIO Controller	Port Pin
TXD	128	PIO A / Peripheral A	PA17
RXD	130	PIO A / Peripheral A	PA18
SCLK	131	PIO B / Peripheral A	PA19
nCTS	135	PIO A / Peripheral A	PA20
nRTS	77	PIO D / Peripheral A	PD21

Table 2: USART0 Port Pinout

7.2 USART1

Signal	DIMM-Pin	PIO Controller	Port Pin
TXD	68	PIO B / Peripheral A	PB20
RXD	72	PIO B / Peripheral A	PB21
SCLK	78	PIO B / Peripheral A	PB22
nDCD	86	PIO B / Peripheral A	PB23
nCTS	75	PIO B / Peripheral A	PB24
nDSR	82	PIO B / Peripheral A	PB25
nRTS	98	PIO D / Peripheral A	PD22
nDTR	92	PIO D / Peripheral A	PD25

Table 3: USART1 Port Pinout

7.3 USART2

Signal	DIMM-Pin	PIO Controller	Port Pin
TXD	133	PIO A / Peripheral A	PA23
RXD	120	PIO A / Peripheral A	PA22
SCLK	132	PIO A / Peripheral A	PA24
nCTS	110	PIO A / Peripheral A	PA30
nRTS	88	PIO D / Peripheral A	PD13

Table 4: USART2 Port Pinout

The nCTS-Pin for USART2 is only available on PA30, which also is the DRXD-Pin of the debug UART.

7.4 USART3

Signal	DIMM-Pin	PIO Controller	Port Pin
TXD	123	PIO A / Peripheral B	PA5
RXD	124	PIO A / Peripheral B	PA6
SCLK	85	PIO B / Peripheral B	PB2
nCTS	138	PIO B / Peripheral B	PB1
nRTS	100	PIO D / Peripheral A	PD24
	136	PIO B / Peripheral B	PB0

Table 5: USART3 Port Pinout

The Pins SCLK, nCTS and nRTS on PIO B for USART3 share their pins with Pins TF0, TK0 and TD0 of SSC0. If you want to use USART3 with full hardware handshake you can't use SSC0 transmit functionality. If you want to use USART3 for RS485, you should use nRTS on PIO D / PD24 for direction switching.

7.5 SPI

Signal	DIMM-Pin	PIO Controller	Port Pin
NPCS0	65	PIO A / Peripheral A	PA3
NPCS1	79	PIO D / Peripheral A	PD18
NPCS2	84	PIO D / Peripheral A	PD19
NPCS3	94	PIO D / Peripheral A	PD20
MISO	71	PIO A / Peripheral A	PA0
MOSI	67	PIO A / Peripheral A	PA1
SPCK	69	PIO A / Peripheral A	PA2

Table 6: SPI Port Pinout

If the optional SD-Card socket on the DIMM-RM9200 is populated, NPCS1 is used for this card socket and therefore can not be used for external peripherals.

7.6 MCI

Signal	DIMM-Pin	PIO Controller	Port Pin
MCCK	112	PIO A / Peripheral A	PA27
MCCDA	111	PIO A / Peripheral A	PA28
MCDA0	109	PIO A / Peripheral A	PA29
MCDA1	108	PIO B / Peripheral B	PB3
MCDA2	102	PIO B / Peripheral B	PB4
MCDA3	107	PIO B / Peripheral B	PB5
MCCDB	127	PIO A / Peripheral B	PA8
MCDB0	121	PIO A / Peripheral B	PA9

Table 7: MCI Port Pinout

Slot A support both MMC and SD Cards while Slot B only supports MMC Cards. If using Slot A for SD-Cards you can't use SSC0 receive functionality, as the signals MCDA1-3 share their pins with RD0, RK0 and RF0.

7.7 TWI

Signal	DIMM-Pin	PIO Controller	Port Pin
TWD	56	PIO A / Peripheral A	PA25
TWCK	57	PIO A / Peripheral A	PA26

Table 8: TWI Port Pinout

7.8 SSC0

Signal	DIMM-Pin	PIO Controller	Port Pin
TF0	136	PIO B / Peripheral A	PB0
TK0	138	PIO B / Peripheral A	PB1
TD0	85	PIO B / Peripheral A	PB2
RD0	108	PIO B / Peripheral A	PB3
RK0	102	PIO B / Peripheral A	PB4
RF0	107	PIO B / Peripheral A	PB5

Table 9: SSC0 Port Pinout

SSC0 shares it's pins with USART3 (transmit functionality) and MCI (receive functionality). If you want to use SSC0, you can't use hardware handshake / synchronous transfer on USART3 and SD-Card interface using 4 data lines.

7.9 SSC1

Signal	DIMM-Pin	PIO Controller	Port Pin
TF1	103	PIO B / Peripheral A	PB6
TK1	106	PIO B / Peripheral A	PB7
TD1	105	PIO B / Peripheral A	PB8
RD1	90	PIO B / Peripheral A	PB9
RK1	96	PIO B / Peripheral A	PB10
RF1	104	PIO B / Peripheral A	PB11

Table 10: SSC1 Port Pinout

8 Signal Description

The SO-DIMM connector provides the signals for the embedded peripheral components of the AT91RM9200 as well as address / data lines and chip selects for connection of external peripheral components like USARTs, CAN interfaces or a LCD controller. If not mentioned, the signals are directly connected to the processor. For a description of the processor pin functionality please take a look at the AT91RM9200 user's manual.

Caution:

- The processor is a 3.3V device. Input voltages above 3.6V may cause permanent damage to the processor.
  Only the address / data bus signals and some control signals are 5V tolerant!

Following sections describe only the pins which are not directly connected to the processor.

8.1 Address / Data Bus

From the processors address and data bus the address lines A0..A22 and data lines D0..D15 are available at the SO-DIMM connector via 5V tolerant bus buffers of type 74LVX16245. The address bus signals are always active, while the data bus signals are active only when SDRAM is inactive.

8.2 Control Signals

8.2.1 nRESET

The signal nRESET is the reset output of the on-board supervisory circuit. It will be activated (active low) whenever the supply voltage drops below 2.94V or the core voltage drops below 1.75V. Additionally it can be forced active by setting the signal nRESET_IN low.

8.2.2 nOE

The signal nOE is the buffered nOE signal from the processor. It is active low for read accesses to the external memory interface. For further information concerning this signal please consult the AT91RM9200 user's manual / data sheet.

8.2.3 nWE

The signal nWE is the buffered nWE signal from the processor. It is active low for write accesses to the external memory interface. For further information please consult the AT91RM9200 user's manual / data sheet.

8.2.4 NBS1/nBS3

The signals nBS1/nBS3 are the buffered nBS1/nBS3 signal from the processor. They serve as ior / iow signals for compact flash devices. Further information can be found in the AT91RM9200 user's manual / data sheet.

8.2.5 nRESET_IN

The signal nRESET_IN is an external reset input to the on-board supervisory circuit. An active low signal on this pin asserts a hardware reset by activating the on-board reset signal. The signal has an on-board 33k pullup and can be driven with an open collector/open drain or push/pull driver.

8.2.6 nBOOTMODE

The signal nBOOTMODE is connected to the BMS signal of the processor. When set high the on chip boot mode is selected and the processor starts execution from internal ROM. When set to low the code at 0x10000000 (external memory area 0) is executed. The external memory area 0 selects the onboard parallel flash. For further information please consult the AT91RM9200 user's manual.

8.3 Peripherals

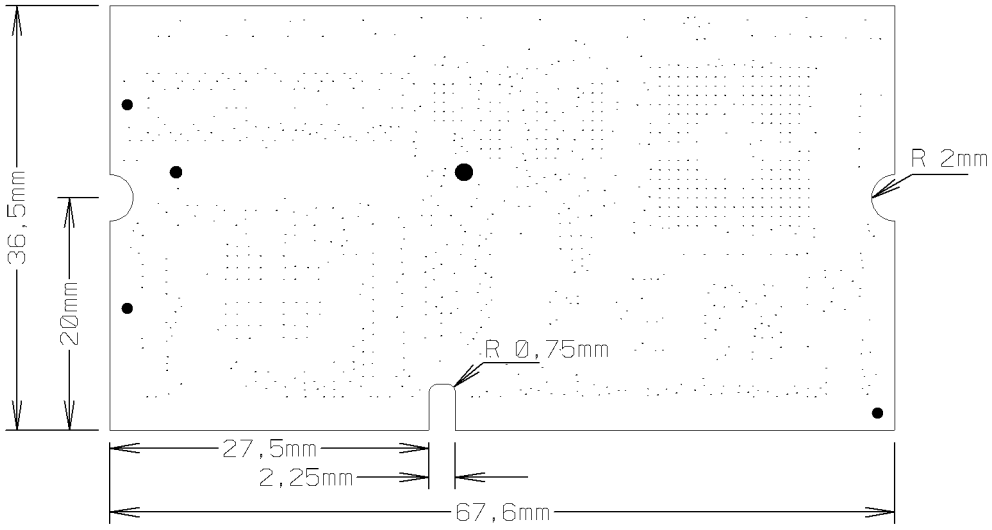
8.3.1 Ethernet

The ethernet interface uses a Micrel KS8721 or Micrel KS8001 physical layer chip for interfacing to the RJ45 connector. The termination network for the RX-signals is already placed on the DIMM-RM9200. The series resistors for the TX-signals have to be placed on the carrier board.
The RX signals are available at pins 141 (ETH_RX+) and 143 (ETH-RX-).
The TX signals are available at pins 142 (ETH_TX+) and 144 (ETH-TX-).
Due to the size of the recomended components, the decoupling of the analog supply pins AVVDR and AVVDT needs additional external components for good ripple rejection. 10µF ceramic or tantalum capacitors should be mounted as close as possible to the SO-DIMM connector pins 139 (AVDDR) and 140 (AVDDT).

All other peripheral pins are directly connected to the corresponding pin of the processor.

9 Mechanical Dimensions

9.1 DIMM-RM9200 Module



Picture 3: Module Dimensions

9.2 DIMM Connector

The DIMM-RM9200 uses standard SO-DIMM memory sockets for connection to the carrier board. 3.3V as well as 5V keying can be used for the SO-DIMM sockets, as the DIMM-RM9200 features a wide key for both keying types.

Caution:

- The pinout of the DIMM-RM9200 SO-DIMM connector is NOT compatible with memory sockets.
  Insertion into a socket with wrong pinout may damage the DIMM-RM9200 and the carrier board!

Following table is a short list of possible DIMM connectors which can be used with the DIMM-RM9200. Most connectors are right angled connectors with varying height.

Manufacturer	Order Code	Description
JST	DM-3B1-N1210	Horizontal mounted, SMD, extremely small space
JAE	MM30-144A series	Vertical mounted, through hole, different lever / keying types
JAE	MM30-144 series	Horizontal mounted, SMD, different mounted heights

Table 11: DIMM Socket Selection

10 Installing the DIMM-RM9200

10.1 Installing the module

Caution:

- Always wear a grounded wrist strap when handling the DIMM-RM9200 in order to discharge any static electricity from your body!
- Always unplug your system from power before installing the DIMM-RM9200.

The DIMM-RM9200 does not require any configurations before installation. Perform the following step-by-step instructions to install the DIMM-RM9200 in your system:

- **Unplug your system from the power outlet.**
- Insert the DIMM-RM9200 into the SO-DIMM connector on the carrier board. The module should drop easily into place. Do not force the module into the socket to avoid damage to the socket. If the module does not fit check its alignment. You also may pull the two plastic locking clips gently sideways away form the socket during insertion before the module is locked into the socket.
- Reconnect your system to the power outlet. The DIMM is now ready to use.

11 Technical Specifications

Microcontroller

CPU type:	ATMEl AT91RM9200 ARM920T microcontroller
CPU speed:	180 MHz

Memory

SDRAM:	32 MByte, optional 64 MByte, 32-bit data bus
Program-Flash:	16 MByte, optional 32 MByte, 16-bit data bus
Data-Flash:	2 MBit SPI Dataflash (onlyon Revision 1.1 boards)
SD-Card:	optional Socket on bottom side (vertical mounting)

Interfaces

SDRAM:	32 MByte, optional 64 MByte, 32-bit data bus

External Bus Interface

23Bit buffered address bus
16Bit buffered data bus
5V tolerant bus buffers

External power supply (standard)

Input:	3.3 V ± 5 %, 300 mA max.
Input connection:	SO-DIMM bus pins 3V3 and GND

On board power supply

Type:	Low drop out linear voltage regulator
Output:	1.8 V, 50 mA max.
Output connection:	SO-DIMM bus pin 1V8

General information

Connector:	SO-DIMM card edge, 144 pins
Power consumption:	3.3 V, 220 mA typical
PCB type:	8 layer lead free SO-DIMM module
Operating temperature:	-25 °C to +85 °C
Storage temperature:	-25 °C to +85 °C
Humidity:	10 - 90 %, non condensing
Dimensions (h x w):	37 x 67 mm
Weight:	30 g

12 Important Documents

12.1 Atmel AT91RM9200 Datasheet

Literatur Number: 1768D.pdf
Revision History: D
Publication Date: 11-Jul-05
www.atmel.com

12.2 Atmel AT91RM9200 Errata Sheet

Literatur Number: 6015G.pdf
Revision History: G
Publication Date: 11-Jul-05
www.atmel.com

12.3 Micrel KS8721BL/SL Datasheet

Version: KS8721BL/SL Rev. 1.1
Publication Date: May 17, 2004
www.micrel.com

12.4 Micrel KS8001L/S Datasheet

Version: KS8001L/L Rev. 1.03
Publication Date: March 7, 2006
www.micrel.com

12.5 Intel Embedded Flash Memory (J3 v. D) Datasheet

Version: 308551-003
Publication Date: February 2006
www.intel.com

12.6 Intel StrataFlash Embedded Memory (P30) Family Datasheet

Version: 306666-007
Publication Date: May 1, 2006
www.intel.com

13 Hardware Revision History

Version	Date	Alteration
1.1	26.10.05	1st Official Release
1.2	11.10.06	Changed Ethernet Phy from Davicom DM9161A (consumer temperature range) to Micrel KS8721 (industrial temperature range) Removed discontinued AT45DB021 data flash Added TWI-EEROM for manufacturer information
1.3	22.06.07	Changed SPI-CS signal for onboard SPI-driven SD-Card socket from nPCS0 to nPCS1

14 Document Revision History

Version	Date	Alteration
0.9	15.03.05	Initial Draft
0.91	05.09.05	Connector pinout changes Added pin descriptions
1.00	19.10.05	Added signal direction in connector pinout Added DIMM-Socket table
1.01	27.10.05	Added peripheral groups pinout
1.02	28.07.06	Corrected Pinout descritive text Added USART3 nRTS pinout comments Added installation information
1.03	03.07.07	Corrected pinout descriptive text for PB23 / PB24 in Table 7.2
1.04	25.07.07	Added Hardware Revision History
1.05	27.07.07	Changed ethernet PHY description to Micrel KS8721 / KS8001 Added Micel datasheet info Removed Davicom datasheet info Added note in chapter 7.5 about nPCS1 used for optional SD-Card socket
1.06	09.07.08	Added Intel datasheet info Added Watchdog notes in chapter 5.5.3.5 Added open source software legal notice in chapter 4.4