SPECIFICATION

1. DESCRIPTION

DK5V150R25ST1 is a simple design and high efficiency synchronous rectifying IC. It is of TO-220F package with only A and K poles, it can directly replace the SBD rectifying diode with P and N poles.

With 150V NMOS integrated, it can greatly decrease the conduction loss, so that working efficiency of application increases.

2. APPLICATIONS

· USB chargers
· LED drivers
· Flyback power adapters
· Flyback power converter

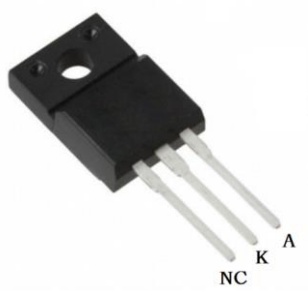
3. MAIN FEATURES

· Suitable for PSR or SSR IC application
· Ultra high efficiency and low temperature
· Ultra low V_F
· Improves EMC/EMI characteristics
· Works under CCM, DCM and QR mode in flyback system
· Internal integrated 25mΩ /150V NMOS
· Self-power supply design, no external power supply needed
· Self-detection, no need for external synchronous signal
· Only 2 poles (A-K), can directly replace Schottky Barrier Diode, no need for external components

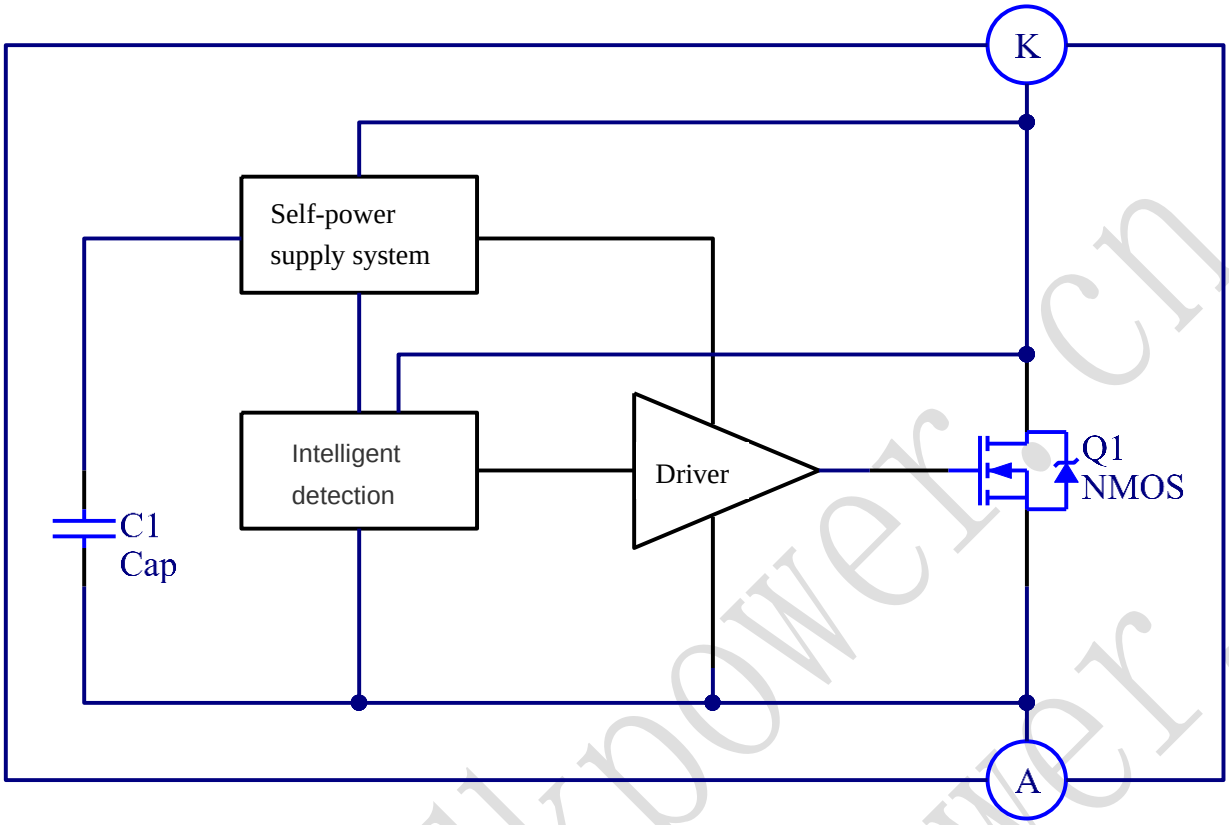
4. CONNECTION DIAGRAM (T0-220F)

PIN FUNCTION:

Pin Name	Function
NC	Floated
K	Same as diode cathode in application
A	Same as diode anode in application



5. FUNCTIONAL STRUCTURE (block diagram)



6. ABSOLUTE MAXIMUM RATINGS

Note: Stresses exceeding the absolute maximum rating may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are the stresses ratings only. Values are at TA=25℃ unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit
NMOS Drain-source Breakdown Voltage	$V_{(BR)DSS}$	150			V
NMOS MAX. Average current	I_{DCDC}		33		A
NMOS Peak current	I_{DSPDC}				A
TO220 Dissipation Power	P_{DMAX}				W
Thermal Resistance (Junction-to-Ambient)	$R\theta_{JA}$		62.5		℃/W
Thermal Resistance (Junction-to-Case)	$R\theta_{JC}$		3.8		℃/W
Operating temperature	T_J			120	℃
Storage temperature	T_{STG}	-55		155	℃
Operating Junction Temperature	T_J	-40		150	℃
Lead soldering temperature			260/5S		℃

7. ELECTRICAL CHARACTERISTIC

Values are at TA =25℃ unless otherwise noted

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
Power voltage						
MOSFET Turn-on Voltage①	V_{CC_ON}			7.2		V
Under-voltage threshold①	V_{CC_OFF}			3.3		V
Over-voltage threshold①	V_{OVP}			10		V
Intelligent detection & control						
NMOS Turn-on Voltage	V_{ON}	K point as reference		-220		mV
NMOS Turn-on Delay	T_{DON}				150	ns
NMOS Turn-off Delay	T_{DOFF}				50	ns
NMOS MAX.Turn-on time	T_{ON_MAX}			20		μs
NMOS MIN. Turn-on time	T_{ON_MIN}			200		ns
NMOS MIN. Off time	T_{OFF_MIN}			500		ns
Dead time②	T_D			400		ns
MAX. working frequency	F_{S_MAX}				150	KHz
NMOS						
NMOS Turn-on Resistance	R_{DS_ON}				25	mΩ

Remark: ① All voltage in data sheet take A point as reference.
② SR IC adjust dead time according to K point fluctuation.

8. OPERATION PRINCIPLE

8.1 Start Up

When K pole voltage is higher than A pole, self-power supply circuit will support the power of VCC, VCC voltage increases. If VCC voltage is lower than start up voltage VCC_ON, internal MOS is off. When VCC voltage is higher than VCC_ON, control circuit inside IC begins to work, start up mode finished. When VCC voltage is lower than VCC_OFF, IC returns to start up mode again.

8.2 Power NMOS control

If the detected voltage of forward rectification between A and K is higher than V_{ON}, MOS opens. And K point voltage is being detected, system's working mode would be judge as per its changes. In CCM mode, If the turn on time reach T_{ON} NMOS close. In non CCM working mode, if detected current through MOS is decreasing and reaches 0, NMOS close.

8.3 RC absorbing circuit

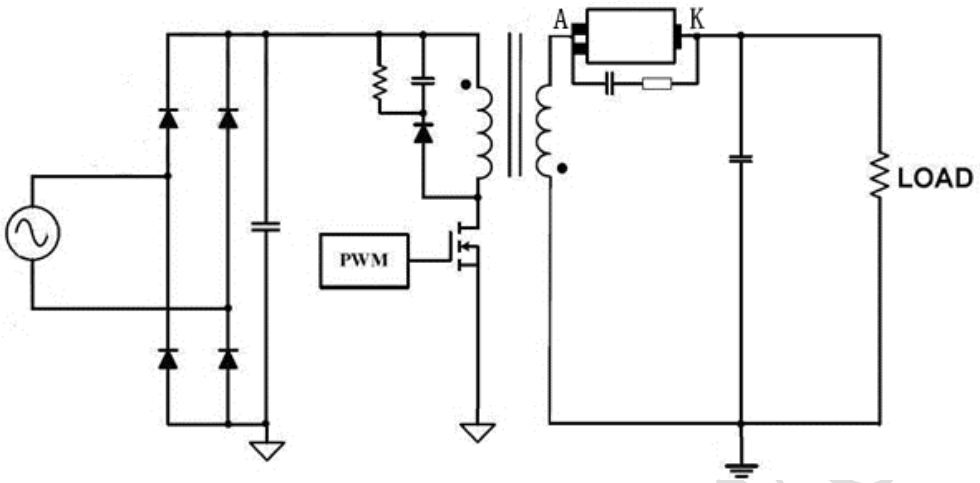
In status of starting up, output short circuit, over input voltage and CCM modes, there will be peak voltage, as to avoid the breaking of NMOS, can add RC absorbing circuit between A and K, so that the peak voltage on K can be reduced.

8.4 NMOS Turn-on Resistance

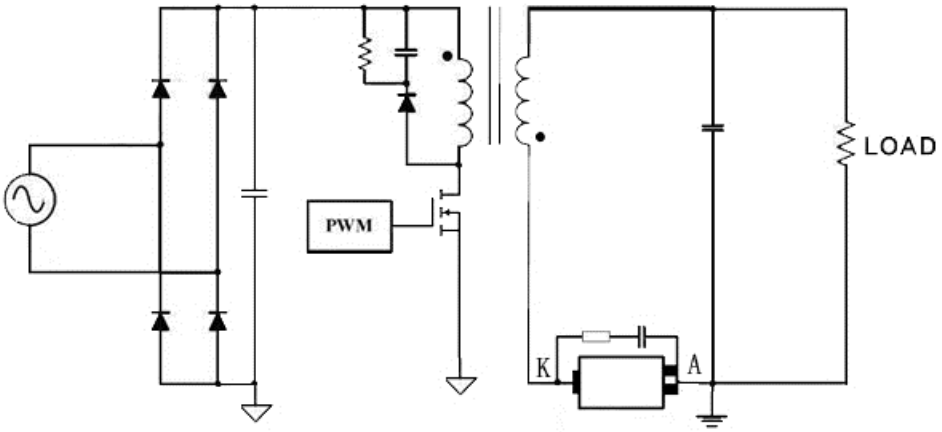
During operation, internal resistance increases together with the temperature, efficiency decreases accordingly. It is better to enlarge the heat releasing area so that the IC temperature can be decreased.

9. TYPICAL APPLICATION

Forward rectification:



Reverse rectification:

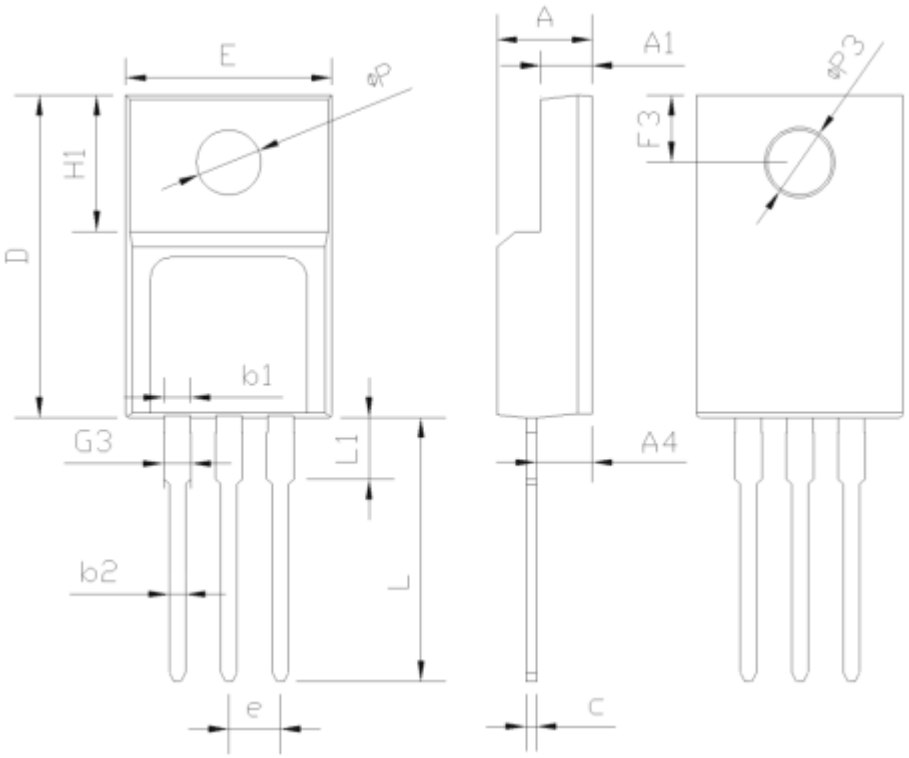


10. SPECIAL NOTICE FOR PBC LAYOUT DESIGN

10. 1 Must take care and make sure the working voltage of the IC is lower than NMOS's breakdown voltage.

10. 2 Take care of the IC temperature in use, to make sure that the working temperature is not higher than its Operating Junction Temperature.

11. MECHANICAL AND PACKING INFORMATION



SYMBOL	mm		
	MIN	NOM	MAX
E	9.96	10.16	10.36
A	4.50	4.70	4.90
A1	2.34	2.54	2.74
A4	2.56	2.76	2.96
c	0.40	0.50	0.65
D	15.57	15.87	16.17
H1		6.70REF	
e		2.54BSC	
L	12.68	12.98	13.28
L1	2.88	3.03	3.18
ΦP	3.03	3.18	3.38
ΦP3	3.15	3.45	3.65
F3	3.15	3.30	3.45
G3	1.25	1.35	1.55
b1	1.18	1.28	1.43
b2	0.70	0.80	0.95

Caution: This product is a static sensitive component, please pay a attention to protect! The scope of ESD damage can be extended from minor performance to equipment failure. Precision IC may be damaged, which may result in component parameters not meeting the published specifications.

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