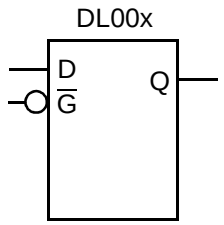
AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

DL00x is a family of transparent, unbuffered D latch with active low gate transparency and without SET or RESET.

Logic Symbol



Truth Table

GN	D	Q
L	L	L
L	H	H
H	X	NC

NC = No Change

HDL Syntax

Verilog ..... DL00x *inst_name* (Q, D, GN);

VHDL..... *inst_name*: DL00x port map (Q, D, GN);

Pin Loading

Pin Name	Equivalent Loads	
	DL001	DL002
D	1.0	1.0
GN	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DL001	4.0	TBD	6.8
DL002	4.0	TBD	8.6

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
DL001	From: D To: Q	t_{PLH} t_{PHL}	0.36 0.44	0.46 0.56	0.58 0.69	0.73 0.85	0.85 0.97
	From: GN To: Q	t_{PLH} t_{PHL}	0.46 0.63	0.55 0.76	0.67 0.89	0.83 1.03	0.96 1.14
	Number of Equivalent Loads		**1**	**8**	**15**	**22**	**30 (max)**
DL002	From: D To: Q	t_{PLH} t_{PHL}	0.39 0.48	0.51 0.64	0.62 0.77	0.71 0.88	0.81 1.00
	From: GN To: Q	t_{PLH} t_{PHL}	0.49 0.67	0.62 0.82	0.73 0.94	0.83 1.05	0.94 1.17

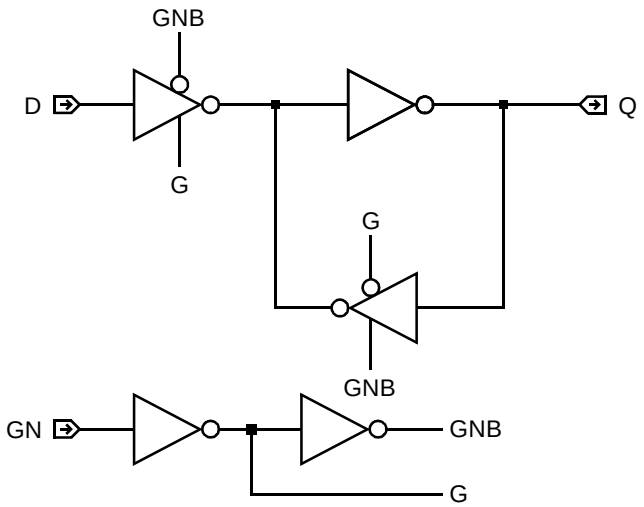
Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell DL001	Cell DL002
Min GN Width	Low	t_w	0.63	0.66
Min D Setup		t_{su}	0.44	0.47
Min D Hold		t_h	0.14	0.15

Logic Schematic



Core Logic