DL011

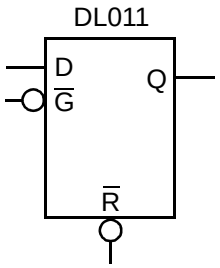
AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

DL011 is a transparent, unbuffered D latch with active low gate transparency. RESET is active low.

Logic Symbol



Truth Table

RN	D	GN	Q
H	L	L	L
H	H	L	H
H	X	H	NC
L	X	X	L

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
GN	1.0
RN	1.0

Core Logic

Equivalent Gates 5.0

HDL Syntax

Verilog ..... DL011 *inst_name* (Q, D, GN, RN);

VHDL..... *inst_name*: DL011 port map (Q, D, GN, RN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	9.0	Eq-load

See page 2-15 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	2	5	8	10 (max)
D	Q	t_{PLH} t_{PHL}	0.43 0.46	0.48 0.50	0.65 0.60	0.81 0.70	0.91 0.77
GN	Q	t_{PLH} t_{PHL}	0.54 0.62	0.59 0.67	0.74 0.77	0.90 0.87	1.01 0.93
RN	Q	t_{PLH} t_{PHL}	0.32 0.26	0.38 0.29	0.54 0.39	0.70 0.48	0.80 0.53

Delay (ns)

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min GN Width	Low	t_w	0.63
Min RN Width	Low	t_w	0.65
Min D Setup		t_{su}	0.45
Min D Hold		t_h	0.15
Min RN Setup		t_{su}	0.33
Min RN Hold		t_h	0.25

Logic Schematic