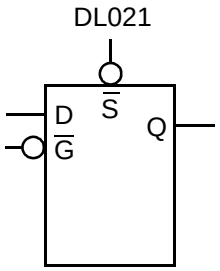
AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

DL021 is a transparent, unbuffered D latch with active low gate transparency. SET is active low.

Logic Symbol



Truth Table

SN	GN	D	Q
L	X	X	H
H	H	X	NC
H	L	L	L
H	L	H	H

NC = No Change

Pin Loading

	Equivalent Load
D	1.0
GN	1.0
SN	1.0

Equivalent Gates 4.0

HDL Syntax

Verilog ..... DL021 *inst_name* (Q, D, GN, SN);

VHDL..... *inst_name*: DL021 port map (Q, D, GN, SN);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	7.5	Eq-load

See page 2-15 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

From	To	Parameter	Number of Equivalent Loads				
			1	2	5	8	10 (max)
D	Q	t_{PLH} t_{PHL}	0.38 0.53	0.42 0.58	0.51 0.73	0.59 0.88	0.65 0.97
GN	Q	t_{PLH} t_{PHL}	0.48 0.71	0.52 0.77	0.61 0.92	0.70 1.05	0.76 1.13
SN	Q	t_{PLH} t_{PHL}	0.14 0.21	0.17 0.26	0.27 0.42	0.36 0.57	0.42 0.66

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Value
Min GN Width	Low	t_w	0.70
Min SN Width	Low	t_w	0.62
Min D Setup		t_{su}	0.53
Min D Hold		t_h	0.14
Min SN Setup		t_{su}	0.22
Min SN Hold		t_h	0.41

Logic Schematic