DL140/D
Rev. 6, Jan-2001

High Performance ECL Data

ECLinPS™ and ECLinPS Lite™

ON Semiconductor™

High Performance ECL Device Data

ECLinPS™, ECLinPS Lite™, and Low Voltage ECLinPS

DL140/D
Rev. 6, Jan–2001

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CHAPTER 1
ECLinPS Data Sheets

MC10E016, MC100E016

5V ECL 8-Bit Synchronous Binary Up Counter

The MC10E/100E016 is a high-speed synchronous, presettable, cascadable 8-bit binary counter. Architecture and operation are the same as the MC10H016 in the MECL 10H family, extended to 8-bits, as shown in the logic symbol.

The counter features internal feedback of $\overline{TC}$, gated by the TCLD (terminal count load) pin. When TCLD is LOW (or left open, in which case it is pulled LOW by the internal pull-downs), the $\overline{TC}$ feedback is disabled, and counting proceeds continuously, with $\overline{TC}$ going LOW to indicate an all-one state. When TCLD is HIGH, the $\overline{TC}$ feedback causes the counter to automatically reload upon $\overline{TC}$ = LOW, thus functioning as a programmable counter. The Q_n outputs do not need to be terminated for the count function to operate properly. To minimize noise and power, unused Q outputs should be left unterminated.

The 100 series contains temperature compensation.

- 700MHz Min. Count Frequency
- 1000ps CLK to Q, $\overline{TC}$
- Internal $\overline{TC}$ Feedback (Gated)
- 8-Bit
- Fully Synchronous Counting and $\overline{TC}$ Generation
- Asynchronous Master Reset
- PECL Mode Operating Range: $V_{CC=}$ 4.2 V to 5.7 V with V_{EE} = 0 V
- NECL Mode Operating Range: $V_{CC=}$ 0 V with V_{EE} = –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 200 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 592 devices

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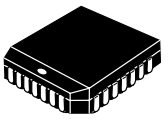
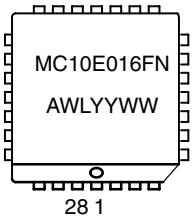


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAMS



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E016FN	PLCC–28	37 Units/Rail
MC10E016FNR2	PLCC–28	500 Units/Reel
MC100E016FN	PLCC–28	37 Units/Rail
MC100E016FNR2	PLCC–28	500 Units/Reel

FUNCTION TABLE

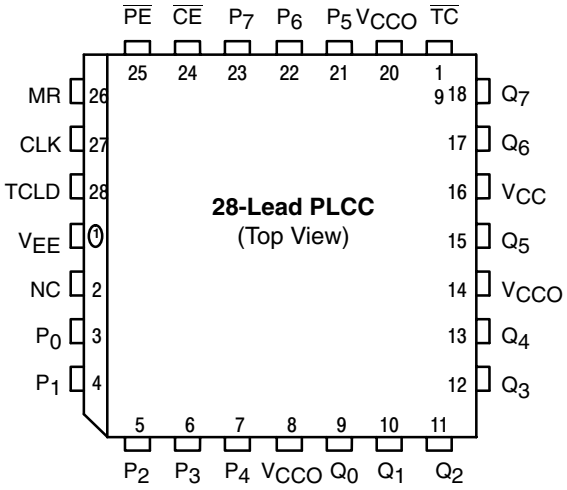
CE	PE	TCLD	MR	CLK	FUNCTION
X	L	X	L	Z	Load Parallel (P_n to Q_n)
L	H	L	L	Z	Continuous Count
L	H	H	L	Z	Count; Load Parallel on $\overline{TC}$ = LOW
H	H	X	L	Z	Hold
X	X	X	L	ZZ	Masters Respond, Slaves Hold
X	X	X	H	X	Reset (Q_n : = LOW, $\overline{TC}$: = HIGH)

Z= clock pulse (low to high);
ZZ= clock pulse (high to low)

PIN DESCRIPTION

PIN	FUNCTION
$P0 - P_7$	ECL Parallel Data (Preset) Inputs
$Q_0 - Q_7$	ECL Data Outputs
$\overline{CE}$	ECL Count Enable Control Input
$\overline{PE}$	ECL Parallel Load Enable Control Input
MR	ECL Master Reset
CLK	ECL Clock
$\overline{TC}$	ECL Terminal Count Output
TCLD	ECL TC-Load Control Input
NC	No Connect
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply

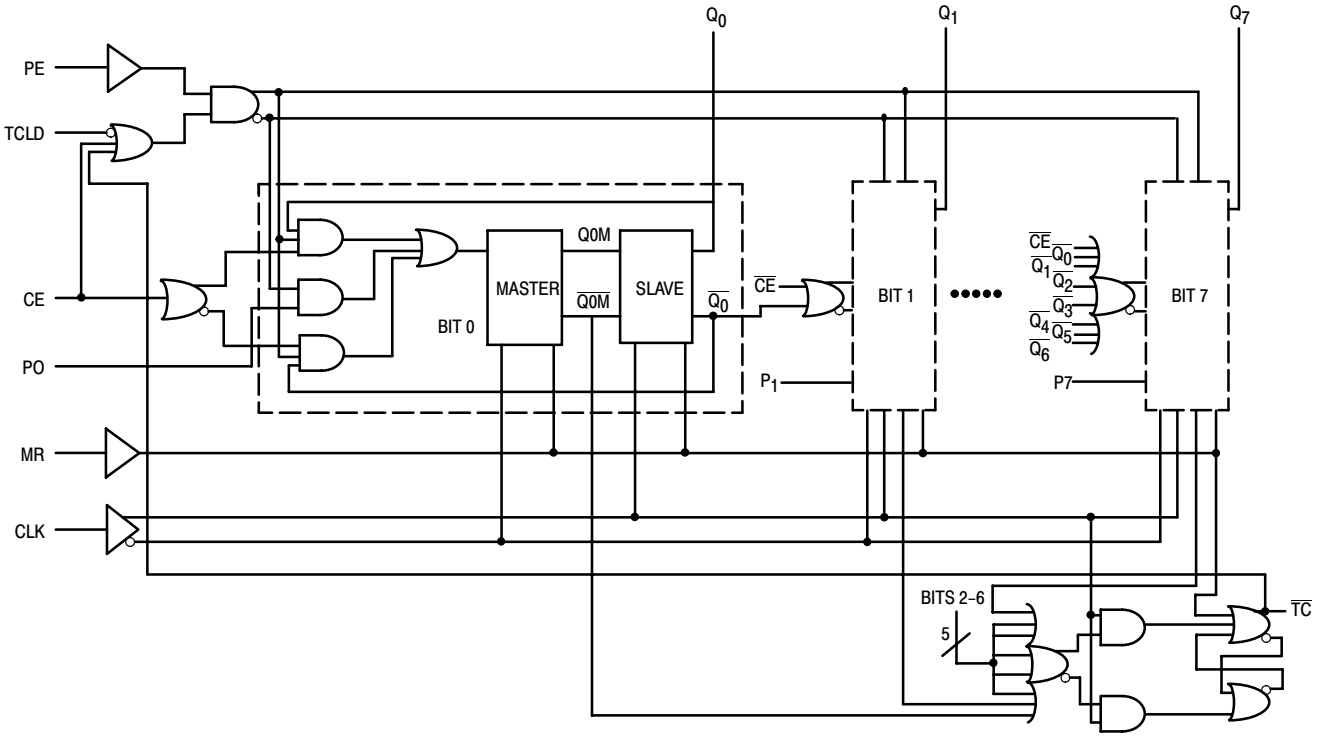
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

8-BIT BINARY COUNTER LOGIC DIAGRAM



Note that this diagram is provided for understanding of logic operation only.
It should not be used for propagation delays as many gate functions are achieved internally without incurring a full gate delay.

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		151	181		151	181		151	181	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		151	181		151	181		151	181	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		151	181		151	181		174	208	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		151	181		151	181		174	208	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
f_{COUNT}	Max. Count Frequency	700	900		700	900		700	900		MHz
t_{PLH}	Propagation Delay to Output										ps
t_{PHL}	CLK to Q	600	725	1000	600	725	1000	600	725	1000	
	MR to Q	600	775	1000	600	775	1000	600	775	1000	
	CLK to $\overline{TC}$	550	775	900	550	775	900	550	775	1050	
	MR to $\overline{TC}$	625	775	1000	625	775	1000	625	775	1000	
t_s	Setup Time (to CLK +)										ps
	Pn	150	– 30		150	– 30		150	– 30		
	$\overline{CE}$	600	400		600	400		600	400		
	$\overline{PE}$	600	400		600	400		600	400		
	TCLD	500	300		500	300		500	300		
t_h	Hold Time (to CLK +)										
	Pn	350	100		350	100		350	100		
	$\overline{CE}$	0	– 400		0	– 400		0	– 400		
	$\overline{PE}$	0	– 400		0	– 400		0	– 400		
	TCLD	100	– 300		100	– 300		100	– 300		
t_{RR}	Reset Recovery Time	900	700		900	700		900	700		ps
t_{PW}	Minimum Pulse Width										ps
	CLK, MR	400			400			400			
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r	Rise/Fall Times										ps
t_f	(20 - 80%)	300	510	800	300	510	800	300	510		

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.

FUNCTION TABLE

Function	PE	CE	MR	TCLD	CLK	P7-P4	P3	P2	P1	P0	Q7-Q4	Q3	Q2	Q1	Q0	TC
Load	L	X	L	X	Z	H	H	H	L	L	H	H	H	L	L	H
Count	H	L	L	L	Z	X	X	X	X	X	H	H	H	L	H	H
	H	L	L	L	Z	X	X	X	X	X	H	H	H	H	L	H
	H	L	L	L	Z	X	X	X	X	X	H	H	H	H	H	L
	H	L	L	L	Z	X	X	X	X	X	L	L	L	L	L	H
Load	L	X	L	X	Z	H	H	H	L	L	H	H	H	L	L	H
Hold	H	H	L	X	Z	X	X	X	X	X	H	H	H	L	L	H
	H	H	L	X	Z	X	X	X	X	X	H	H	H	L	L	H
Load On	H	L	L	H	Z	H	L	H	H	L	H	H	H	L	H	H
Terminal	H	L	L	H	Z	H	L	H	H	L	H	H	H	H	L	H
Count	H	L	L	H	Z	H	L	H	H	L	H	H	H	H	H	L
	H	L	L	H	Z	H	L	H	H	L	H	L	H	H	L	H
	H	L	L	H	Z	H	L	H	H	L	H	L	H	H	H	H
	H	L	L	H	Z	H	L	H	H	L	H	H	L	L	L	H
Reset	X	X	H	X	X	X	X	X	X	X	L	L	L	L	L	H

Applications Information

Cascading Multiple E016 Devices

For applications which call for larger than 8-bit counters multiple E016s can be tied together to achieve very wide bit width counters. The active low terminal count ($\overline{TC}$) output and count enable input ($\overline{CE}$) greatly facilitate the cascading of E016 devices. Two E016s can be cascaded without the need for external gating, however for counters wider than 16 bits external OR gates are necessary for cascade implementations.

Figure 1 below pictorially illustrates the cascading of 4 E016s to build a 32-bit high frequency counter. Note the E101 gates used to OR the terminal count outputs of the lower order E016s to control the counting operation of the higher order bits. When the terminal count of the preceding device (or devices) goes low (the counter reaches an all 1s state) the more significant E016 is set in its count mode and will count one binary digit upon the next positive clock transition. In addition, the preceding devices will also count one bit thus sending their terminal count outputs back to a high state disabling the count operation of the more significant counters and placing them back into hold modes. Therefore, for an E016 in the chain to count, all of the lower order terminal count outputs must be in the low state. The bit width of the counter can be increased or decreased by simply adding or subtracting E016 devices from Figure 1 and maintaining the logic pattern illustrated in the same figure.

The maximum frequency of operation for the cascaded counter chain is set by the propagation delay of the $\overline{TC}$ output and the necessary setup time of the $\overline{CE}$ input and the propagation delay through the OR gate controlling it (for 16-bit counters the limitation is only the $\overline{TC}$ propagation delay and the $\overline{CE}$ setup time). Figure 1 shows EL01 gates used to control the count enable inputs, however, if the frequency of operation is lower a slower, ECL OR gate can be used. Using the worst case guarantees for these parameters from the ECLinPS data book, the maximum count frequency for a greater than 16-bit counter is 500MHz and that for a 16-bit counter is 625MHz.

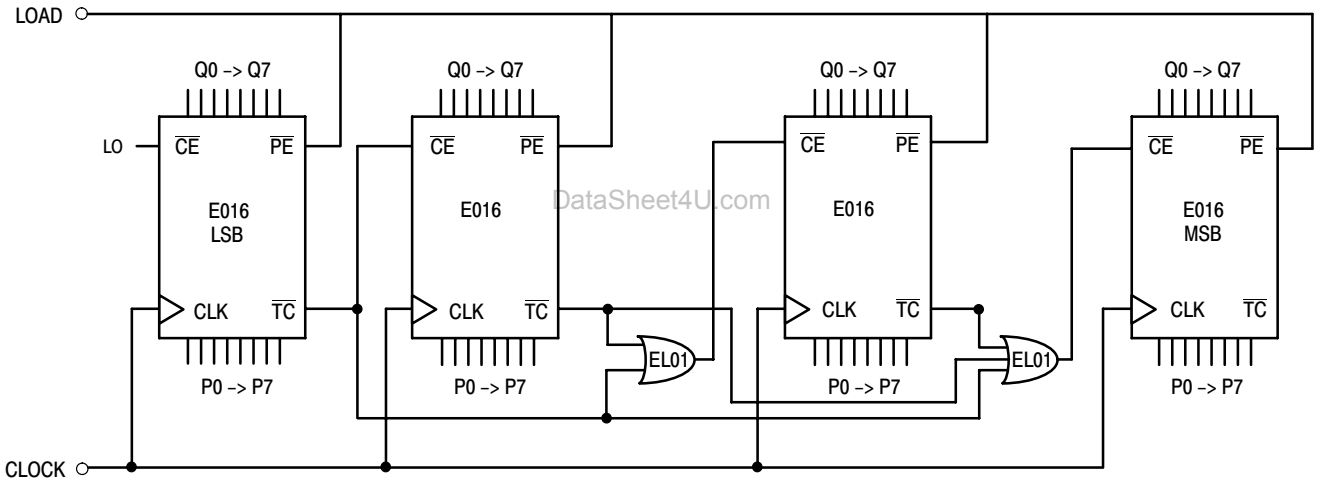


Figure 1. 32-Bit Cascaded E016 Counter

Applications Information (continued)

Note that this assumes the trace delay between the $\overline{TC}$ outputs and the $\overline{CE}$ inputs are negligible. If this is not the case estimates of these delays need to be added to the calculations.

Programmable Divider

The E016 has been designed with a control pin which makes it ideal for use as an 8-bit programmable divider. The TCLD pin (load on terminal count) when asserted reloads the data present at the parallel input pin (Pn's) upon reaching terminal count (an all 1s state on the outputs). Because this feedback is built internal to the chip, the programmable division operation will run at very nearly the same frequency as the maximum counting frequency of the device. Figure 2 below illustrates the input conditions necessary for utilizing the E016 as a programmable divider set up to divide by 113.

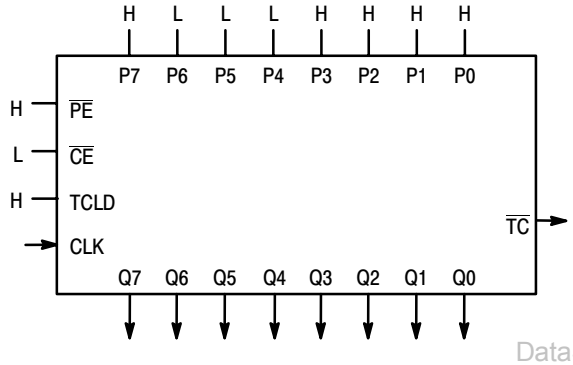


Figure 2. Mod 2 to 256 Programmable Divider

To determine what value to load into the device to accomplish the desired division, the designer simply subtracts the binary equivalent of the desired divide ratio from the binary value for 256. As an example for a divide ratio of 113:

$Pn's = 256 - 113 = 8F_{16} = 1000\ 1111$

where:

P0 = LSB and P7 = MSB

Forcing this input condition as per the setup in Figure 2 will result in the waveforms of Figure 3. Note that the $\overline{TC}$ output is used as the divide output and the pulse duration is equal to a full clock period. For even divide ratios, twice the desired divide ratio can be loaded into the E016 and the $\overline{TC}$ output can feed the clock input of a toggle flip flop to create a signal divided as desired with a 50% duty cycle.

Table 1. Preset Values for Various Divide Ratios

Divide Ratio	Preset Data Inputs							
	P7	P6	P5	P4	P3	P2	P1	P0
2	H	H	H	H	H	H	H	L
3	H	H	H	H	H	H	L	H
4	H	H	H	H	H	H	L	L
5	H	H	H	H	H	L	H	H
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
112	H	L	L	H	L	L	L	L
113	H	L	L	L	H	H	H	H
114	H	L	L	L	H	H	H	L
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
254	L	L	L	L	L	L	H	L
255	L	L	L	L	L	L	L	H
256	L	L	L	L	L	L	L	L

A single E016 can be used to divide by any ratio from 2 to 256 inclusive. If divide ratios of greater than 256 are needed multiple E016s can be cascaded in a manner similar to that already discussed. When E016s are cascaded to build larger dividers the TCLD pin will no longer provide a means for loading on terminal count. Because one does not want to reload the counters until all of the devices in the chain have reached terminal count, external gating of the $\overline{TC}$ pins must be used for multiple E016 divider chains.

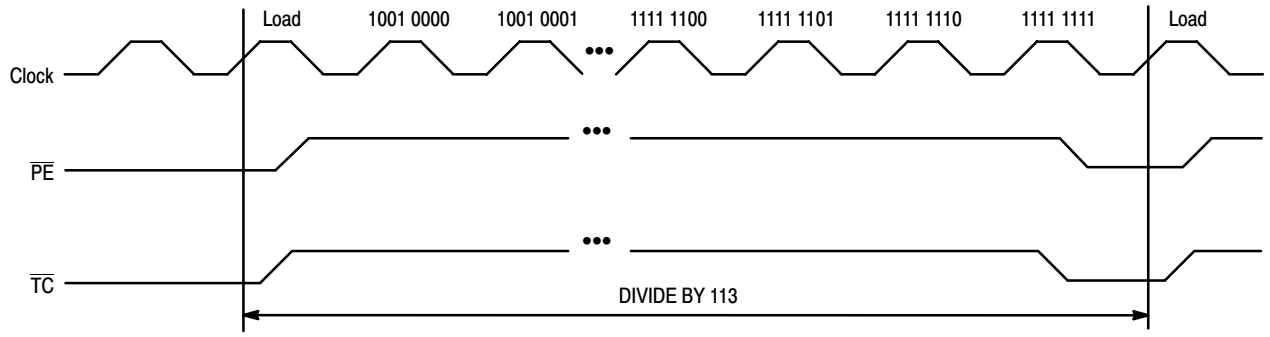


Figure 3. Divide by 113 E016 Programmable Divider Waveforms

Applications Information (continued)

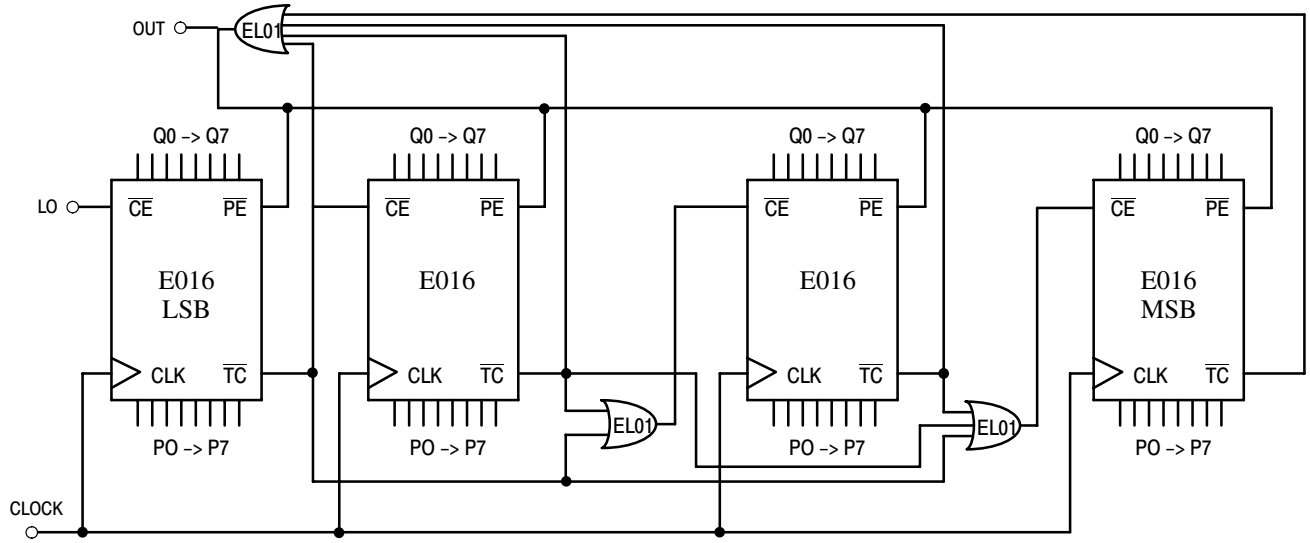


Figure 4. 32-Bit Cascaded E016 Programmable Divider

Figure 4 on the following page shows a typical block diagram of a 32-bit divider chain. Once again to maximize the frequency of operation EL01 OR gates were used. For lower frequency applications a slower OR gate could replace the EL01. Note that for a 16-bit divider the OR function feeding the $\overline{PE}$ (program enable) input CANNOT be replaced by a wire OR tie as the $\overline{TC}$ output of the least significant E016 must also feed the $\overline{CE}$ input of the most significant E016. If the two $\overline{TC}$ outputs were OR tied the cascaded count operation would not operate properly. Because in the cascaded form the $\overline{PE}$ feedback is external and requires external gating, the maximum frequency of operation will be significantly less than the same operation in a single device.

Maximizing E016 Count Frequency

The E016 device produces 9 fast transitioning single ended outputs, thus V_{CC} noise can become significant in situations where all of the outputs switch simultaneously in the same direction. This V_{CC} noise can negatively impact the maximum frequency of operation of the device. Since the device does not need to have the Q outputs terminated to count properly, it is recommended that if the outputs are not going to be used in the rest of the system they should be left unterminated. In addition, if only a subset of the Q outputs are used in the system only those outputs should be terminated. Not terminating the unused outputs will not only cut down the V_{CC} noise generated but will also save in total system power dissipation. Following these guidelines will allow designers to either be more aggressive in their designs or provide them with an extra margin to the published data book specifications.

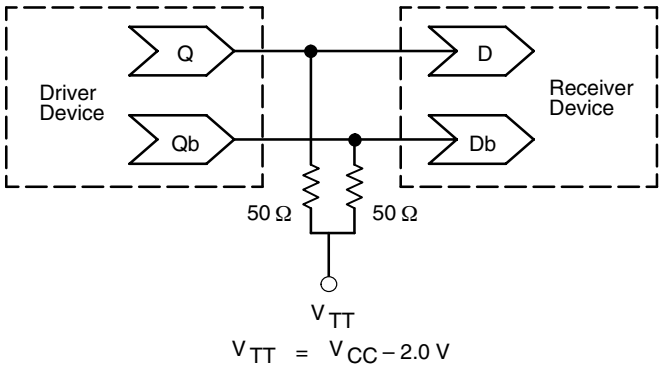


Figure 5. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E101, MC100E101

5V ECL Quad 4-Input OR/NOR Gate

The MC10E/100E101 is a quad 4-input OR/NOR gate. The 100 Series contains temperature compensation.

- 500 ps Max. Propagation Delay
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 200 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 115 devices

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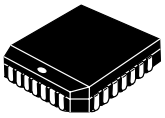
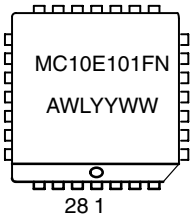
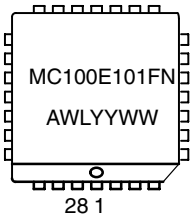
MARKING DIAGRAMS



PLCC–28
FN SUFFIX
CASE 776



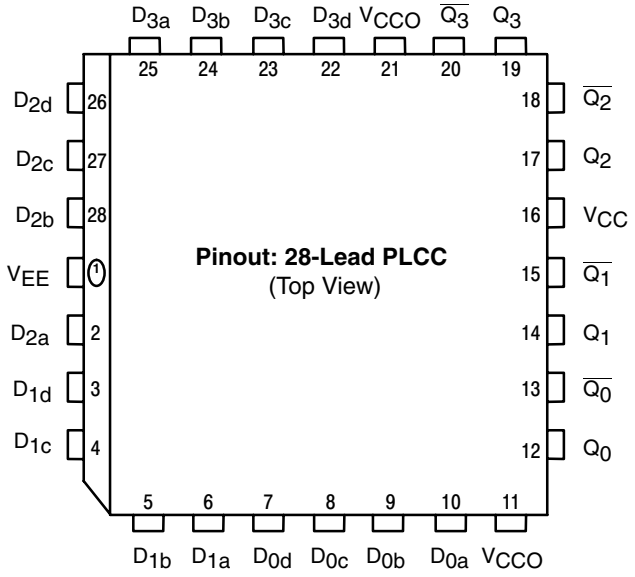
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week



ORDERING INFORMATION

Device	Package	Shipping
MC10E101FN	PLCC–28	37 Units/Rail
MC10E101FNR2	PLCC–28	500 Units/Reel
MC100E101FN	PLCC–28	37 Units/Rail
MC100E101FNR2	PLCC–28	500 Units/Reel

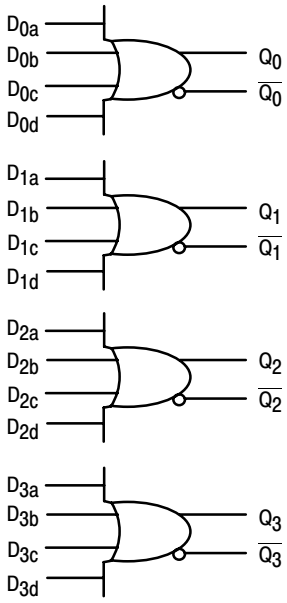
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN	FUNCTION
$D_{0a} - D_{3d}$	ECL Data Inputs
$Q_0 - Q3$, $\overline{Q_0} - \overline{Q_3}$	ECL Differential Outputs
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		30	36		30	36		30	36	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		30	36		30	36		30	36	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		30	36		30	36		35	42	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		30	36		30	36		35	42	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output D to Q	200	350	500	200	350	500	200	350	500	ps
t_{SKEW} t_{SKEW}	Within-Device Skew (Note 2.) Within-Gate Skew (Note 3.)		50 25			50 25			50 25		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Rise/Fall Time (20 - 80%)	300	380	575	300	380	575	300	380	575	ps

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.
3. Within-gate skew is defined as the variation in propagation delays of a gate when driven from its different inputs.

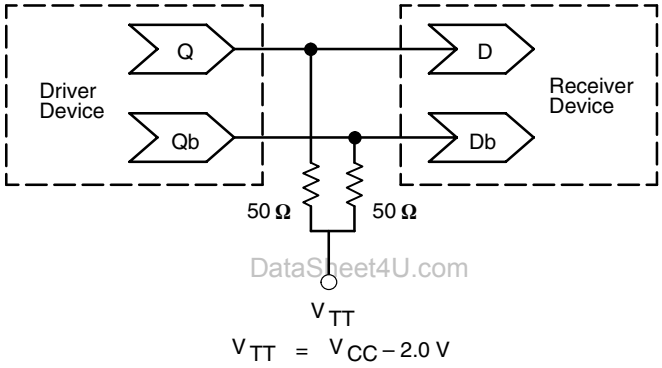


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E104, MC100E104

5V ECL Quint 2-Input AND/NAND Gate

The MC10E/100E104 is a quint 2-input AND/NAND gate. The function output F is the OR of all five AND gate outputs, while $\overline{F}$ is the NOR. The Q outputs need not be terminated if only the F outputs are to be used.

The 100 Series contains temperature compensation.

- 600 ps Max. Propagation Delay
- OR/NOR Function Outputs
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 200 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 134 devices

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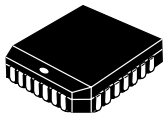
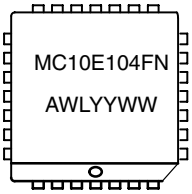
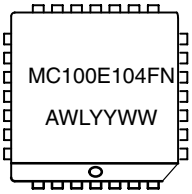
MARKING DIAGRAMS



PLCC–28
FN SUFFIX
CASE 776



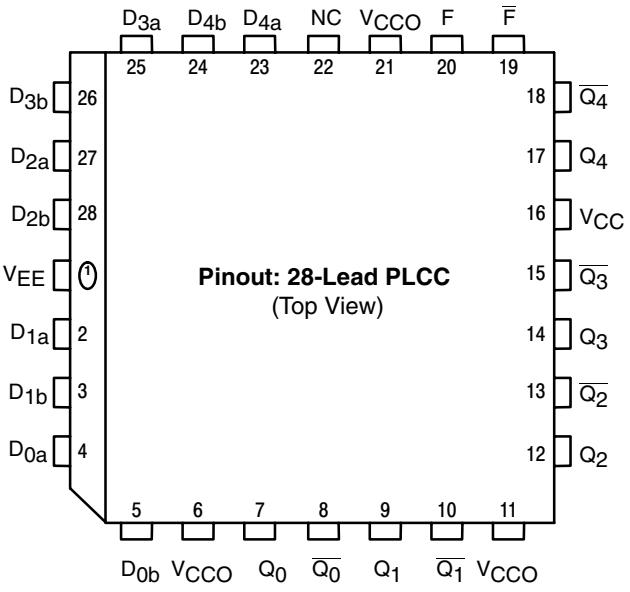
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week



ORDERING INFORMATION

Device	Package	Shipping
MC10E104FN	PLCC–28	37 Units/Rail
MC10E104FNR2	PLCC–28	500 Units/Reel
MC100E104FN	PLCC–28	37 Units/Rail
MC100E104FNR2	PLCC–28	500 Units/Reel

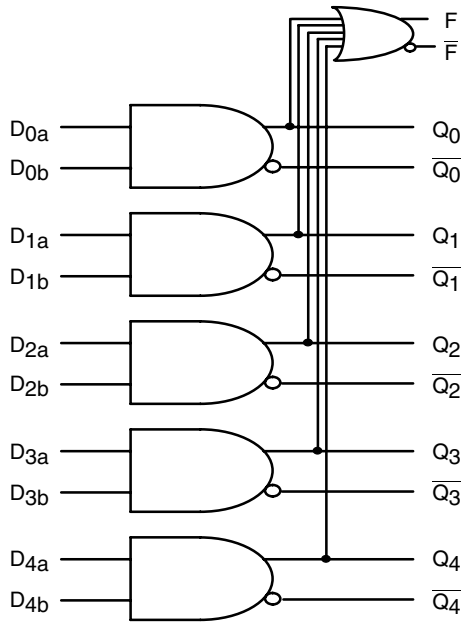
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN	FUNCTION
$D_{0a} - D_{4b}$	ECL Data Inputs
$Q_0 - Q_4$	ECL AND Outputs
$\overline{Q_0} - \overline{Q_4}$	ECL NAND Outputs
F	ECL OR Output
$\overline{F}$	ECL NOR Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

FUNCTION OUTPUTS

$$F = (D_{0a} \bullet D_{0b}) + (D_{1a} \bullet D_{1b}) + (D_{2a} \bullet D_{2b}) + (D_{3a} \bullet D_{3b}) + (D_{4a} \bullet D_{4b})$$

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		38	46		38	46		38	46	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current			200			200			200	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		38	46		38	46		38	46	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current			200			200			200	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		38	46		38	46		44	53	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current			200			200			200	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		38	46		38	46		44	53	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
I_{IH}	Input HIGH Current			200			200			200	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH}	Propagation Delay to Output										ps
t_{PHL}	D to Q	225	385	600	225	385	600	225	385	600	
	D to F	500	725	1000	500	725	1000	500	725	1000	
t_{SKEW}	Within-Device Skew (Note 2.)										ps
	D to Q		75			75			75		
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r	Rise/Fall Times										ps
t_f	(20 - 80%)										
	Q	275	425	700	275	425	700	275	425	700	
	F	300	475	700	300	475	700	300	475	700	

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.

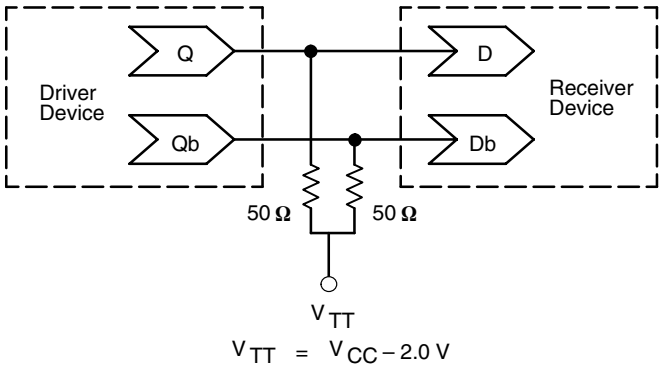


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E107, MC100E107

5V ECL Quint 2-Input XOR/XNOR Gate

The MC10E/100E107 is a quint 2-input XOR/XNOR gate. The function output F is the OR of all five XOR outputs, while $\overline{F}$ is the NOR. The Q outputs need not be terminated if only the F outputs are to be used.

The 100 Series contains temperature compensation.

- 600 ps Max. Propagation Delay
- OR/NOR Function Outputs
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 200 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 140 devices

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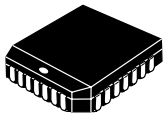
MARKING DIAGRAMS



PLCC–28
FN SUFFIX
CASE 776

28 1

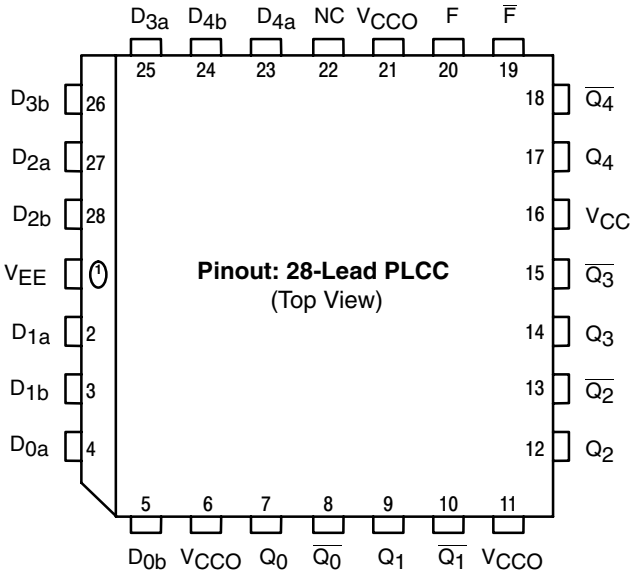
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

28 1

ORDERING INFORMATION

Device	Package	Shipping
MC10E107FN	PLCC–28	37 Units/Rail
MC10E107FNR2	PLCC–28	500 Units/Reel
MC100E107FN	PLCC–28	37 Units/Rail
MC100E107FNR2	PLCC–28	500 Units/Reel

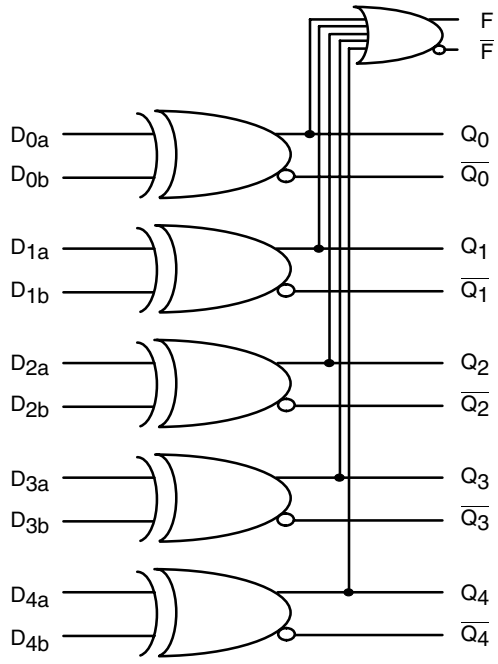
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN	FUNCTION
$D_{0a} - D_{4b}$	ECL Data Inputs
$Q_0 - Q_4$	ECL XOR Outputs
$\overline{Q_0} - \overline{Q_4}$	ECL XNOR Outputs
F	ECL OR Output
$\overline{F}$	ECL NOR Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

FUNCTION OUTPUTS

$$F = (D_{0a} \oplus D_{0b}) + (D_{1a} \oplus D_{1b})\,(D_{2a} \oplus D_{2b}) + (D_{3a} \oplus D_{3b}) + (D_{4a} \oplus D_{4b})$$

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ		Unit
I_{EE}	Power Supply Current		42	50		42	50		42	50	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current			200			200			200	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		42	50		42	50		42	50	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current			200			200			200	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		42	50		42	50		48	58	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current			200			200			200	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		42	50		42	50		48	58	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
I_{IH}	Input HIGH Current			200			200			200	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH}	Propagation Delay to Output										ps
t_{PHL}	D to Q	250	410	600	250	410	600	250	410	600	
	D to F	500	725	1000	500	725	100	500	725	1000	
t_{SKEW}	Within-Device Skew										ps
	D to Q (Note 2.)		75			75			75		
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r	Rise/Fall Times										ps
t_f	(20 - 80%)										
	Q	275	450	700	275	450	700	275	450	700	
	F	300	475	700	300	475	700	300	475	700	

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.

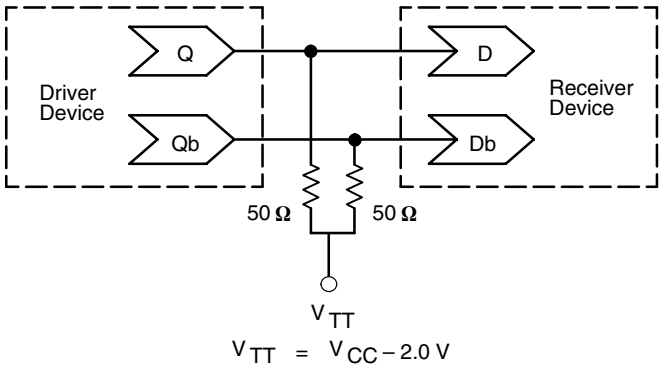


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E111, MC100E111

5V ECL 1:9 Differential Clock Driver

The MC10E/100E111 is a low skew 1-to-9 differential driver, designed with clock distribution in mind. It accepts one signal input, which can be either differential or else single-ended if the V_{BB} output is used. The signal is fanned out to 9 identical differential outputs. An enable input is also provided. A HIGH disables the device by forcing all Q outputs LOW and all $\overline{Q}$ outputs HIGH.

The device is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate to gate skew within-device, and empirical modeling is used to determine process control limits that ensure consistent t_{pd} distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50 Ω, even if only one side is being used. In most applications, all nine differential pairs will be used and therefore terminated. In the case where fewer than nine pairs are used, it is necessary to terminate at least the output pairs on the same package side (i.e. sharing the same V_{CCO}) as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20 ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

- Guaranteed Skew Spec
- Differential Design
- V_{BB} Output
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 3 KV HBM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 178 devices

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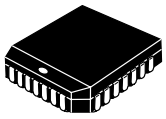
MARKING DIAGRAMS



PLCC–28
FN SUFFIX
CASE 776

28 1

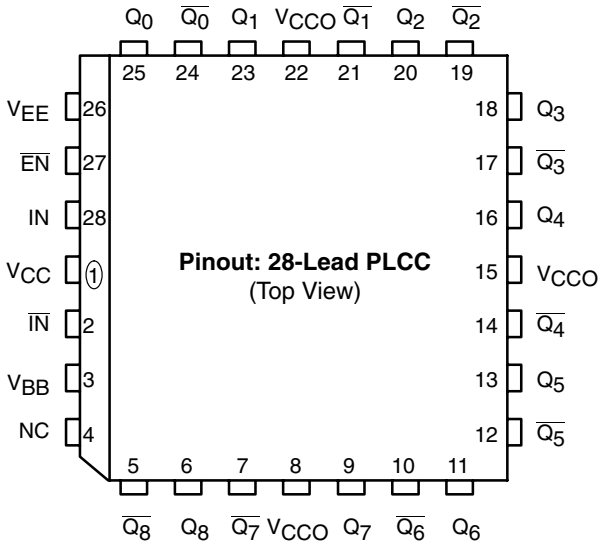
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

28 1

ORDERING INFORMATION

Device	Package	Shipping
MC10E111FN	PLCC–28	37 Units/Rail
MC10E111FNR2	PLCC–28	500 Units/Reel
MC100E111FN	PLCC–28	37 Units/Rail
MC100E111FNR2	PLCC–28	500 Units/Reel

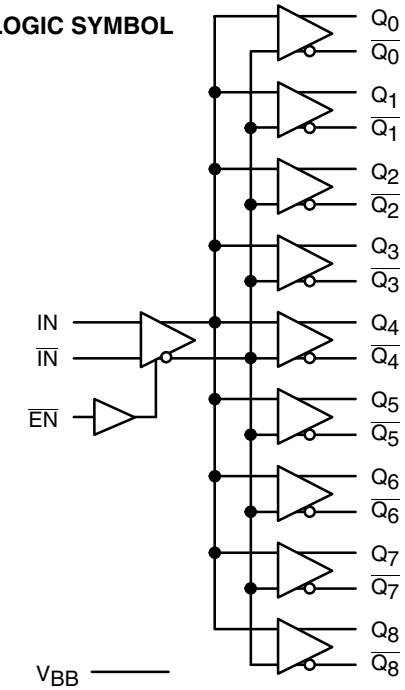
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC SYMBOL



PIN DESCRIPTION

PIN	FUNCTION
IN, IN	ECL Differential Input Pair
$\overline{EN}$	ECL Enable
Q_0, $\overline{Q_0}$–Q_8, $\overline{Q_8}$	ECL Differential Outputs
V_{BB}	Reference Voltage Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		48	60		48	60		48	60	mA
V_{OH}	Output HIGH Voltage (Note 2.)				4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)				3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single Ended)				3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage (Single Ended)				3050	3285	3520	3050	3302	3555	mV
V_{BB}	Output Voltage Reference	3.57		3.7	3.65		3.75	3.69		3.90	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.6		4.6	2.6		4.6	2.6		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current				0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		48	60		48	60		48	60	mA
V_{OH}	Output HIGH Voltage (Note 2.)				–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)				–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage (Single Ended)				–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage (Single Ended)				–1950	–1715	–1480	–1950	–1698	–1445	mV
V_{BB}	Output Voltage Reference	–1.43		–1.30	–1.35		–1.25	–1.31		–1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.4		–0.4	–2.4		–0.4		–2.4	–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current				0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		48	60		48	60		55	69	mA
V_{OH}	Output HIGH Voltage (Note 2.)				3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)				3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)				3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage (Single Ended)				3190	3525	3525	3190	3525	3525	mV
V_{BB}	Output Voltage Reference	3.64		3.75	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.6		4.6	2.6		4.6	2.6		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current				0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		48	60		48	60		55	69	mA
V_{OH}	Output HIGH Voltage (Note 2.)				–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)				–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)				–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage (Single Ended)				–1810	–1475	–1475	–1810	–1475	–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.25	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.4		–0.4	–2.4		–0.4	–2.4		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current				0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

AC CHARACTERISTICS V_{CCx} = 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output IN (Diff) (Note 2.) IN (SE) (Note 3.) Enable (Note 4.) Disable Note 4.)	 380 280 400 400		 680 780 900 900	 480 430 450 450		 580 630 850 850	 510 460 450 450		 610 660 850 850	ps
t_S	Setup Time (Note 6.) $\overline{EN}$ to IN	250	0		200	0		200	0		ps
t_H	Hold Time (Note 7.) IN to $\overline{EN}$	50	–200		0	–200		0	–200		ps
t_R	Release Time (Note 8.) $\overline{EN}$ to IN	350	100		300	100		300	100		ps
t_{skew}	Within-Device Skew (Note 5.)		25	75		25	50		25	50	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Minimum Input Swing	50			50			50			mV
t_r, t_f	Rise/Fall Time	250	450	650	275	375	600	275	375	600	ps

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 / –0.8 V.
2. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
3. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
4. Enable is defined as the propagation delay from the 50% point of a **negative** transition on $\overline{EN}$ to the 50% point of a **positive** transition on Q (or a negative transition on $\overline{Q}$). Disable is defined as the propagation delay from the 50% point of a **positive** transition on $\overline{EN}$ to the 50% point of a **negative** transition on Q (or a positive transition on $\overline{Q}$).
5. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
6. The setup time is the minimum time that $\overline{EN}$ must be asserted prior to the next transition of IN/$\overline{IN}$ to prevent an output response greater than ±75 mV to that IN/$\overline{IN}$ transition (see Figure 1).
7. The hold time is the minimum time that $\overline{EN}$ must remain asserted after a negative going IN or a positive going $\overline{IN}$ to prevent an output response greater than ±75 mV to that IN/$\overline{IN}$ transition (see Figure 2).
8. The release time is the minimum time that $\overline{EN}$ must be deasserted prior to the next IN/$\overline{IN}$ transition to ensure an output response that meets the specified IN to Q propagation delay and output transition times (see Figure 3).

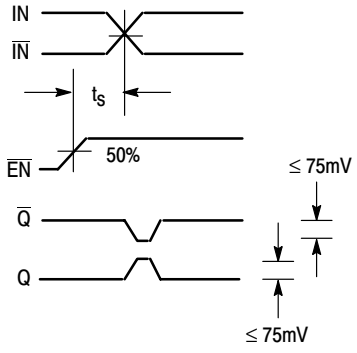


Figure 1. Setup Time

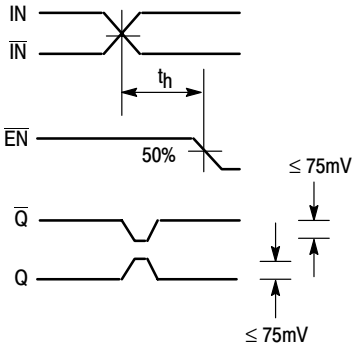


Figure 2. Hold Time

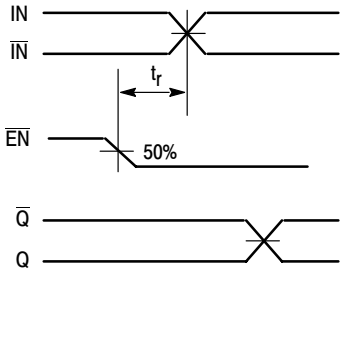


Figure 3. Release Time

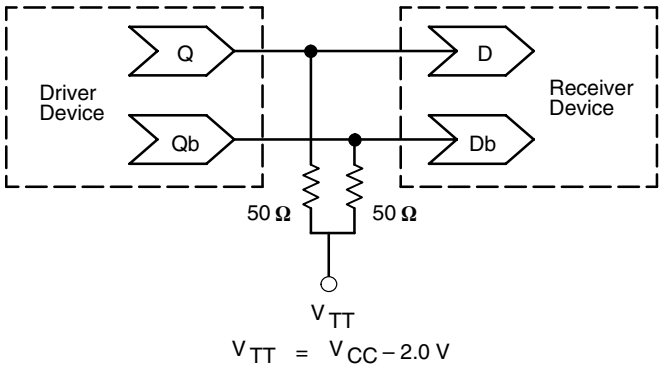


Figure 4. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E112, MC100E112

5V ECL Quad Driver

The MC10E/100E112 is a quad driver with two pairs of OR/NOR outputs from each gate, and a common, buffered enable input. Using the data inputs the device can serve as an ECL memory address fan-out driver. Using just the enable input, the device serves as a clock driver, although the MC10E/100E111 is designed specifically for this purpose, and offers lower skew than the E112. For memory address driver applications where scan capabilities are required, please refer to the E212 device.

The 100 Series contains temperature compensation.

- 600 ps Max. Propagation Delay
- Common Enable Input
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 200 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 125 devices

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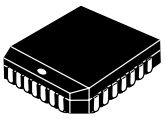
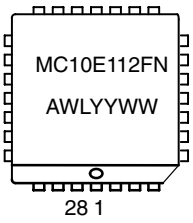
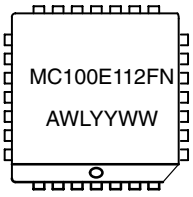
MARKING DIAGRAMS



PLCC–28
FN SUFFIX
CASE 776



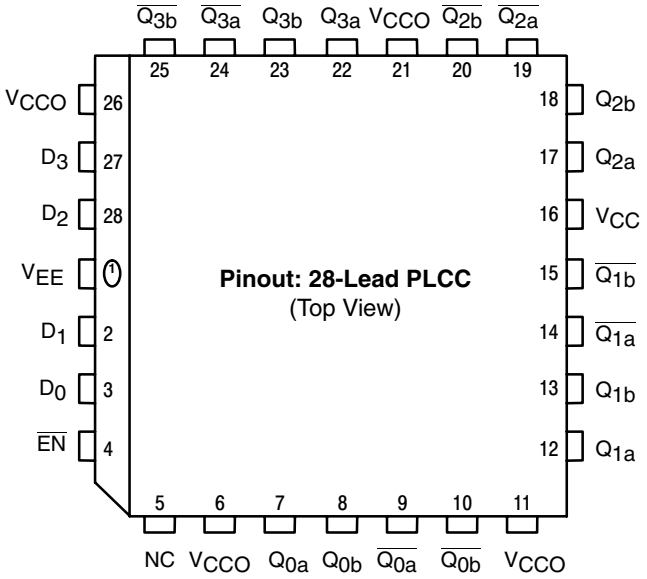
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week



ORDERING INFORMATION

Device	Package	Shipping
MC10E112FN	PLCC–28	37 Units/Rail
MC10E112FNR2	PLCC–28	500 Units/Reel
MC100E112FN	PLCC–28	37 Units/Rail
MC100E112FNR2	PLCC–28	500 Units/Reel

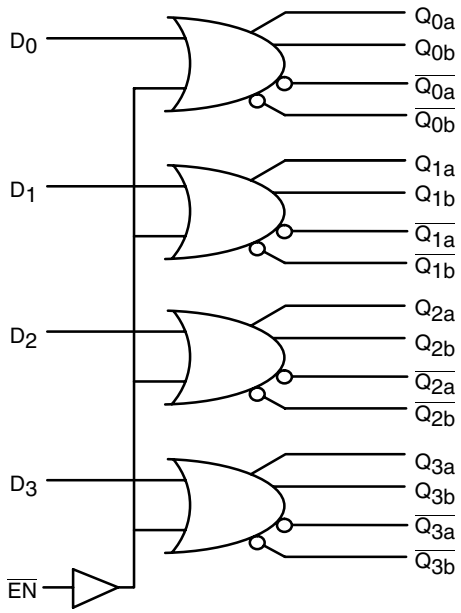
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN	FUNCTION
$D_0 - D_3$	ECL Data Inputs
$\overline{EN}$	ECL Enable Input
Q_{na}, Q_{nb}	ECL True Outputs
$\overline{Q_{na}}$, $\overline{Q_{nb}}$	ECL Inverting Outputs
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		47	56		47	56		47	56	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current			200			200			200	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		47	56		47	56		47	56	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current			200			200			200	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		47	56		47	56		54	65	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current			200			200			200	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		47	56		47	56		54	65	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
I_{IH}	Input HIGH Current			200			200			200	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz 25
t_{PLH}	Propagation Delay to Output										ps
t_{PHL}	D	200	400	600	200	400	600	200	400	600	
	EN	275	450	675	275	450	675	275	450	675	
t_{SKEW}	Within-Device Skew										ps
	Dn to Qn, $\overline{Qn}$ (Note 2.)		80			80			80		
	Qna to Qnb (Note 3.)		40			40			40		
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r	Rise/Fall Times										ps
t_f	(20 - 80%)	275	425	700	275	425	700	275	425	700	

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.
3. Skew defined between common OR or common NOR outputs of a single gate.

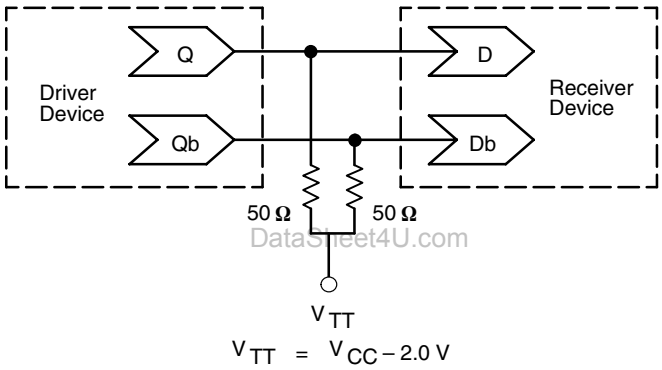


Figure 1. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405 – ECL Clock Distribution Techniques
AN1406 – Designing with PECL (ECL at +5.0 V)
AN1503 – ECLinPS I/O SPICE Modeling Kit
AN1504 – Metastability and the ECLinPS Family
AN1568 – Interfacing Between LVDS and ECL
AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650 – Using Wire–OR Ties in ECLinPS Designs
AN1672 – The ECL Translator Guide
AND8001 – Odd Number Counters Design
AND8002 – Marking and Date Codes
AND8020 – Termination of ECL Logic Devices

MC10E116, MC100E116

5V ECL Quint Differential Line Receiver

The MC10E/100E116 is a quint differential line receiver with emitter-follower outputs. For applications which require bandwidths greater than that of the E116, the E416 device may be of interest.

Active current sources plus a deep collector feature of the MOSAIC III process provide the receivers with excellent common-mode noise rejection. Each receiver has a dedicated V_{CCO} supply lead, providing optimum symmetry and stability.

If both inverting and non-inverting inputs are at an equal potential of > –2.5 V, the receiver does *not* go to a defined state, but rather current-shares in normal differential amplifier fashion, producing output voltage levels midway between HIGH and LOW, or the device may even oscillate.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

- 500 ps Max. Propagation Delay
- V_{BB} Supply Output
- Dedicated V_{CCO} Pin for Each Receiver
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Output Qs will default low when inputs are <V_{CC} –2.5 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- ESD Protection: > 2 KV HBM, > 200 V MM
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 98 devices

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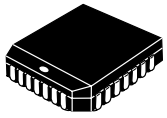
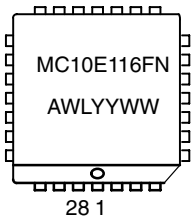


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAMS

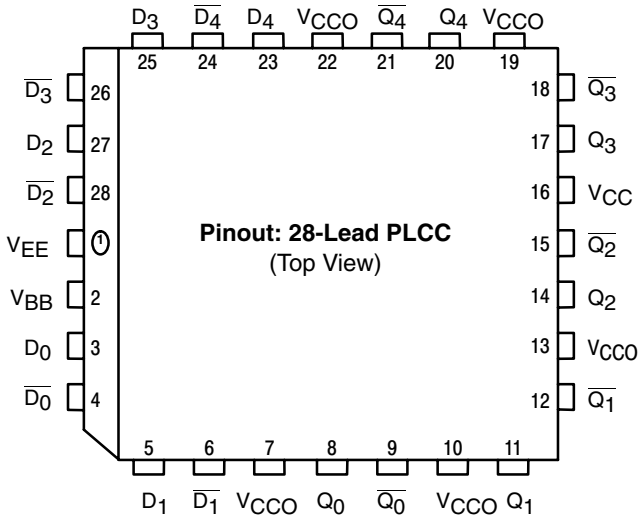


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E116FN	PLCC–28	37 Units/Rail
MC10E116FNR2	PLCC–28	500 Units/Reel
MC100E116FN	PLCC–28	37 Units/Rail
MC100E116FNR2	PLCC–28	500 Units/Reel

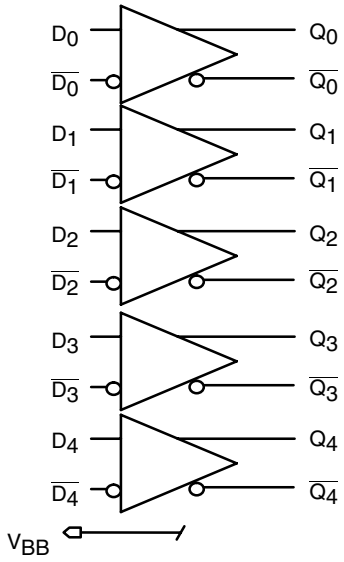
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN	FUNCTION
D_0, $\overline{D_0}$ – D_4, $\overline{D_4}$	ECL Differential Input Pairs
Q_0, $\overline{Q_0}$ – Q_4, $\overline{Q_4}$	ECL Differential Output Pairs
V_{BB}	Reference Voltage Output.
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		29	35		29	35		29	35	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage (Single Ended)	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
V_{BB}	Output Voltage Reference	3.57		3.00	3.65		3.75	3.69		3.81	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.2		4.4	2.2		4.4	2.2		4.4	V
I_{IH}	Input HIGH Current			200			200			200	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		29	35		29	35		29	35	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
V_{BB}	Output Voltage Reference	–1.13		–1.30	–1.35		–1.25	–1.31		–1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.8		–0.6	–2.8		–0.6	–2.8		–0.6	V
I_{IH}	Input HIGH Current			200			200			200	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		29	35		29	35		29	40	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
V_{BB}	Output Voltage Reference	3.64		3.75	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.2		4.4	2.2		4.4	2.2		4.4	V
I_{IH}	Input HIGH Current			200			200			200	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		29	35		29	35		29	40	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.25	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.8		–0.6	–2.8		–0.6	–2.8		–0.6	V
I_{IH}	Input HIGH Current			200			200			200	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output D (Differential) D (Single-Ended)	 150 150	 300 300	 500 550	 200 150	 300 300	 450 500	 200 150	 300 300	 450 500	ps
t_{skew}	Within-Device Skew (Note 2.)		50			50			50		ps
t_{skew}	Duty Cycle Skew (Note 3.) $t_{PLH} - t_{PHL}$		±10			±10			±10		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}(AC)	Minimum Input Swing (Note 4.)	150			150			150			mV
t_r/t_f	Rise/Fall Time 20–80%	250	375	625	???	???	???	275	375	575	ps

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.
3. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.
4. Minimum input swing for which AC parameters are guaranteed.

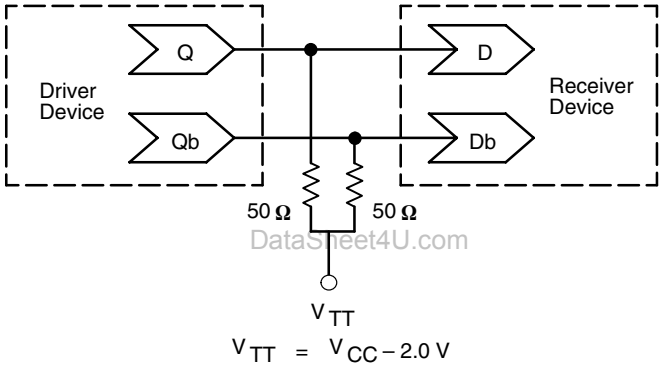


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405 – ECL Clock Distribution Techniques
AN1406 – Designing with PECL (ECL at +5.0 V)
AN1503 – ECLinPS I/O SPICE Modeling Kit
AN1504 – Metastability and the ECLinPS Family
AN1568 – Interfacing Between LVDS and ECL
AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650 – Using Wire–OR Ties in ECLinPS Designs
AN1672 – The ECL Translator Guide
AND8001 – Odd Number Counters Design
AND8002 – Marking and Date Codes
AND8020 – Termination of ECL Logic Devices

MC10E122, MC100E122

5V ECL 9-Bit Buffer

The MC10E/100E122 is a 9-bit buffer. The device contains nine non-inverting buffer gates.

The 100 Series contains temperature compensation.

- 500 ps Max. Propagation Delay
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 200 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 111 devices

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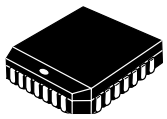
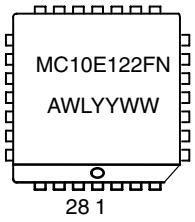
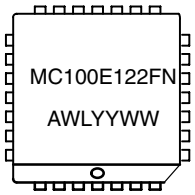


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAMS



28 1



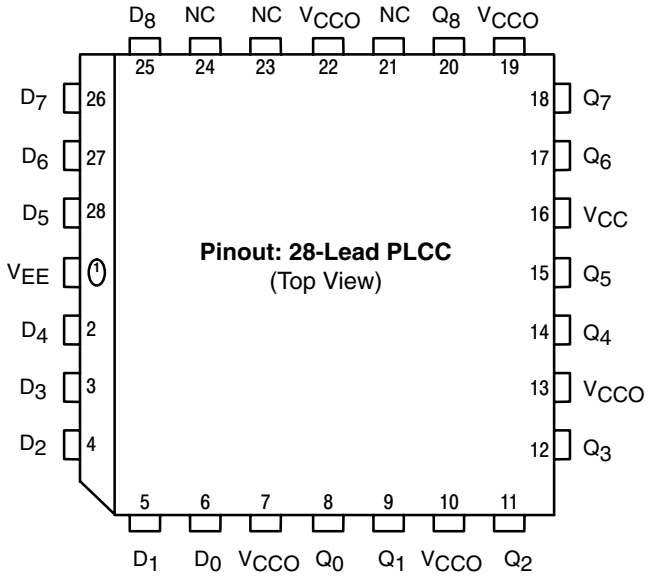
28 1

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E122FN	PLCC–28	37 Units/Rail
MC10E122FNR2	PLCC–28	500 Units/Reel
MC100E122FN	PLCC–28	37 Units/Rail
MC100E122FNR2	PLCC–28	500 Units/Reel

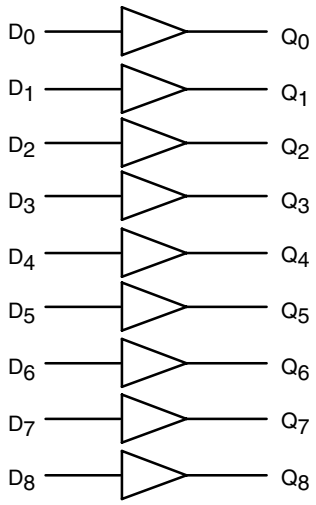
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN	FUNCTION
$D_0 – D_8$	ECL Data Inputs
$Q_0 – Q_8$	ECL Data Outputs
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		41	49		41	49		41	49	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current			200			200			200	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		41	49		41	49		41	49	mA
V_{OH}	Output HIGH Voltage	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current			200			200			200	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		41	49		41	49		47	57	mA
V_{OH}	Output HIGH Voltage	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current			200			200			200	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		41	49		41	49		47	57	mA
V_{OH}	Output HIGH Voltage	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
I_{IH}	Input HIGH Current			200			200			200	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output D to Q	150	350	500	150	350	500	150	350	500	ps
t_{SKEW}	Within-Device Skew D to Q (Note 2.)		75			75			75		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Rise/Fall Times (20 - 80%)	300	425	800	300	425	800	300	425	800	ps

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.

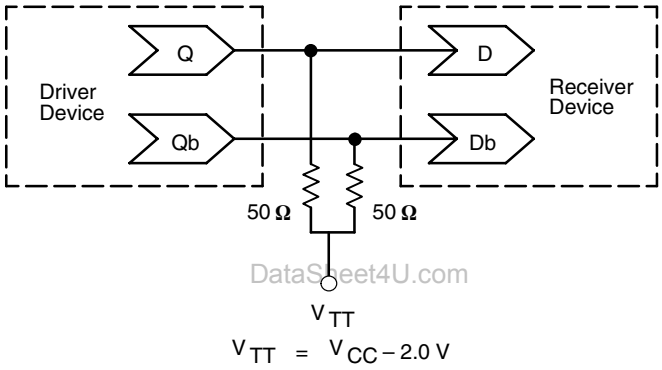


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405 – ECL Clock Distribution Techniques
AN1406 – Designing with PECL (ECL at +5.0 V)
AN1503 – ECLinPS I/O SPICE Modeling Kit
AN1504 – Metastability and the ECLinPS Family
AN1568 – Interfacing Between LVDS and ECL
AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650 – Using Wire–OR Ties in ECLinPS Designs
AN1672 – The ECL Translator Guide
AND8001 – Odd Number Counters Design
AND8002 – Marking and Date Codes
AND8020 – Termination of ECL Logic Devices

MC10E131, MC100E131

5V ECL 4-Bit D Flip-Flop

The MC10E/100E131 is a quad master-slave D-type flip-flop with differential outputs. Each flip-flop may be clocked separately by holding Common Clock (C_C) LOW and using the Clock Enable ($\overline{CE}$) inputs for clocking. Common clocking is achieved by holding the $\overline{CE}$ inputs LOW and using C_C to clock all four flip-flops. In this case, the $\overline{CE}$ inputs perform the function of controlling the common clock, to each flip-flop.

Individual asynchronous resets are provided (R). Asynchronous set controls (S) are ganged together in pairs, with the pairing chosen to reflect physical chip symmetry.

Data enters the master when both C_C and $\overline{CE}$ are LOW, and transfers to the slave when either C_C or $\overline{CE}$ (or both) go HIGH.

The 100 Series contains temperature compensation.

- 1100 MHz Min. Toggle Frequency
- Differential Outputs
- Individual and Common Clocks
- Individual Resets (asynchronous)
- Paired Sets (asynchronous)
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- Metastability Time Constant is 200 ps.
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- ESD Protection: > 2 KV HBM, > 200 V MM
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 240 devices

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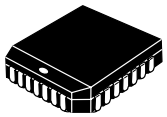
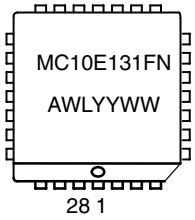


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAMS

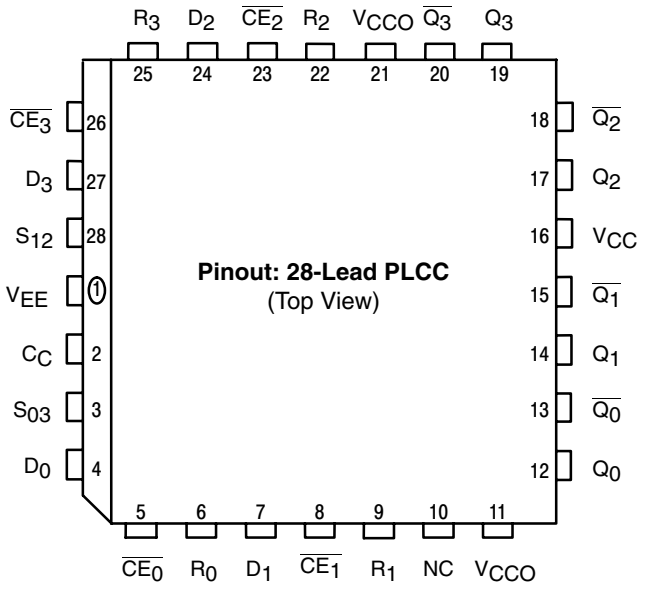


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E131FN	PLCC–28	37 Units/Rail
MC10E131FNR2	PLCC–28	500 Units/Reel
MC100E131FN	PLCC–28	37 Units/Rail
MC100E131FNR2	PLCC–28	500 Units/Reel

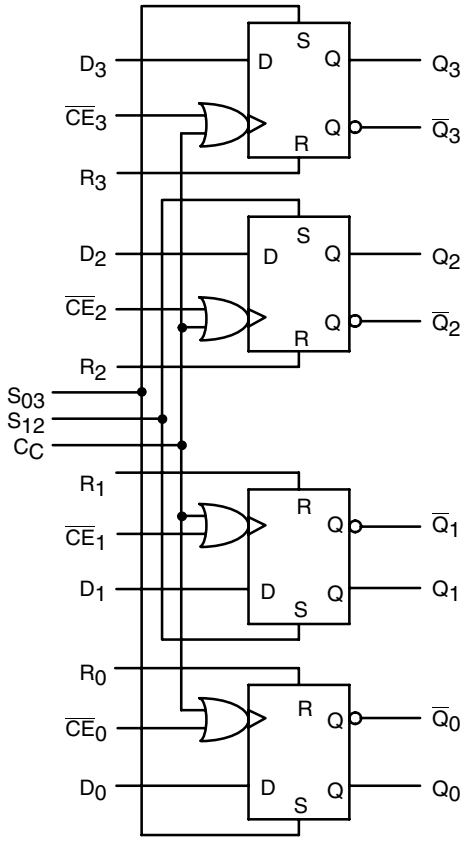
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN	FUNCTION
$D_0 - D_3$	ECL Data Inputs
$\overline{CE}_0 - \overline{CE}_3$	ECL Clock Enables (Individual)
$R_0 - R_3$	ECL Resets
C_C	ECL Common Clock
S_{03}, S_{12}	ECL Sets (paired)
$Q_0 - Q_3$, $\overline{Q}_0 - \overline{Q}_3$	ECL Differential Outputs
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		58	70		58	70		58	70	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current C_C S R, $\overline{CE}$ D			350 450 300 150			350 450 300 150			350 450 300 150	µA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		58	70		58	70		58	70	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current C_C S R, $\overline{CE}$ D			350 450 300 150			350 450 300 150			350 450 300 150	µA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		58	70		58	70		67	81	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current C_C S R, $\overline{CE}$ D			350 450 300 150			350 450 300 150			350 450 300 150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		58	70		58	70		67	81	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
I_{IH}	Input HIGH Current C_C S R, $\overline{CE}$ D			350 450 300 150			350 450 300 150			350 450 300 150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic		–40°C			25°C			85°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency			TBD			TBD			TBD		MHz
t_{PLH} t_{PHL}	Propagation Delay to Output	$\overline{CE}$	310	600	750	360	500	700	360	500	700	ps
		C_C	275	600	725	325	500	675	325	500	675	
		R	300	625	775	350	550	725	350	550	725	
		S	300	550	775	350	550	725	350	550	725	
t_S	Setup Time (Note 2.)	D	200	20		150	20		150	20		ps
t_H	Hold Time (Note 2.)	D	225	–20		175	–20		175	–20		ps
t_{RR}	Reset Recovery Time		450	150		400	150		400	150		ps
t_{PW}	Minimum Pulse Width	CLK	400			400			400			ps
		R, S	400			400			400			
t_{SKEW}	Within-Device Skew (Note 3.)			60			60			60		ps
t_{JITTER}	Cycle–to–Cycle Jitter			TBD			TBD			TBD		ps
t_r/t_f	Rise/Fall Time (20–80%)		275	460	725	300	480		300	480	675	ps

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Setup/hold times guaranteed for both C_C and $\overline{CE}$.
3. Within-device skew is defined as identical transitions on similar paths through a device.

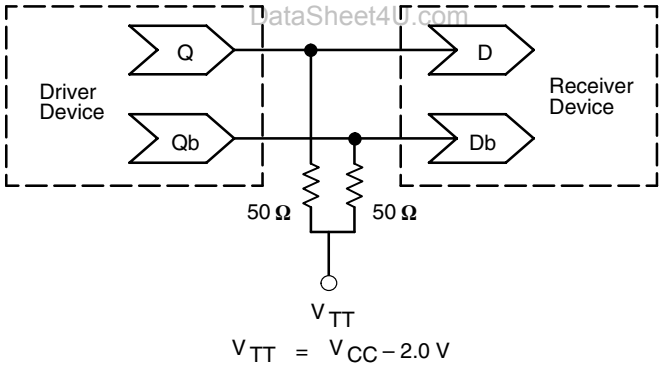


Figure 1. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E136, MC100E136

5V ECL 6-Bit Universal Up/Down Counter

The MC10E/100E136 is a 6-bit synchronous, presettable, cascadable universal counter. The device generates a look-ahead-carry output and accepts a look-ahead-carry input. These two features allow for the cascading of multiple E136's for wider bit width counters that operate at very nearly the same frequency as the stand alone counter.

The $\overline{\text{CLOUT}}$ output will pulse LOW for one clock cycle one count before the E136 reaches terminal count. The $\overline{\text{COUT}}$ output will pulse LOW for one clock cycle when the counter reaches terminal count. For more information on utilizing the look-ahead-carry features of the device please refer to the applications section of this data sheet. The differential COUT output facilitates the E136's use in programmable divider and self-stopping counter applications.

Unlike the H136 and other similar universal counter designs the E136 carry out and look-ahead-carry out signals are registered on chip.

This design alleviates the glitch problem seen on many counters where the carry out signals are merely gated. Because of this architecture there are some minor functional differences between the E136 and H136 counters. The user, regardless of familiarity with the H136, should read this data sheet carefully. Note specifically (see logic diagram) the operation of the carry out outputs and the look-ahead-carry in input when utilizing the master reset.

When left open all of the input pins will be pulled LOW via an input pulldown resistor. The master reset is an asynchronous signal which when asserted will force the Q outputs LOW.

The Q outputs need not be terminated for the E136 to function properly, in fact if these outputs will not be used in a system it is recommended to save power and minimize noise that they be left open. This practice will minimize switching noise which can reduce the maximum count frequency of the device or significantly reduce margins against other noise in the system.

The 100 Series contains temperature compensation.

- 550 MHz Count Frequency
- Fully Synchronous Up and Down Counting
- Look-Ahead-Carry Input and Output
- Asynchronous Master Reset
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 100 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8",
  Oxygen Index 28 to 34
- Transistor Count = 506 devices

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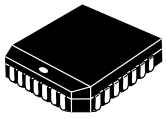
MARKING DIAGRAMS



PLCC–28
FN SUFFIX
CASE 776

28 1

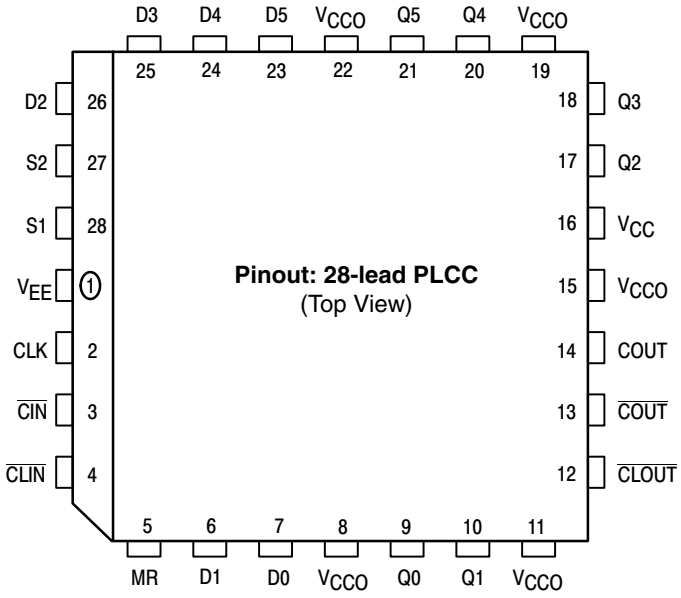
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

28 1

ORDERING INFORMATION

Device	Package	Shipping
MC10E136FN	PLCC–28	37 Units/Rail
MC10E136FNR2	PLCC–28	500 Units/Reel
MC100E136FN	PLCC–28	37 Units/Rail
MC100E136FNR2	PLCC–28	500 Units/Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

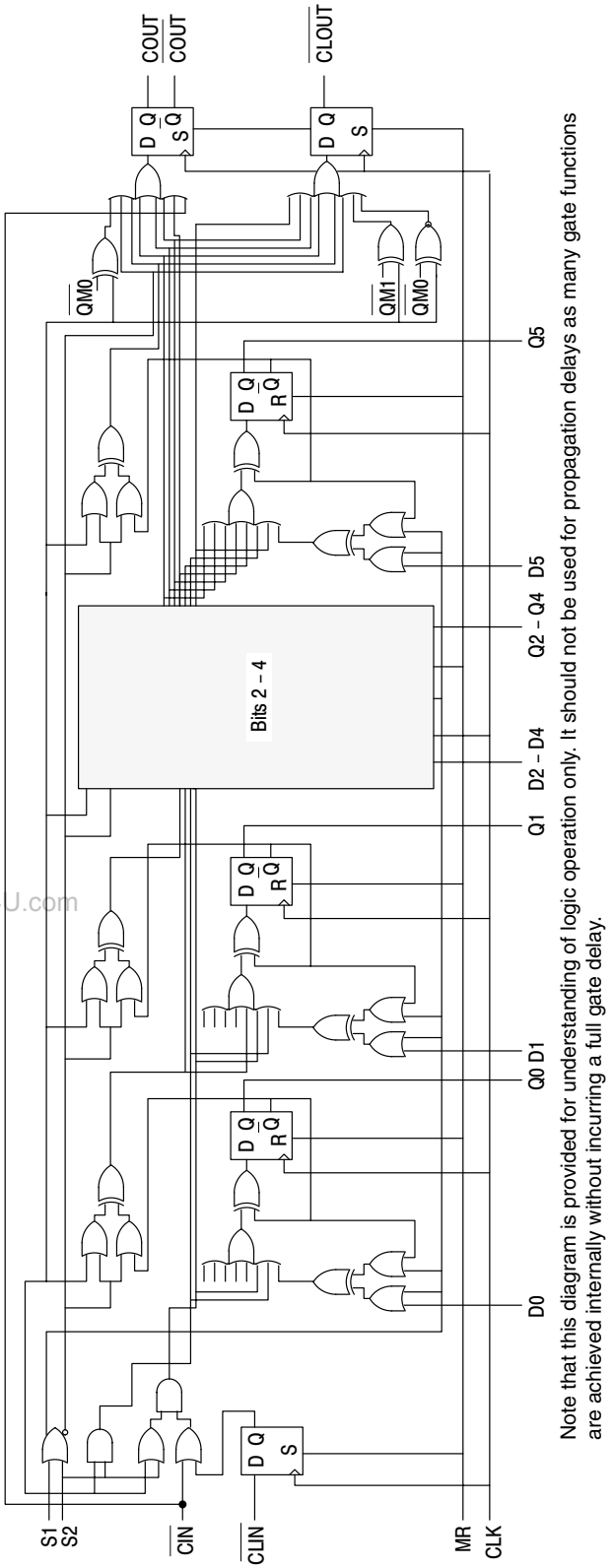
Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN NAMES

PIN	FUNCTION
$D_0 - D_5$	ECL Preset Data Inputs
$Q_0 - Q_5$	ECL Data Outputs
S1, S2	Mode Control Pins
MR	Master Reset
CLK	ECL Clock Input
$\overline{COUT}$, COUT	ECL Differential Carry-Out Output (Active LOW)
$\overline{CLOUT}$	ECL Look-Ahead-Carry Out (Active LOW)
$\overline{CIN}$	ECL Carry-In Input (Active LOW)
$\overline{CLIN}$	ECL Look-Ahead-Carry In Input (Active LOW)
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply

FUNCTION TABLE (Expanded truth table on page 67)

S1	S2	$\overline{CIN}$	MR	CLK	Function
L	L	X	L	Z	Preset Parallel Data
L	H	L	L	Z	Increment (Count Up)
L	H	H	L	Z	Hold Count
H	L	L	L	Z	Decrement (Count Down)
H	L	H	L	Z	Hold Count
H	H	X	L	Z	Hold Count
X	X	X	H	X	Reset (Qn = LOW)



Note that this diagram is provided for understanding of logic operation only. It should not be used for propagation delays as many gate functions are achieved internally without incurring a full gate delay.

E136 Universal Up/Down Counter Logic Diagram

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		125	150		125	150		125	150	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		125	150		125	150		125	150	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		125	150		125	150		140	170	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		125	150		125	150		140	170	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.

2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{COUNT}	Maximum Count Frequency	550	650	—	550	650	—	550	650	—	MHz
t_{PLH} t_{PHL}	Propagation Delay to Output										ps
	CLK to Q	850	1150	1450	850	1150	1450	850	1150	1450	
	MR to Q	850	1150	1450	850	1150	1450	850	1150	1450	
	CLK to $\overline{COUT}$	800	1150	1300	800	1150	1300	800	1150	1300	
	CLK to $\overline{CLOUT}$	825	1150	1400	825	1150	1400	825	1150	1400	
t_s	Setup Time										ps
	S1, S2	1000	650	—	1000	650	—	1000	650	—	
	D	800	400	—	800	400	—	800	400	—	
	$\overline{CLIN}$	150	0	—	150	0	—	150	0	—	
	$\overline{CIN}$	800	400	—	800	400	—	800	400	—	
t_h	Hold Time										ps
	S1, S2	150	–200	—	150	–200	—	150	–200	—	
	D	150	–250	—	150	–250	—	150	–250	—	
	$\overline{CLIN}$	300	0	—	300	0	—	300	0	—	
	$\overline{CIN}$	150	–250	—	150	–250	—	150	–250	—	
t_{RR}	Reset Recovery Time	1000	700	—	1000	700	—	1000	700	—	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_{PW}	Minimum Pulse Width										ps
	CLK, MR	700	400	—	700	400	—	700	400	—	
t_r t_f	Rise/Fall Times 20% - 80%										ps
	$\overline{COUT}$	275	—	600	275	—	600	275	—	600	
	Other	300	—	700	300	—	700	300	—	700	

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.

EXPANDED TRUTH TABLE

Function	S1	S2	MR	$\overline{CIN}$	$\overline{CLIN}$	CLK	D5	D4	D3	D2	D1	D0	Q5	Q4	Q3	Q2	Q1	Q0	$\overline{COUT}$	$\overline{CLOUT}$
Preset	L	L	L	X	X	Z	L	L	L	L	H	H	L	L	L	L	H	H	H	H
Down	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	H	L	H	H
	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	H	H	L
	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	L	H
	H	L	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	H	H	H
Preset	L	L	L	X	X	Z	H	H	H	H	L	L	H	H	H	H	L	L	H	H
Up	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	L	H	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	L	H	L
	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	H	L	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	H	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	H	L	H	H
Hold	H	H	L	X	X	Z	X	X	X	X	X	X	L	L	L	L	H	L	H	H
	H	H	L	X	X	Z	X	X	X	X	X	X	L	L	L	L	H	L	H	H
Down	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	H	H	L
Hold	H	L	L	H	L	Z	X	X	X	X	X	X	L	L	L	L	L	H	H	H
Down	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	L	H
Hold	H	L	L	H	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	H	H
	H	L	L	H	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	H	H
	H	L	L	H	H	Z	X	X	X	X	X	X	L	L	L	L	L	L	H	H
Hold	H	L	L	L	H	Z	X	X	X	X	X	X	L	L	L	L	L	L	L	H
	H	L	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	L	H
Hold	H	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	L	H
Preset	L	L	L	X	X	Z	H	H	H	H	L	L	H	H	H	H	L	L	H	H
Up	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	L	H	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	L	H	L
Hold	L	H	L	H	L	Z	X	X	X	X	X	X	H	H	H	H	H	L	H	H
Up	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	H	L	H
Hold	L	H	L	H	L	Z	X	X	X	X	X	X	H	H	H	H	H	H	H	H
	L	H	L	H	H	Z	X	X	X	X	X	X	H	H	H	H	H	H	H	H
Hold	L	H	L	L	L	Z	X	X	X	X	X	X	H	H	H	H	H	H	L	H
Up	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	L	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	L	H	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	H	L	H	H
	L	H	L	L	L	Z	X	X	X	X	X	X	L	L	L	L	H	H	H	H
Reset	X	X	H	X	X	X	X	X	X	X	X	X	L	L	L	L	L	L	H	H

Z = Low to High Transition

APPLICATIONS INFORMATION

Overview

The MC10E/100E136 is a 6-bit synchronous, presettable, cascadable universal counter. Using the S1 and S2 control pins the user can select between preset, count up, count down and hold count. The master reset pin will reset the internal counter, and set the $\overline{\text{COUT}}$, $\overline{\text{CLOUT}}$, and $\overline{\text{CLIN}}$ flip-flops. Unlike previous 136 type counters the carry out outputs will go to a high state during the preset operation. In addition since the carry out outputs are registered they will not go low if terminal count is loaded into the register. The look-ahead-carry out output functions similarly.

Note from the schematic the use of the master information from the least significant bits for control of the two carry out functions. This architecture not only reduces the carry out delay, but is essential to incorporate the registered carry out functions. In addition to being faster, because these functions are registered the resulting carry out signals are stable and glitch free.

Cascading Multiple E136 Devices

Many applications require counters significantly larger than the 6 bits available with the E136. For these applications several E136 devices can be cascaded to increase the bit width of the counter to meet the needs of the application.

In the past cascading several 136 type universal counters necessarily impacted the maximum count frequency of the resulting counter chain. This performance impact was the result of the terminal count signal of the lower order counters having to ripple through the entire counter chain. As a result past counters of this type were not widely used in large bit counter applications.

An alternative counter architecture similar to the E016 binary counter was implemented to alleviate the need to ripple propagate the terminal count signal. Unfortunately these types of counters require external gating for cascading designs of more than two devices. In addition to requiring additional components, these external gates limit the cascaded count frequency to a value less than the free running count frequency of a single counter. Although there is a performance impact with this type of architecture it is minor compared to the impact of the ripple propagate designs. As a result the E016 type counters have been used extensively in applications requiring very high speed, wide bit width synchronous counters.

ON Semiconductor has incorporated several improvements to past universal counter designs in the E136 universal counter. These enhancements make the E136 the unparalleled leader in its class. With the addition of look-ahead-carry features on the terminal count signal, very large counter chains can be designed which function at very nearly the same clock frequency as a single free running device. More importantly these counter chains require no external gating. Figure 1 below illustrates the interconnect scheme for using the look-ahead-carry features of the E136 counter.

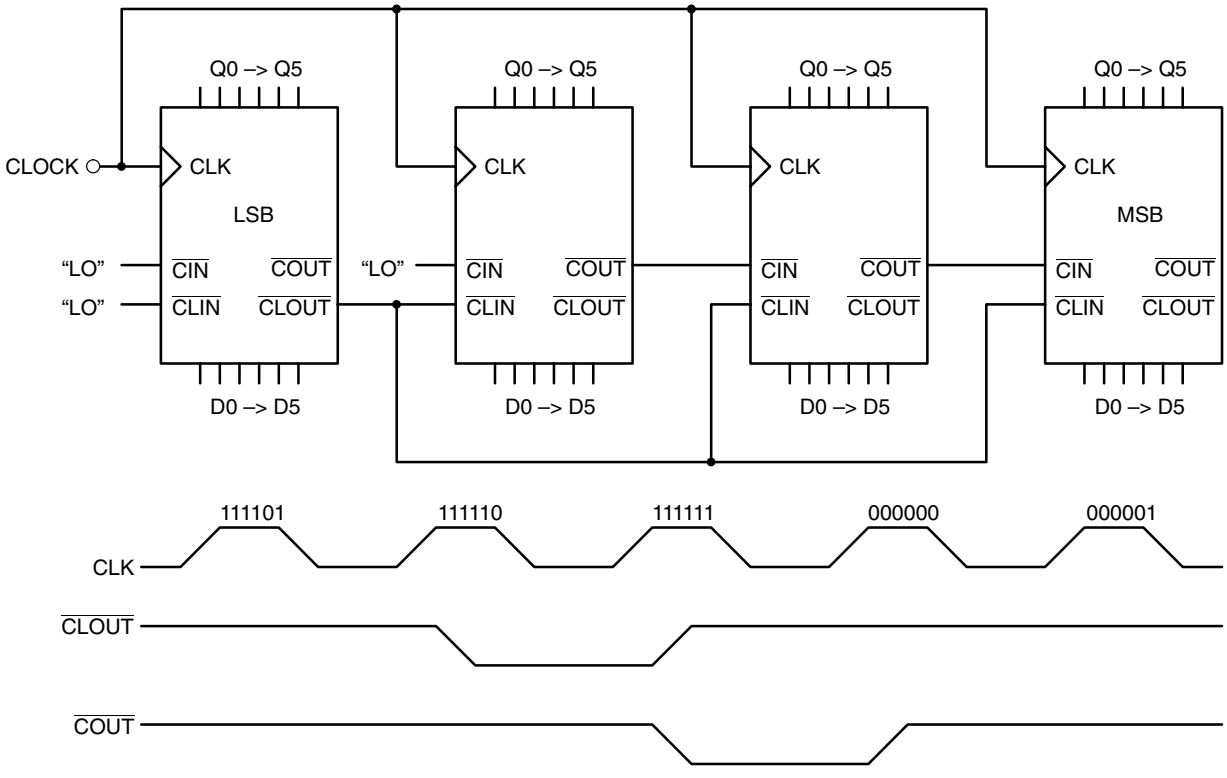


Figure 1. 24-bit Cascaded E136 Counter

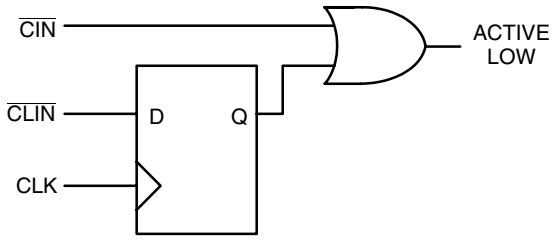


Figure 2. Look-Ahead-Carry Input Structure

Note from the waveforms that the look-ahead-carry output ($\overline{\text{CLOUT}}$) pulses low one clock pulse before the counter reaches terminal count. Also note that both $\overline{\text{CLOUT}}$ and the carry out pin ($\overline{\text{COUT}}$) of the device pulse low for only one clock period. The input structure for look-ahead-carry in ($\overline{\text{CLIN}}$) and carry in ($\overline{\text{CIN}}$) is pictured in Figure 2.

The $\overline{\text{CLIN}}$ input is registered and then ORed with the $\overline{\text{CIN}}$ input. From the truth table one can see that both the $\overline{\text{CIN}}$ and the $\overline{\text{CLIN}}$ inputs must be in a LOW state for the E136 to be enabled to count (either count up or count down). The $\overline{\text{CLIN}}$ inputs are driven by the $\overline{\text{CLOUT}}$ output of the lowest order E136 and therefore are only asserted for a single clock period. Since the $\overline{\text{CLIN}}$ input is registered it must be asserted one clock period prior to the $\overline{\text{CIN}}$ input.

If the counter previous to a given counter is at terminal count its $\overline{\text{COUT}}$ output and thus the $\overline{\text{CIN}}$ input of the given counter will be in the "LOW" state. This signals the given counter that it will need to count one upon the next terminal count of the least significant counter (LSC). The $\overline{\text{CLOUT}}$ output of the LSC will pulse low one clock period before it reaches terminal count. This $\overline{\text{CLOUT}}$ signal will be clocked into the $\overline{\text{CLIN}}$ input of the higher order counters on the following positive clock transition. Since both $\overline{\text{CIN}}$ and $\overline{\text{CLIN}}$ are in the LOW state the next clock pulse will cause the least significant counter to roll over and all higher order counters, if signaled by their $\overline{\text{CIN}}$ inputs, to count by one.

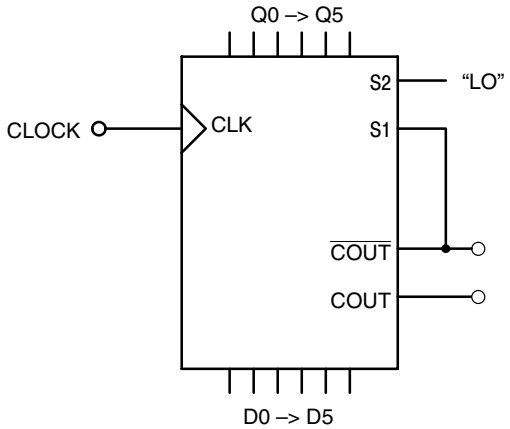


Figure 3. 6-bit Programmable Divider

During the clock pulse in which the higher order counter is counting by one the $\overline{\text{CLIN}}$ is clocking in the high signal presented by the $\overline{\text{CLOUT}}$ of the LSC. The $\overline{\text{CIN}}$'s in the higher order counter will ripple propagate through the chain to update the count status for the next occurrence of terminal count on the LSC. This ripple propagation will not affect the count frequency as it has 2^6–1 or 63 clock pulses to ripple through without affecting the count operation of the chain.

The only limiting factor which could reduce the count frequency of the chain as compared to a free running single device will be the setup time of the $\overline{\text{CLIN}}$ input. This limit will consist of the CLK to $\overline{\text{CLOUT}}$ delay of the E136 plus the $\overline{\text{CLIN}}$ setup time plus any path length differences between the $\overline{\text{CLOUT}}$ output and the clock.

Programmable Divider

Using external feedback of the $\overline{\text{COUT}}$ pin, the E136 can be configured as a programmable divider. Figure 3 illustrates the configuration for a 6-bit count down programmable divider. If for some reason a count up divider is preferred the $\overline{\text{COUT}}$ signal is simply fed back to S2 rather than S1. Examination of the truth table for the E136 shows that when both S1 and S2 are LOW the counter will parallel load on the next positive transition of the clock. If the S2 input is low and the S1 input is high the counter will be in the count down mode and will count towards an all zero state upon successive clock pulses. Knowing this and the operation of the $\overline{\text{COUT}}$ output it becomes a trivial matter to build programmable dividers.

For a programmable divider one wants to load a predesignated number into the counter and count to terminal count. Upon terminal count the counter should automatically reload the divide number. With the architecture shown in Figure 3 when the counter reaches terminal count the $\overline{\text{COUT}}$ output and thus the S1 input will go LOW, this combined with the low on S2 will cause the counter to load the inputs present on D0-D5. Upon loading the divide value into the counter $\overline{\text{COUT}}$ will go HIGH as the counter is no longer at terminal count thereby placing the counter back into the count mode.

Table 1. Preset Inputs Versus Divide Ratio

Divide Ratio	Preset Data Inputs					
	D5	D4	D3	D2	D1	D0
2	L	L	L	L	L	H
3	L	L	L	L	H	L
4	L	L	L	L	H	H
5	L	L	L	H	L	L
•	•	•	•	•	•	•
•	•	•	•	•	•	•
36	H	L	L	L	H	H
37	H	L	L	H	L	L
38	H	L	L	H	L	H
•	•	•	•	•	•	•
•	•	•	•	•	•	•
62	H	H	H	H	L	H
63	H	H	H	H	H	L
64	H	H	H	H	H	H

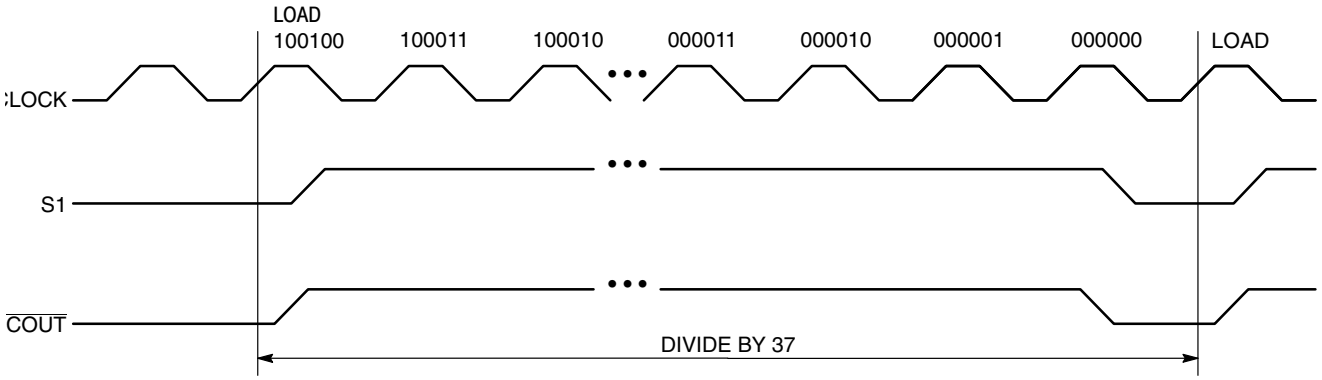


Figure 4. Programmable Divider Waveforms

The exercise of building a programmable divider then becomes simply determining what value to load into the counter to accomplish the desired division. Since the load operation requires a clock pulse, to divide by N, N–1 must be loaded into the counter. A single E136 device is capable of divide ratios of 2 to 64 inclusive, Table 1 outlines the load values for the various divide ratios. Figure 4 presents the waveforms resulting from a divide by 37 operation. Note that the availability of the COUT complimentary output $\overline{\text{COUT}}$ allows the user to choose the polarity of the divide by output.

For single device programmable counters the E016 counter is probably a better choice than the E136. The E016 has an internal feedback to control the reloading of the counter, this not only simplifies board design but also will result in a faster maximum count frequency.

For programmable dividers of larger than 8 bits the superiority of the E016 diminishes, and in fact for very wide dividers the E136 will provide the capability of a faster count frequency. This potential is a result of the cascading features mentioned previously in this document. Figure 5 shows the architecture of a 24-bit programmable divider implemented using E136 counters. Note the need for one external gate to control the loading of the entire counter chain. An ideal device for the external gating of this architecture would be the 4-input OR function in the 8-lead SOIC ECLinPS Lite™ family. However the final decision as to what device to use for the external gating requires a balancing of performance needs, cost and available board space. Note that because of the need for external gating the maximum count frequency of a given sized programmable divider will be less than that of a single cascaded counter.

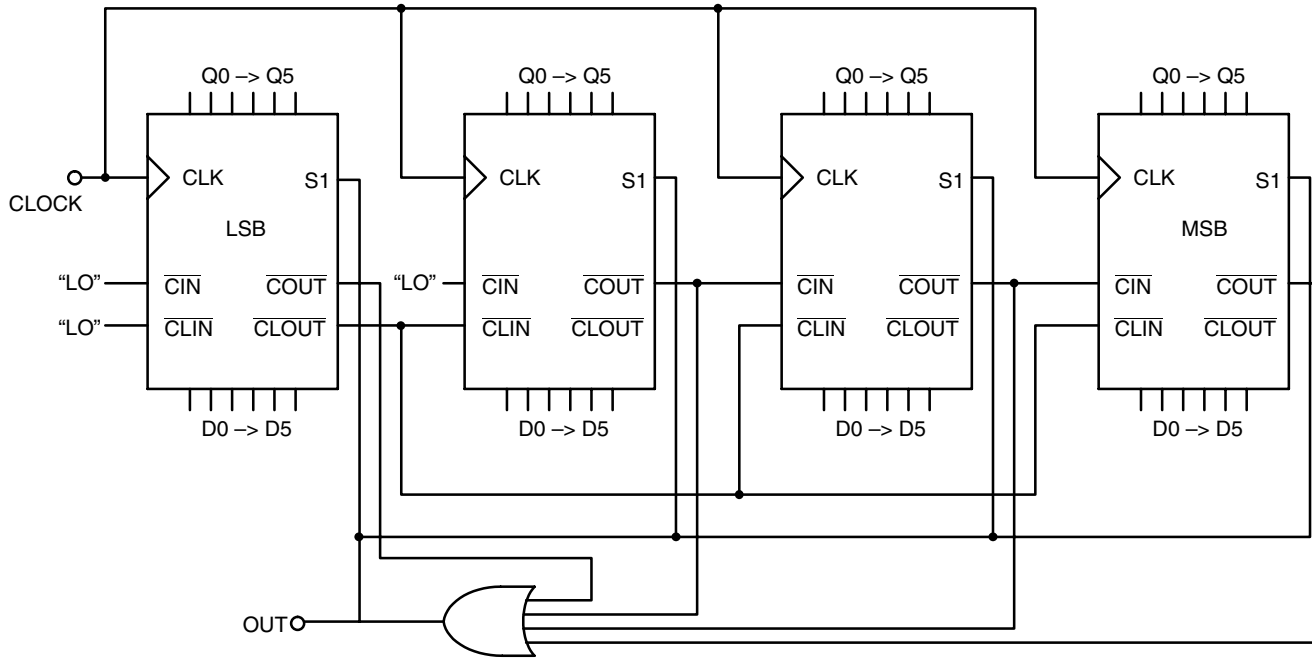


Figure 5. 24-bit Programmable Divider Architecture

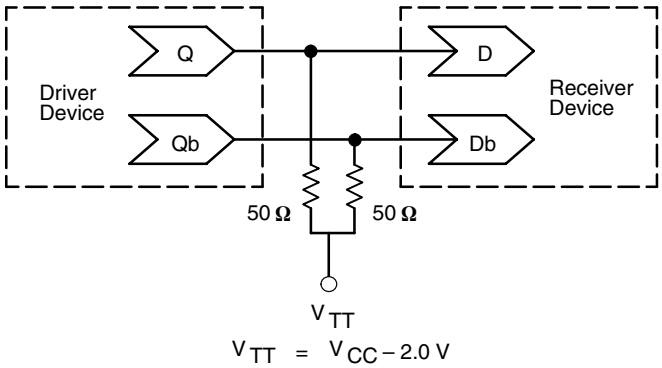


Figure 6. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E137, MC100E137

5V ECL 8-Bit Ripple Counter

The MC10E/100E137 is a very high speed binary ripple counter. The two least significant bits were designed with very fast edge rates while the more significant bits maintain standard ECLinPS™ output edge rates. This allows the counter to operate at very high frequencies while maintaining a moderate power dissipation level.

The device is ideally suited for multiple frequency clock generation as well as a counter in a high performance ATE time measurement board.

Both asynchronous and synchronous enables are available to maximize the device's flexibility for various applications. The asynchronous enable input, A_Start, when asserted enables the counter while overriding any synchronous enable signals. The E137 features XORed enable inputs, EN1 and EN2, which are synchronous to the CLK input. When only one synchronous enable is asserted the counter becomes disabled on the next CLK transition; all outputs remain in the previous state poised for the other synchronous enable or A_Start to be asserted to re-enable the counter. Asserting both synchronous enables causes the counter to become enabled on the next transition of the CLK. If EN1 (or EN2) and CLK edges are coincident, sufficient delay has been inserted in the CLK path (to compensate for the XOR gate delay and the internal D-flip flop setup time) to insure that the synchronous enable signal is clocked correctly, hence, the counter is disabled.

All input pins left open will be pulled LOW via an input pulldown resistor. Therefore, do not leave the differential CLK inputs open. Doing so causes the current source transistor of the input clock gate to become saturated, thus upsetting the internal bias regulators and jeopardizing the stability of the device.

The asynchronous Master Reset resets the counter to an all zero state upon assertion.

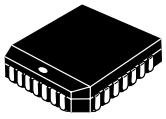
The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

- Differential Clock Input and Data Output Pins
- V_{BB} Output for Single-Ended Use
- Synchronous and Asynchronous Enable Pins
- Asynchronous Master Reset
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 100 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8",
  Oxygen Index 28 to 34
- Transistor Count = 330 devices

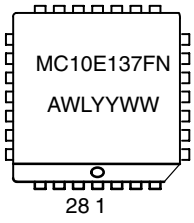
ON Semiconductor™

http://onsemi.com



PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAMS



28 1

28 1

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

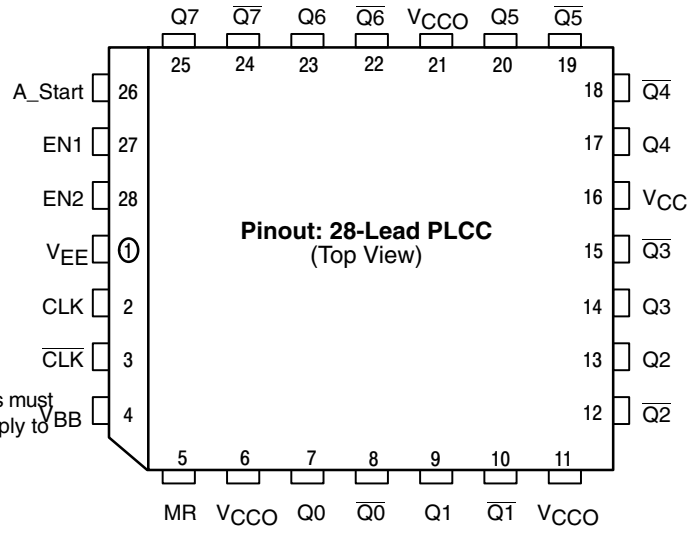
Device	Package	Shipping
MC10E137FN	PLCC–28	37 Units/Rail
MC10E137FNR2	PLCC–28	500 Units/Reel
MC100E137FN	PLCC–28	37 Units/Rail
MC100E137FNR2	PLCC–28	500 Units/Reel

PIN DESCRIPTION

PIN	FUNCTION
CLK, $\overline{CLK}$	ECL Differential Clock Inputs
Q0-Q7, $\overline{Q0}$-$\overline{Q7}$	ECL Differential Q Outputs
A_Start	ECL Asynchronous Enable Input
EN1, EN2	ECL Synchronous Enable Inputs
MR	Asynchronous Master Reset
V_{BB}	Reference Voltage Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply

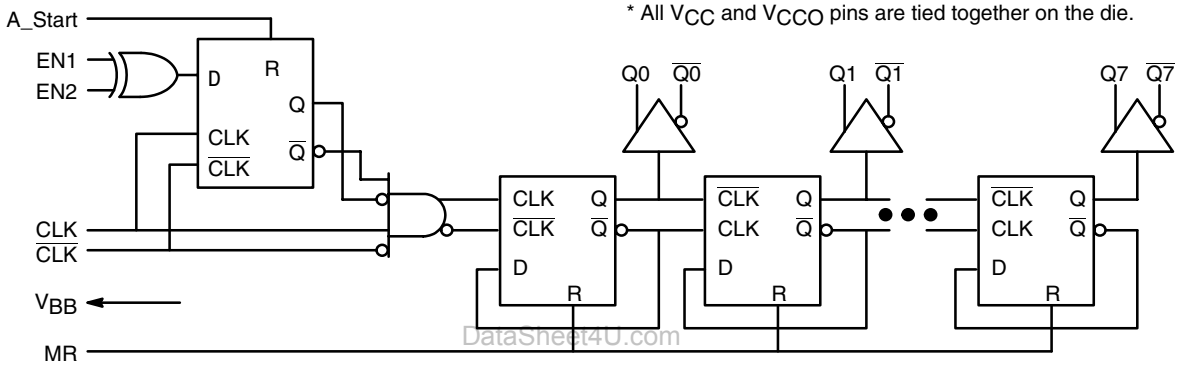
Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

LOGIC DIAGRAM



SEQUENTIAL TRUTH TABLE

Function	EN1	EN2	A_Start	MR	CLK	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
Reset	X	X	X	H	X	L	L	L	L	L	L	L	L
Count	L	L	L	L	Z	L	L	L	L	L	L	L	H
	L	L	L	L	Z	L	L	L	L	L	L	H	L
	L	L	L	L	Z	L	L	L	L	L	L	H	H
Stop	H	L	L	L	Z	L	L	L	L	L	L	H	H
	H	L	L	L	Z	L	L	L	L	L	L	H	H
Asynch Start	H	L	H	L	Z	L	L	L	L	L	H	L	L
	H	L	H	L	Z	L	L	L	L	L	H	L	H
	L	L	H	L	Z	L	L	L	L	L	H	H	L
Count	L	L	L	L	Z	L	L	L	L	L	H	H	H
	L	L	L	L	Z	L	L	L	L	H	L	L	L
	L	L	L	L	Z	L	L	L	L	H	L	L	H
Stop	L	H	L	L	Z	L	L	L	L	H	L	L	H
	L	H	L	L	Z	L	L	L	L	H	L	L	H
Synch Start	H	H	L	L	Z	L	L	L	L	H	L	H	L
	H	H	L	L	Z	L	L	L	L	H	L	H	H
	H	H	L	L	Z	L	L	L	L	H	H	L	L
Stop	H	L	L	L	Z	L	L	L	L	H	H	L	L
	H	L	L	L	Z	L	L	L	L	H	H	L	L
Count	L	L	L	L	Z	L	L	L	L	H	H	L	H
	L	L	L	L	Z	L	L	L	L	H	H	H	L
	L	L	L	L	Z	L	L	L	L	H	H	H	H
Reset	X	X	X	H	X	L	L	L	L	L	L	L	L

Z = Low to High Transition

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		121	145		121	145		121	145	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage (Single Ended)	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
V_{BB}	Output Voltage Reference	3.62		3.73	3.65		3.75	3.69		3.81	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.2		4.6	2.2		4.6	2.2		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		121	145		121	145		121	145	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
V_{BB}	Output Voltage Reference	–1.38		–1.27	–1.35		–1.25	–1.31		–1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.8		–0.4	–2.8		–0.4	–2.8		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		121	145		121	145		139	167	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
V_{BB}	Output Voltage Reference	3.62		3.73	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.2		4.6	2.2		4.6	2.2		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		121	145		121	145		139	167	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.27	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–3.8		–0.4	–3.8		–0.4	–3.8		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{COUNT}	Maximum Count Frequency	1800	2200		1800	2200		1800	2200		MHz
t_{PLH} t_{PHL}	Propagation Delay to Output										ps
	CLK to Q0	1300	1700	2150	1300	1700	2150	1350	1750	2200	
	CLK to Q1	1600	2025	2500	1600	2050	2500	1650	2100	2550	
	CLK to Q2	1950	2425	2925	1950	2450	2925	2025	2500	3000	
	CLK to Q3	2275	2750	3350	2275	2775	3350	2350	2850	3425	
	CLK to Q4	2625	3125	3750	2625	3150	3750	2700	3225	3825	
	CLK to Q5	2950	3450	4150	2950	3475	4150	3050	3550	4250	
	CLK to Q6	3250	3775	4450	3250	3800	4450	3375	3925	4600	
	CLK to Q7	3575	4075	4800	3575	4125	4800	3700	4250	4950	
	A_Start to Q0	950	1325	1700	950	1325	1700	950	1325	1700	
	MR to Q0	700	1000	1300	700	1000	1300	700	1000	1300	
t_s	Setup Time (EN1, EN2)	0	–150		0	–150		0	–150		ps
t_h	Hold Time (EN1, EN2)	300	150		300	150		300	150		ps
t_{RR}	Reset Recovery Time										ps
	MR, A_Start	400	200		400	200		400	200		
t_{PW}	Minimum Pulse Width										ps
	CLK, MR, A_Start	400			400			400			
V_{PP}	Minimum Input Swing (CLK) (Note 2.)	0.25		1.0	0.25		1.0	0.25		1.0	V
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Rise/Fall Times (20%–80%)										ps
	Q0,Q1	150		400	150		400	150		400	
	Q2 to Q7	275		600	275		600	275		600	

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Minimum input swing for which AC parameters are guaranteed. Full DC ECL output swings will be generated with only 50 mV input swings.

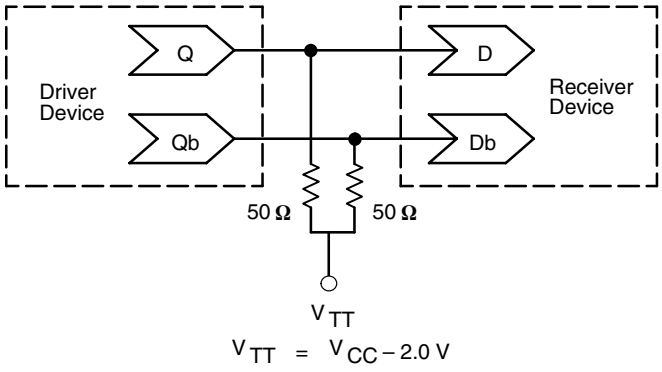


Figure 1. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E141, MC100E141

5V ECL 8-Bit Shift Register

The MC10E/100E141 is an 8-bit full-function shift register. The E141 performs serial/parallel in and serial/parallel out, shifting in either direction. The eight inputs $D_0 - D_7$ accept parallel input data, while DL/DR accept serial input data for left/right shifting. The Qn outputs do not need to be terminated for the shift operation to function. To minimize noise and power, any Q output not used should be left unterminated.

The select pins, SEL0 and SEL1, select one of four modes of operation: Load, Hold, Shift Left, Shift Right, according to the Function Table.

Input data is accepted a set-up time before the positive clock edge. A HIGH on the Master Reset (MR) pin asynchronously resets all the registers to zero.

The 100 Series contains temperature compensation.

- 700 MHz Min. Shift Frequency
- 8-Bit
- Full-Function, Bi-Directional
- Asynchronous Master Reset
- Pin-Compatible with E241
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 200 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 565 devices

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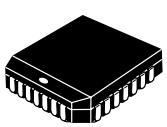
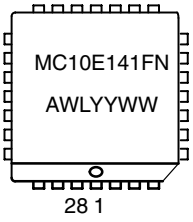
MARKING DIAGRAMS



PLCC–28
FN SUFFIX
CASE 776



28 1

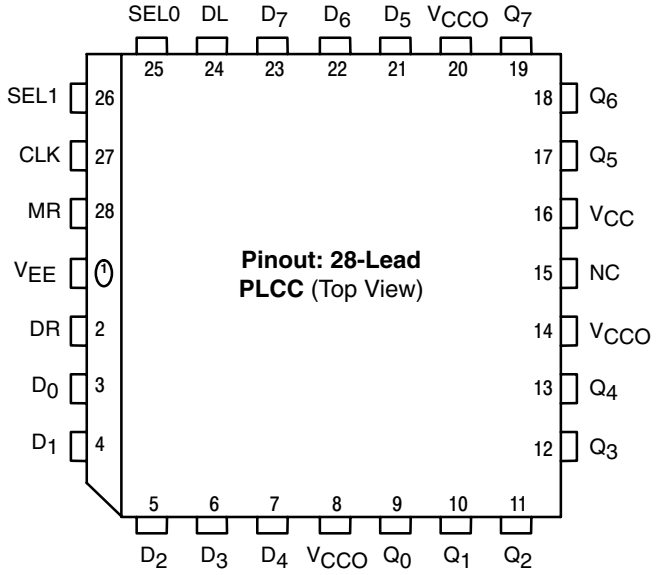
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

28 1

ORDERING INFORMATION

Device	Package	Shipping
MC10E141FN	PLCC–28	37 Units/Rail
MC10E141FNR2	PLCC–28	500 Units/Reel
MC100E141FN	PLCC–28	37 Units/Rail
MC100E141FNR2	PLCC–28	500 Units/Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



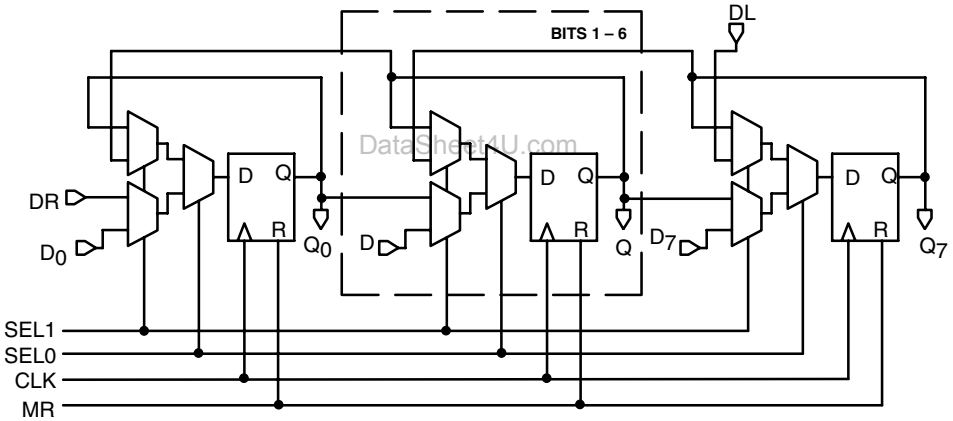
* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

PIN	FUNCTION
$D_0 – D_7$	ECL Parallel Data Inputs
DL, DR	ECL Serial Data Inputs
SEL0, SEL1	ECL Mode Select In Inputs
CLK	ECL Clock
$Q_0 – Q_7$	ECL Data Outputs
MR	ECL Master Reset
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

LOGIC DIAGRAM



FUNCTION TABLE

SEL0	SEL1	Function
L	L	Load
L	H	Shift Right (D_n to D_{n+1})
H	L	Shift Left (D_n to D_{n-1})
H	H	Hold

EXPANDED FUNCTION TABLE

Function	DL	DR	SEL0	SEL1	MR	CLK	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Load	X	X	L	L	L	Z	D0	D1	D2	D3	D4	D5	D6	D7
Shift Right	X	L	L	H	L	Z	L	Q0	Q1	Q2	Q3	Q4	Q5	Q6
	X	H	L	H	L	Z	H	L	Q0	Q1	Q2	Q3	Q4	Q5
Shift Left	L	X	H	L	L	Z	L	Q0	Q1	Q2	Q3	Q4	Q5	L
	H	X	H	L	L	Z	Q0	Q1	Q2	Q3	Q4	Q5	L	H
Hold	X	X	H	H	L	Z	Q0	Q1	Q2	Q3	Q4	Q5	L	H
	X	X	H	H	L	Z	Q0	Q1	Q2	Q3	Q4	Q5	L	H
Reset	X	X	X	X	H	X	L	L	L	L	L	L	L	L

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		131	181		131	181		131	181	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		131	181		131	181		131	181	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		131	181		131	181		151	181	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		131	181		131	181		151	181	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{SHIFT}	Max. Shift Frequency	700	900		700	900		700	900		MHz
t_{PLH} / t_{PHL}	Propagation Delay To Output										ps
	Clk	625	750	975	625	750	975	625	750	975	
	MR	600	725	975	600	725	975	600	725	975	
t_s	Setup Time										ps
	D	175	25		175	25		175	25		
	SEL0	350	200		350	200		350	200		
	SEL1	300	150		300	150		300	150		
t_h	Hold Time										ps
	D	200	– 25		200	– 25		200	– 25		
	SEL0	100	– 200		100	– 200		100	– 200		
	SEL1	100	–150		100	–150		100	–150		
t_{RR}	Reset Recovery Time	900	700		900	700		900	700		ps
t_{PW}	Minimum Pulse Width										ps
	Clk, MR	400			400			400			
t_{SKEW}	Within-Device Skew (Note 2.)		60			60			60		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r / t_f	Rise/Fall Times										ps
	(20 - 80%)	300	525	800	300	525	800	300	525	800	

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.

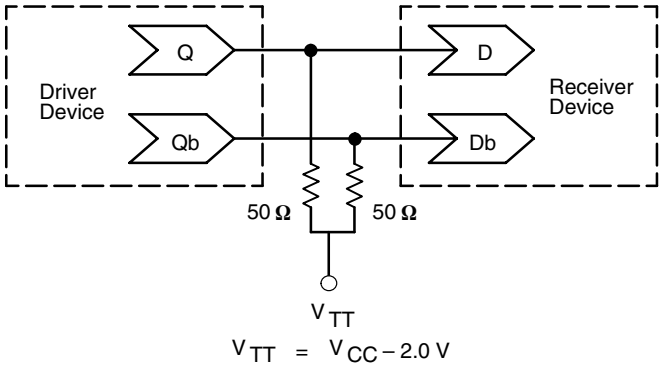


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
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AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E142, MC100E142

5V ECL 9-Bit Shift Register

The MC10E/100E142 is a 9-bit shift register, designed with byte-parity applications in mind. The E142 performs serial/parallel in and serial/parallel out, shifting in one direction. The nine inputs D0 – D8 accept parallel input data, while S-IN accepts serial input data. The Qn outputs do not need to be terminated for the shift operation to function. To minimize noise and power, any Q output not used should be left unterminated.

The SEL (Select) input pin is used to switch between the two modes of operation — SHIFT and LOAD. The shift direction is from bit 0 to bit 8. Input data is accepted by the registers a set-up time before the positive going edge of CLK1 or CLK2; shifting is also accomplished on the positive clock edge. A HIGH on the Master Reset pin (MR) asynchronously resets all the resisters to zero.

The 100 Series contains temperature compensation.

- 700 MHz Min. Shift Frequency
- 9-Bit for Byte-Parity Applications
- Asynchronous Master Reset
- Dual Clocks
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 200 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 405 devices

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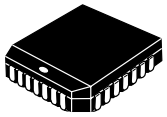
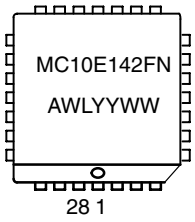
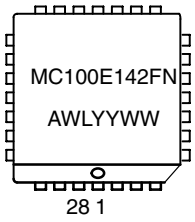
MARKING DIAGRAMS



PLCC–28
FN SUFFIX
CASE 776



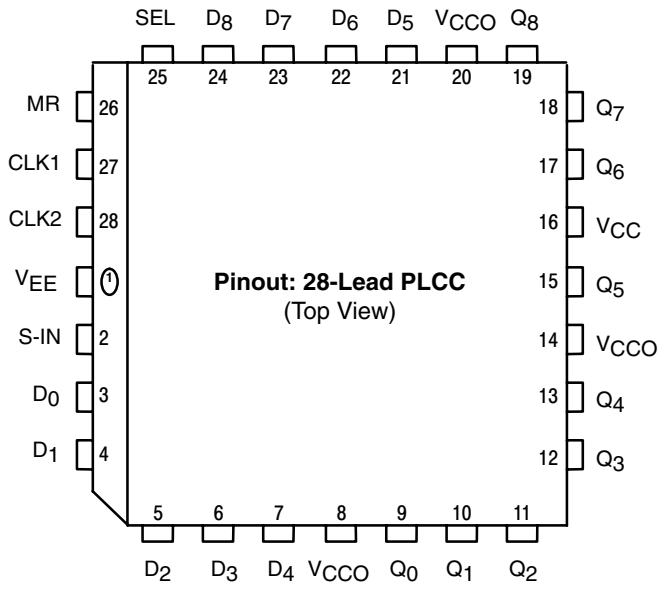
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week



ORDERING INFORMATION

Device	Package	Shipping
MC10E142FN	PLCC–28	37 Units/Rail
MC10E142FNR2	PLCC–28	500 Units/Reel
MC100E142FN	PLCC–28	37 Units/Rail
MC100E142FNR2	PLCC–28	500 Units/Reel

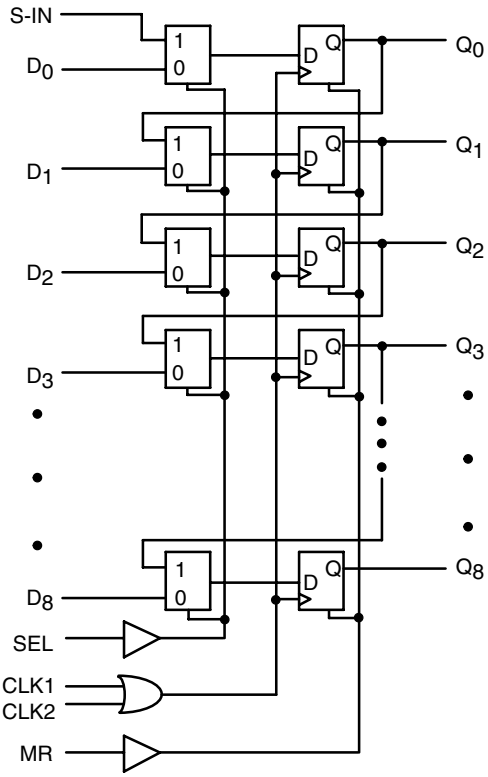
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN	FUNCTION
$D_0 - D_8$	ECL Parallel Data Inputs
S-IN	ECL Serial Data Input
SEL	ECL Mode Select Input
CLK1, CLK2	ECL Clock Inputs
MR	ECL Master Reset
$Q_0 - Q_8$	ECL Data Outputs
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply

FUNCTIONS

SEL	Mode
L H	Load Shift

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		120	145		120	145		120	145	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		120	145		120	145		120	145	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		120	145		120	145		138	165	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		120	145		120	145		138	165	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
f_{SHIFT}	Max. Shift Frequency	700	900		700	900		700	900		MHz
t_{PLH}	Propagation Delay to Output										ps
t_{PHL}	Clk	600	800	1000	600	800	1000	600	800	1000	
	MR	600	800	1000	600	800	1000	600	800	1000	
t_s	Setup Time										ps
	D	50	–100		50	–100		50	–100		
	SEL	300	150		300	150		300	150		
t_h	Hold Time										ps
	D	300	100		300	100		300	100		
	SEL	75	–150		75	–150		75	–150		
t_{RR}	Reset Recovery Time	900	700		900	700		900	700		ps
t_{PW}	Minimum Pulse Width										ps
	Clk, MR	400			400			400			
t_{SKEW}	Within-Device Skew (Note 2.)		75			75			75		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r	Rise/Fall Times										ps
t_f	(20 - 80%)	300	525	800	300	525	800	300	525	800	

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.

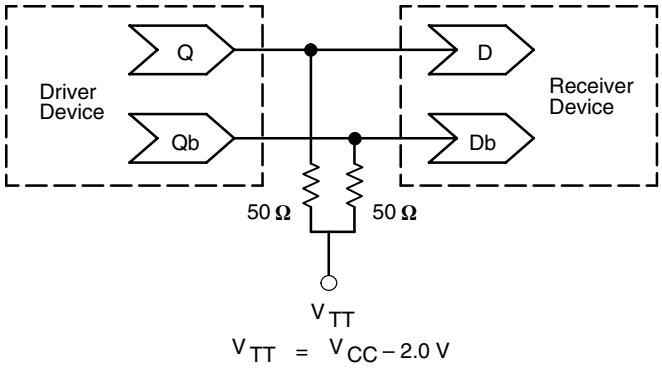


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E143, MC100E143

5V ECL 9-Bit Hold Register

The MC10E/100E143 is a 9-bit holding register, designed with byte-parity applications in mind. The E143 holds current data or loads new data, with the nine inputs D0 – D8 accepting parallel input data.

The SEL (Select) input pin is used to switch between the two modes of operation — HOLD and LOAD. Input data is accepted by the registers a set-up time before the positive going edge of CLK1 or CLK2. A HIGH on the Master Reset pin (MR) asynchronously resets all the registers to zero.

The 100 Series contains temperature compensation.

- 700 MHz Min. Operating Frequency
- 9-Bit for Byte-Parity Applications
- Asynchronous Master Reset
- Dual Clocks
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 200 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 484 devices

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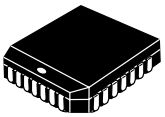
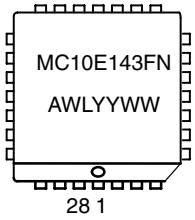
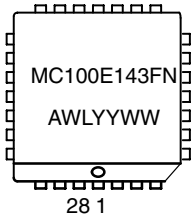


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAMS



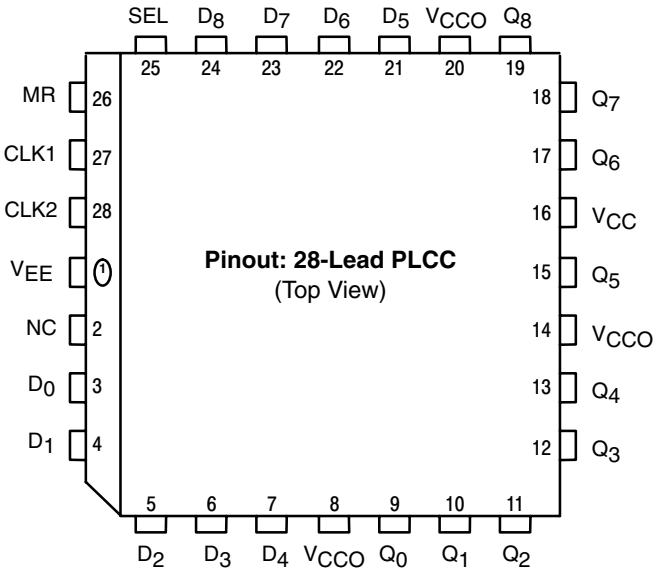


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E143FN	PLCC–28	37 Units/Rail
MC10E143FNR2	PLCC–28	500 Units/Reel
MC100E143FN	PLCC–28	37 Units/Rail
MC100E143FNR2	PLCC–28	500 Units/Reel

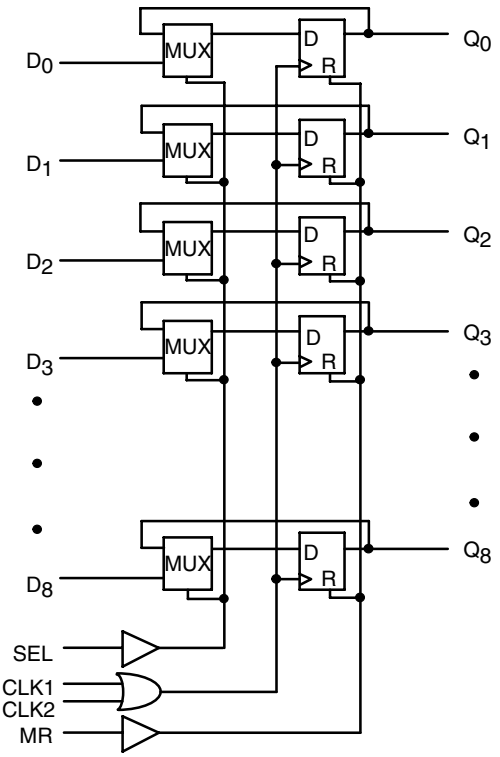
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN	FUNCTION
$D_0 – D_8$	ECL Parallel Data Inputs
SEL	ECL Mode Select Input
CLK1, CLK2	ECL Clock Inputs
MR	ECL Master Reset
$Q_0 – Q_8$	ECL Data Outputs
NC	No Connect
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply

FUNCTIONS

SEL	Mode
L	Load
H	Hold

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		120	145		120	145		120	145	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		120	145		120	145		120	145	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		120	145		120	145		138	165	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		120	145		120	145		138	165	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH}	Propagation Delay to Output										ps
t_{PHL}	Clk	600	800	1000	600	800	1000	600	800	1000	
	MR	600	800	1000	600	800	1000	600	800	1000	
t_s	Setup Time										ps
	D	50	–100		50	–100		50	–100		
	SEL	300	150		300	150		300	150		
t_h	Hold Time										ps
	D	300	100		300	100		300	100		
	SEL	75	–150		75	–150		75	–150		
t_{RR}	Reset Recovery Time	900	700		900	700		900	700		ps
t_{PW}	Minimum Pulse Width										ps
	Clk, MR	400			400			400			
t_{SKEW}	Within-Device Skew (Note 2.)		75			75			75		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r	Rise/Fall Times										ps
t_f	(20 - 80%)	300	525	800	300	525	800	300	525	800	

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.

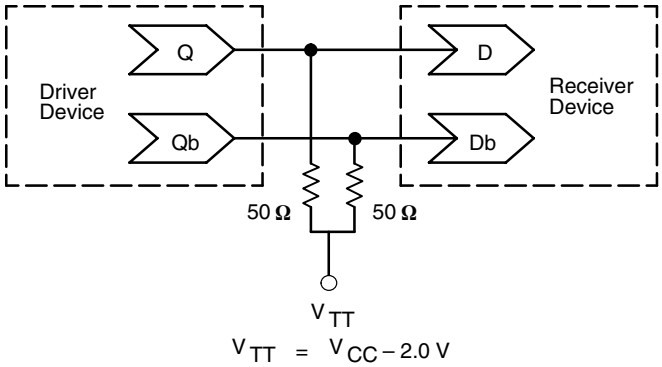


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E150, MC100E150

5V ECL 6-Bit D Latch

The MC10E/100E150 contains six D-type latches with differential outputs. When both Latch Enables (LEN1, LEN2) are LOW, the latch is transparent and input data transitions propagate through to the output. A logic HIGH on either LEN1 or LEN2 (or both) latches the data. The Master Reset (MR) overrides all other controls to set the Q outputs low.

The 100 Series contains temperature compensation.

- 800 ps Max. Propagation Delay
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 1 KV HBM, > 75 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 173 devices

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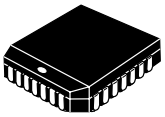

PLCC–28
FN SUFFIX
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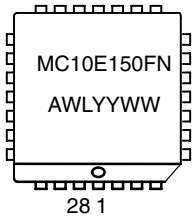
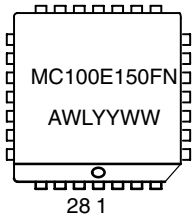
MARKING DIAGRAMS



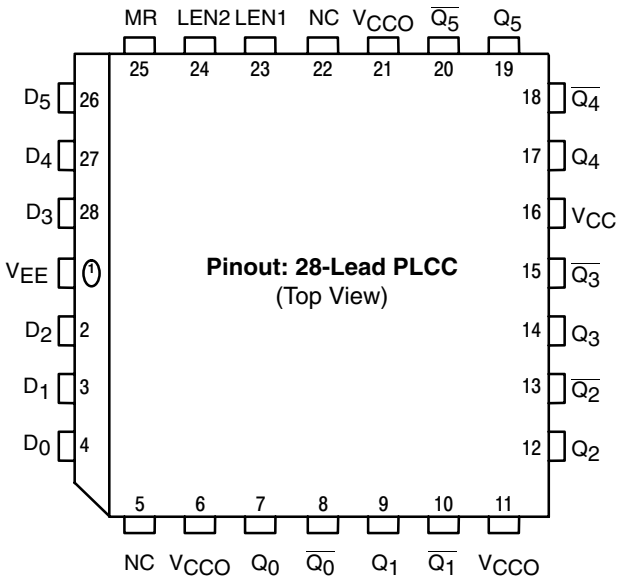


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E150FN	PLCC–28	37 Units/Rail
MC10E150FNR2	PLCC–28	500 Units/Reel
MC100E150FN	PLCC–28	37 Units/Rail
MC100E150FNR2	PLCC–28	500 Units/Reel

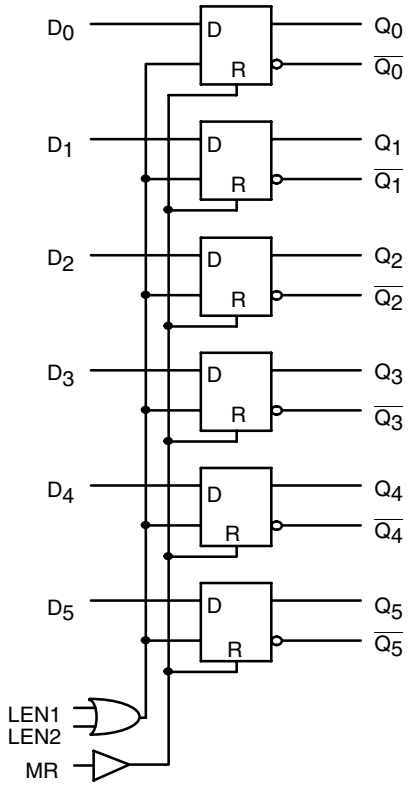
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN	FUNCTION
$D_0 - D_5$	ECL Data Inputs
LEN1, LEN2	ECL Latch Enables
MR	ECL Master Reset
$Q_0 - Q_5, \overline{Q_0} - \overline{Q_5}$	ECL Differential Outputs
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		52	62		52	62		52	62	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current D LEN, MR			 200 150			 200 150			 200 150	 µA µA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		52	62		52	62		52	62	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current D LEN, MR			 200 150			 200 150			 200 150	 µA µA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		52	62		52	62		60	72	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current D LEN, MR			 200 150			 200 150			 200 150	 µA µA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		52	62		52	62		60	72	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
I_{IH}	Input HIGH Current D LEN, MR			 200 150			 200 150			 200 150	 µA µA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output D LEN MR	 250 375 450	 375 500 625	 550 700 750	 250 375 450	 375 500 625	 550 700 750	 250 375 450	 375 500 625	 550 700 750	ps
t_s	Setup Time D	 200	 50		 200	 50		 200	 50		ps
t_h	Hold Time D	 200	 – 50		 200	 – 50		 200	 – 50		ps
t_{RR}	Reset Recovery Time	750	650		750	650		750	650		ps
t_{PW}	Minimum Pulse Width MR	 400			 400			 400			ps
t_{SKEW}	Within-Device Skew (Note 2.)		50			50			50		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Rise/Fall Times (20 - 80%)	 300	 450	 650	 300	 450	 650	 300	 450	 650	ps

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.

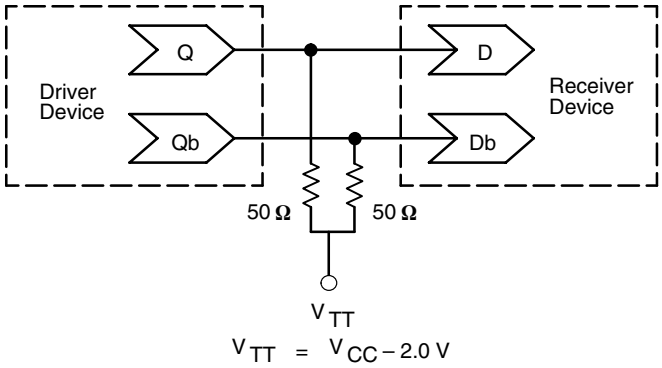


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E151, MC100E151

5V ECL 6-Bit D Register

The MC10E/100E151 contains 6 D-type, edge-triggered, master-slave flip-flops with differential outputs. Data enters the master when both CLK1 and CLK2 are LOW, and is transferred to the slave when CLK1 or CLK2 (or both) go HIGH. The asynchronous Master Reset (MR) makes all Q outputs go LOW.

The 100 Series contains temperature compensation.

- 1100 MHz Min. Toggle Frequency
- Differential Outputs
- Asynchronous Master Reset
- Dual Clocks
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 200 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 304 devices

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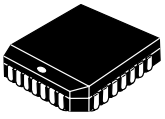


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAMS

28 1

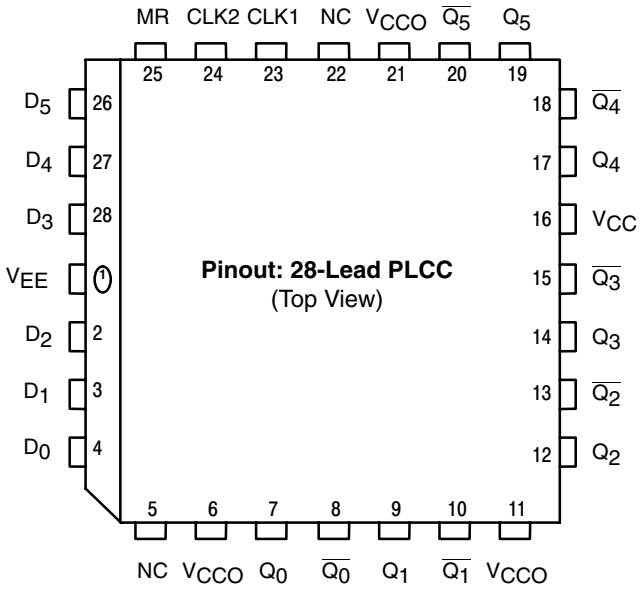
28 1

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E151FN	PLCC–28	37 Units/Rail
MC10E151FNR2	PLCC–28	500 Units/Reel
MC100E151FN	PLCC–28	37 Units/Rail
MC100E151FNR2	PLCC–28	500 Units/Reel

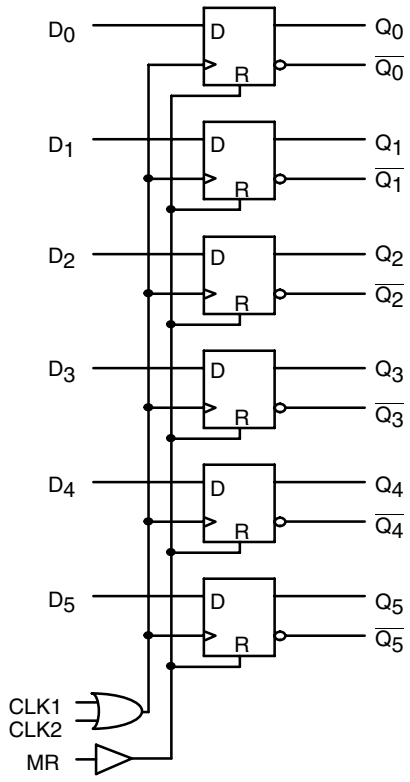
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN	FUNCTION
$D_0 - D_5$	ECL Data Inputs
CLK1, CLK2	ECL Clock Inputs
MR	ECL Master Reset
$Q_0 - Q_5$, $\overline{Q_0} - \overline{Q_5}$	ECL Differential Outputs
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

FUNCTION TABLE

MR		Qn
1	Reset	L
0	Operational	H

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current										mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current										μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current										mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current										μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		65	78		65	78		75	90	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		65	78		65	78		75	90	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH}	Propagation Delay to Output										ps
t_{PHL}	Clk	475	650	800	475	650	800	475	650	800	
	MR	475	650	850	475	650	850	475	650	850	
t_s	Setup TIme										ps
	D	0	–175		0	–175		0	–175		
t_h	Hold Time										ps
	D	350	175		350	175		350	175		
t_{RR}	Reset Recovery Time	750	550		750	550		750	550		
t_{PW}	Minimum Pulse Width										ps
	CLK, MR	400			400			400			
t_{SKEW}	Within-Device Skew (Note 2.)		65			65			65		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r	Rise/Fall Times										ps
t_f	(20 - 80%)	300	450	700	300	450	700	300	450	700	

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.

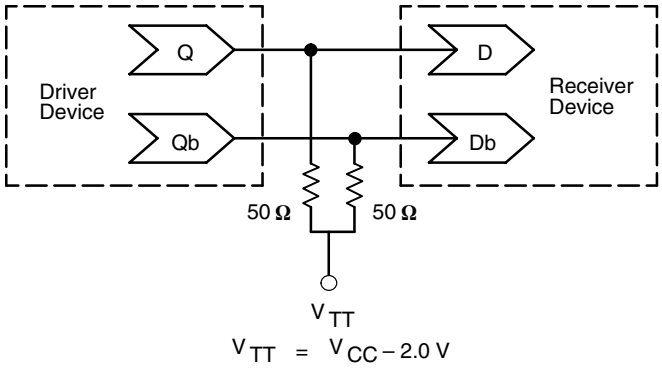


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E154, MC100E154

5V ECL 5-Bit 2:1 Mux-Latch

The MC10E/100E154 contains five 2:1 multiplexers followed by transparent latches with differential outputs. When both Latch Enables (LEN1, LEN2) are LOW, the latch is transparent, and output data is controlled by the multiplexer select control, SEL. A logic HIGH on either LEN1 or LEN2 (or both) latches the outputs. The Master Reset (MR) overrides all other controls to set the Q outputs LOW.

The 100 series contains temperature compensation.

- 850 ps Max. LEN to Output
- 825 ps Max. D to Output
- Differential Outputs
- Asynchronous Master Reset
- Dual Latch-Enables
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE} = –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 200 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 237 devices

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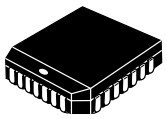
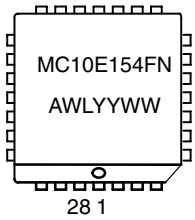
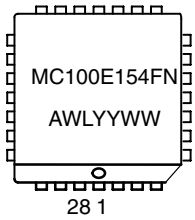


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAMS



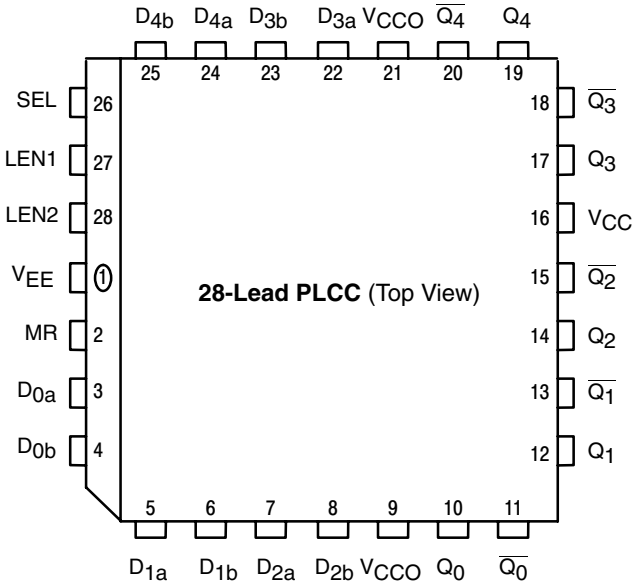
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week



ORDERING INFORMATION

Device	Package	Shipping
MC10E154FN	PLCC–28	37 Units/Rail
MC10E154FNR2	PLCC–28	500 Units/Reel
MC100E154FN	PLCC–28	37 Units/Rail
MC100E154FNR2	PLCC–28	500 Units/Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

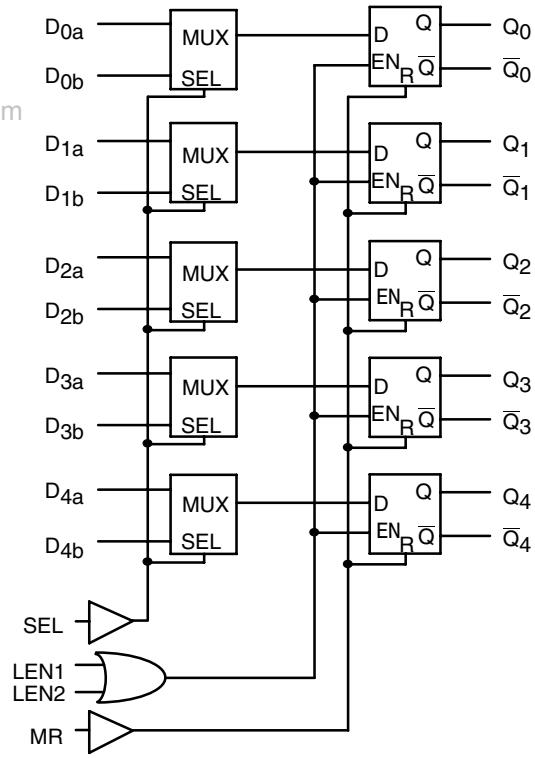
PIN DESCRIPTION

PIN	FUNCTION
$D_{0a} - D_{4a}$	ECL Input Data a
$D_{0b} - D_{4b}$	ECL Input Data b
SEL	ECL Data Select Input
LEN1, LEN2	ECL Latch Enables
MR	ECL Master Reset
$Q_0 - Q_4$, $\overline{Q}_0 - \overline{Q}_4$	ECL Differential Outputs
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply

TRUTH TABLE

SEL	Data
H	a
L	b

LOGIC DIAGRAM



MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		76	91		76	91		76	91	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		76	91		76	91		76	91	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		76	91		76	91		87	105	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		76	91		76	91		87	105	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH}	Propagation Delay to Output										ps
t_{PHL}	D	325	500	700	325	500	700	325	500	700	
	SEL	475	650	925	475	650	925	475	650	925	
	LEN	350	500	750	350	500	750	350	500	750	
	MR	450	600	800	450	600	800	450	600	800	
t_s	Setup Time										ps
	D	300	100		300	100		300	100		
	SEL	500	250		500	250		500	250		
t_h	Hold Time										ps
	D	300	–100		300	–100		300	–100		
	SEL	200	– 250		200	– 250		200	– 250		
t_{RR}	Reset Recovery Time	800	600		800	600		800	600		ps
t_{PW}	Minimum Pulse Width										ps
	MR	400			400			400			
t_{SKEW}	Within-Device Skew (Note 2.)		50			50			50		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r	Rise/Fall Times										ps
t_f	(20 - 80%)	300	475	800	300	475	800	300	475	800	

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.

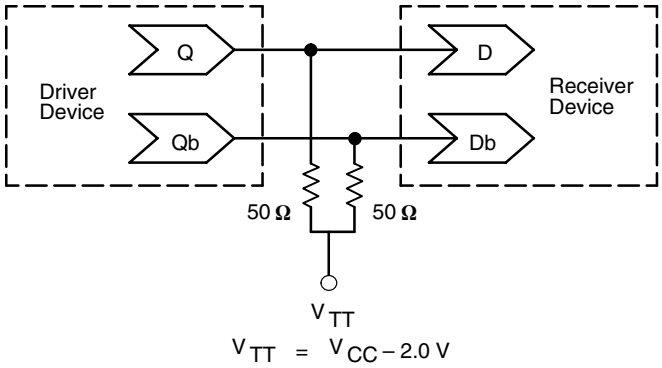


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E155, MC100E155

5V ECL 6-Bit 2:1 Mux-Latch

The MC10E/100E155 contains six 2:1 multiplexers followed by transparent latches with single-ended outputs. When both Latch Enables (LEN1, LEN2) are LOW, the latch is transparent, and output data is controlled by the multiplexer select control, SEL. A logic HIGH on either LEN1 or LEN2 (or both) latches the outputs. The Master Reset (MR) overrides all other controls to set the Q outputs LOW.

The 100 Series contains temperature compensation.

- 850 ps Max. LEN to Output
- 825 ps Max. D to Output
- Single-Ended Outputs
- Asynchronous Master Reset
- Dual Latch-Enables
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 200 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 239 devices

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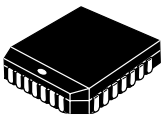
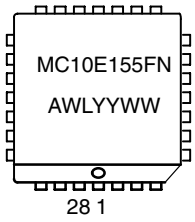
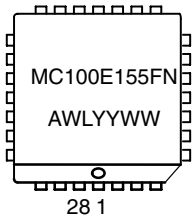


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAMS



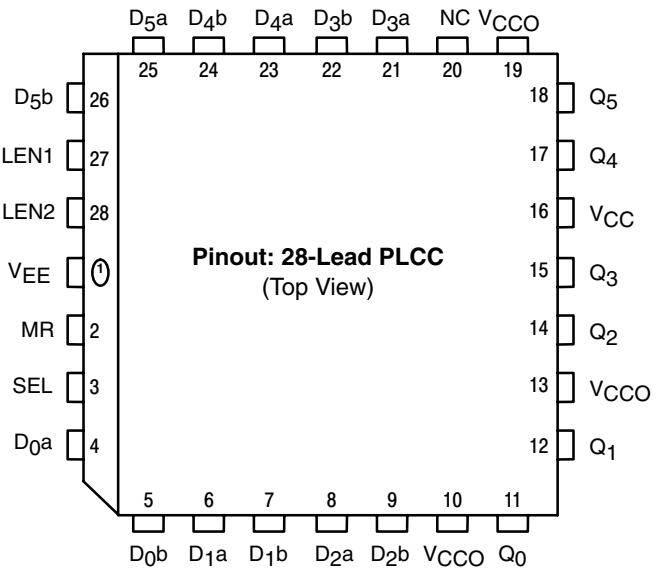


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E155FN	PLCC–28	37 Units/Rail
MC10E155FNR2	PLCC–28	500 Units/Reel
MC100E155FN	PLCC–28	37 Units/Rail
MC100E155FNR2	PLCC–28	500 Units/Reel

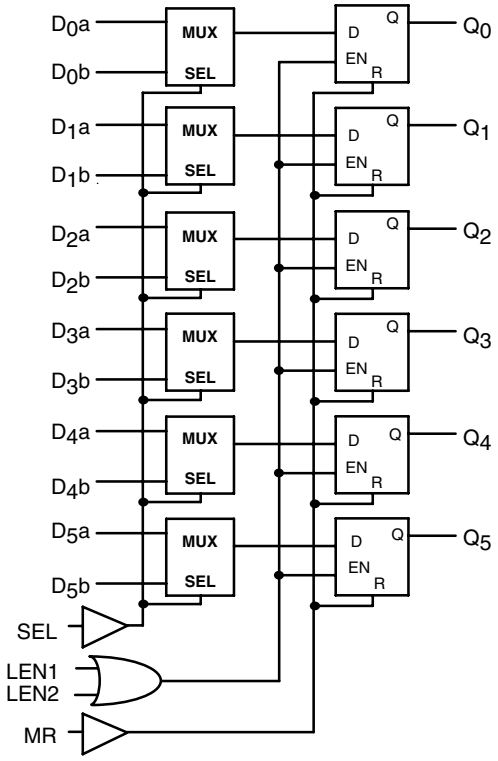
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN	FUNCTION
D_0a – D_04	ECL Input Data a
D_0b – D_4b	ECL Input Data b
SEL	ECL Data Select Input
LEN1, LEN2	ECL Latch Enables
Q_0 – Q_4	ECL Outputs
MR	Master Reset
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

TRUTH TABLE

SEL	Data
H	a
L	b

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		85	102		85	102		85	102	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		85	102		85	102		85	102	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		85	102		85	102		98	117	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		85	102		85	102		98	117	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH}	Propagation Delay to Output										ps
t_{PHL}	D	325	500	700	325	500	700	325	500	700	
	SEL	475	675	925	475	675	925	475	675	925	
	LEN	350	500	750	350	500	750	350	500	750	
	MR	450	600	850	450	600	850	450	600	850	
t_s	Setup Time										ps
	D	300	100		300	100		300	100		
	SEL	500	250		500	250		500	250		
t_h	Hold TIme										ps
	D	300	–100		300	–100		300	–100		
	SEL	0	– 250		0	– 250		0	– 250		
t_{RR}	Reset Recovery Time	800	650		800	650		800	650		ps
t_{PW}	Minimum Pulse Width										ps
	MR	400			400			400			
t_{SKEW}	Within-Device Skew (Note 2.)		75			75			75		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r	Rise/Fall Times										ps
t_f	(20 - 80%)	300	450	800	300	450	800	300	450	800	

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.

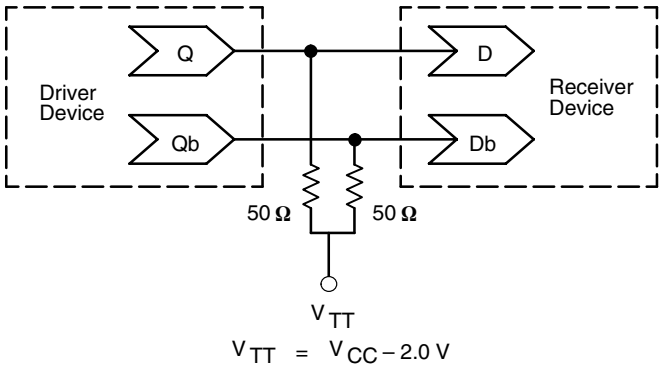


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E156, MC100E156

5V ECL 3-Bit 4:1 Mux-Latch

The MC10E/100E156 contains three 4:1 multiplexers followed by transparent latches with differential outputs. When both Latch Enables (LEN1, LEN2) are LOW, the latch is transparent, and output date is controlled by the multiplexer select controls (SEL0, SEL1). A logic HIGH on either LEN1 or LEN2 (or both) latches the outputs. The Master Reset (MR) overrides all other controls to set the Q outputs LOW.

The 100 Series contains temperature compensation.

- 950 ps Max. D to Output
- 850 ps Max. LEN to Output
- Differential Outputs
- Asynchronous Master Reset
- Dual Latch-Enables
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 200 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 271 devices

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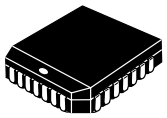
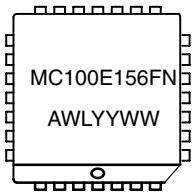
MARKING DIAGRAMS



PLCC–28
FN SUFFIX
CASE 776

28 1



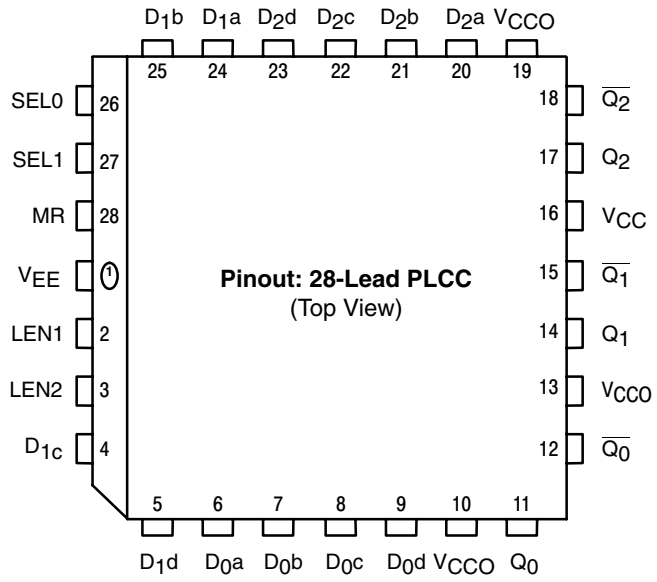
28 1

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E156FN	PLCC–28	37 Units/Rail
MC10E156FNR2	PLCC–28	500 Units/Reel
MC100E156FN	PLCC–28	37 Units/Rail
MC100E156FNR2	PLCC–28	500 Units/Reel

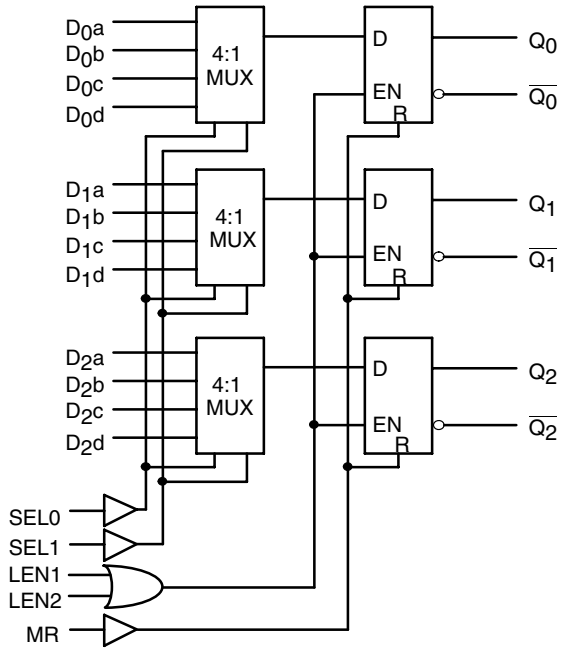
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN	FUNCTION
$D_0x - D_3x$	ECL Input Data
SEL0, SEL1	ECL Select Inputs
LEN1, LEN2	ECL Latch Enables
$Q_0 - Q_2$, $\overline{Q}_0 - \overline{Q}_2$	ECL Differential Outputs
MR	ECL Master Reset
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply

FUNCTION TABLE

SEL1	SEL0	Data
L	L	a
L	H	b
H	L	c
H	H	d

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		75	90		75	90		75	90	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		75	90		75	90		75	90	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		75	90		75	90		86	103	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		75	90		75	90		86	103	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH}	Propagation Delay to Output										ps
t_{PHL}	D	400	600	900	400	600	900	400	600	900	
	SEL0	550	775	1050	550	775	1050	550	775	1050	
	SEL1	450	650	900	450	650	900	450	650	900	
	LEN	350	500	800	350	500	800	350	500	800	
	MR	350	600	825	350	600	825	350	600	825	
t_s	Setup Time										ps
	D	400	275		400	275		400	275		
	SEL0	700	300		700	300		700	300		
	SEL1	600	400		600	400		600	400		
t_h	Hold Time										ps
	D	300	– 275		300	– 275		300	– 275		
	SEL0	100	– 300		100	– 300		100	– 300		
	SEL1	200	– 400		200	– 400		200	– 400		
t_{RR}	Reset Recovery Time	800	600		800	600		800	600		ps
t_{PW}	Minimum Pulse Width										ps
	MR	400			400			400			
t_{SKEW}	Within-Device Skew (Note 2.)		50			50			50		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r	Rise/Fall Times										ps
t_f	(20 - 80%)	275	475	700	275	475	700	275	475	700	

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.

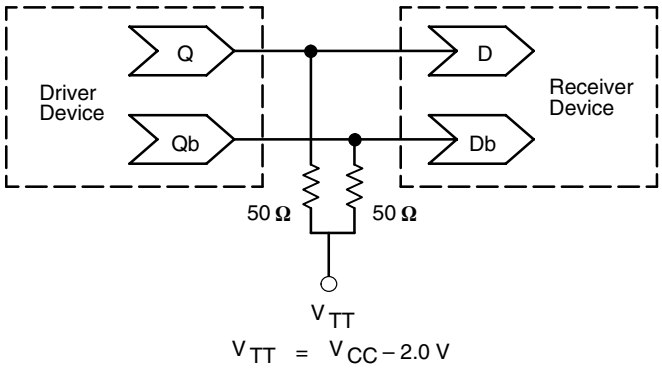


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E157, MC100E157

5V ECL Quad 2:1 Multiplexer

The MC10E/100E157 contains four 2:1 multiplexers with differential outputs. The output data are controlled by the individual Select (SEL) inputs. The individual select control makes the devices well suited for random logic designs.

The 100 Series contains temperature compensation.

- Individual Select Controls
- 550 ps Max. D to Output
- 800 ps Max. SEL to Output
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- ESD Protection: > 1 KV HBM, > 75 V MM
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 137 devices

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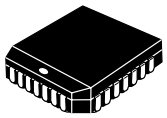
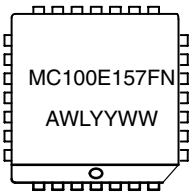


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAMS

28 1



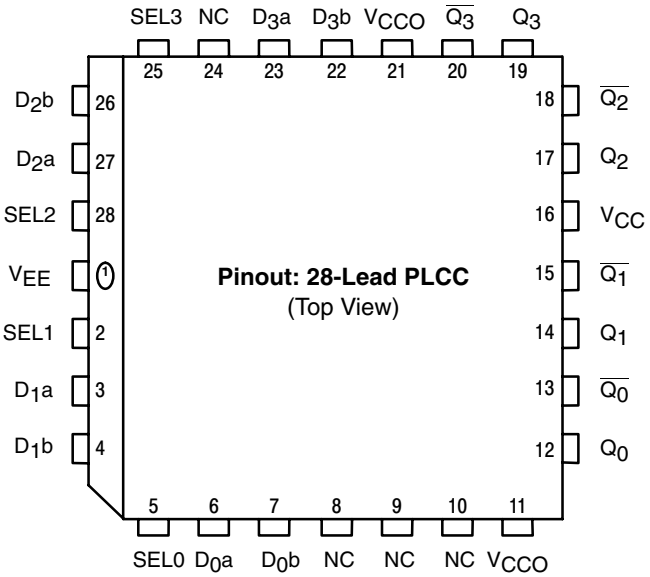
28 1

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E157FN	PLCC–28	37 Units/Rail
MC10E157FNR2	PLCC–28	500 Units/Reel
MC100E157FN	PLCC–28	37 Units/Rail
MC100E157FNR2	PLCC–28	500 Units/Reel

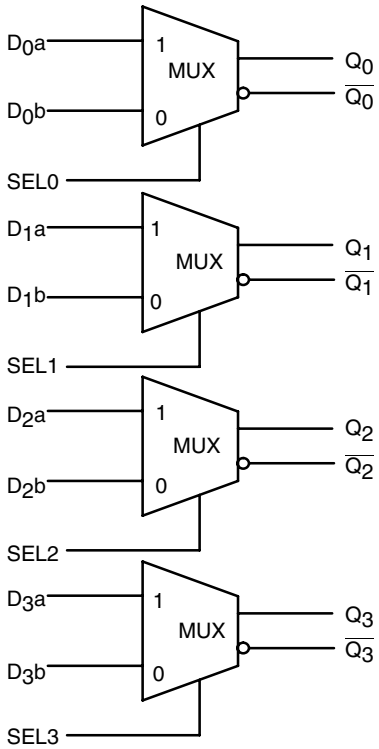
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN	FUNCTION
D_0a – D_3a	ECL Input Data a
D_0b – D_3b	ECL Input Data b
SEL0 – SEL3	ECL Select Inputs
Q_0 – Q_3, $\overline{Q_0}$ – $\overline{Q_3}$	ECL Differential Outputs
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

TRUTH TABLE

SEL	DATA
H	a
L	b

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC2}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

0		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		32	38		32	38		32	38	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current D SEL			 200 150			 200 150			 200 150	 µA µA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		32	38		32	38		32	38	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current D SEL			 200 150			 200 150			 200 150	 µA µA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		32	38		32	38		37	44	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
I_{IH}	Input HIGH Current										
	D			200			200			200	μA
	SEL			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		32	38		32	38		37	44	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
I_{IH}	Input HIGH Current										
	D			200			200			200	μA
	SEL			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH}	Propagation Delay to Output										ps
t_{PHL}	D	220	380	550	220	380	550	220	380	550	
	SEL	425	600	800	425	600	800	425	600	800	
t_{SKEW}	Within-Device Skew (Note 2.)		70			70			70		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r	Rise/Fall Times										ps
t_f	(20 - 80%)	275	400	650	275	400	650	275	400	650	

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.

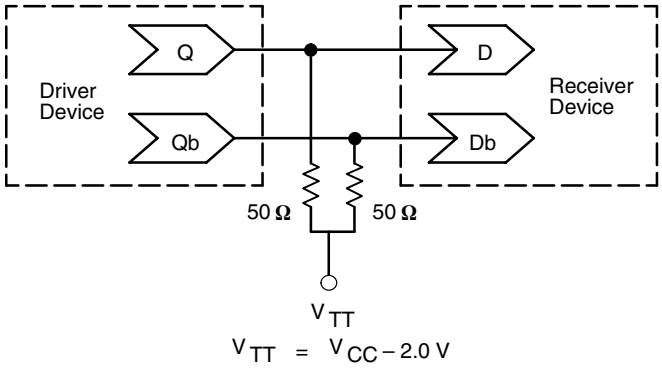


Figure 1. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E158, MC100E158

5V ECL 5-Bit 2:1 Multiplexer

The MC10E/100E158 contains five 2:1 multiplexers with differential outputs. The output data are controlled by the Select input (SEL).

The 100 Series contains temperature compensation.

- 600 ps Max. D to Output
- 800 ps Max. SEL to Output
- Differential Outputs
- One V_{CCO} Pin Per Output Pair
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 200 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 126 devices

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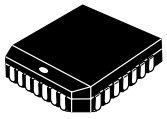
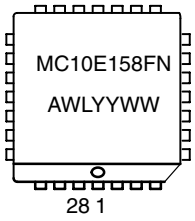
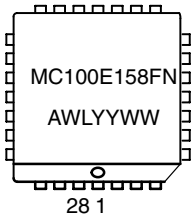


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAMS



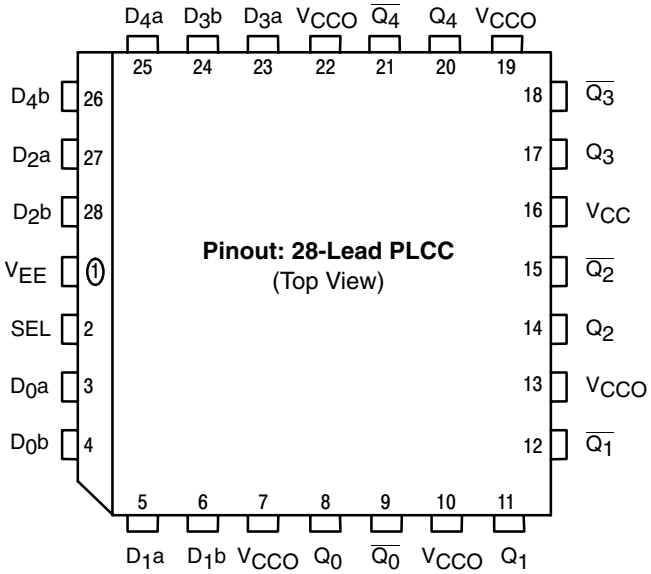
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week



ORDERING INFORMATION

Device	Package	Shipping
MC10E158FN	PLCC–28	37 Units/Rail
MC10E158FNR2	PLCC–28	500 Units/Reel
MC100E158FN	PLCC–28	37 Units/Rail
MC100E158FNR2	PLCC–28	500 Units/Reel

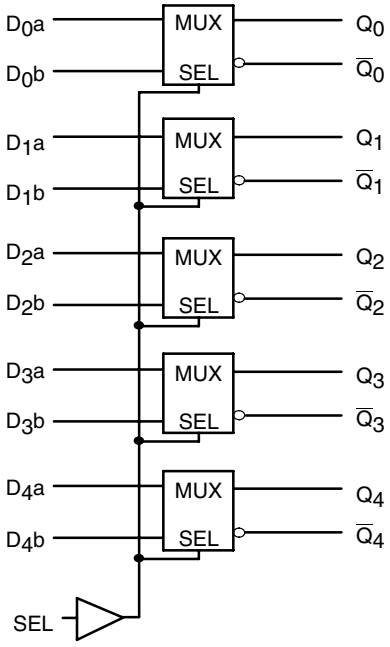
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



PIN DESCRIPTION

Pin	Function
$D_0a – D_4a$	ECL Input Data a
$D_0b – D_4b$	ECL Input Data b
$Q_0 – Q_4$	ECL True Outputs
$\overline{Q}_0 – \overline{Q}_4$	ECL Inverted Outputs
SEL	ECL Select Input
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply

FUNCTION TABLE

SEL	Data
H	a
L	b

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		33	40		33	40		33	40	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current D SEL			 200 150			 200 150			 200 150	 µA µA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		33	40		33	40		33	40	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current D SEL			 200 150			 200 150			 200 150	 µA µA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		33	40		33	40		38	46	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current D SEL			 200 150			 200 150			 200 150	 µA µA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		33	40		33	40		38	46	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
I_{IH}	Input HIGH Current D SEL			 200 150			 200 150			 200 150	 µA µA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output D SEL	 225 400	 385 600	 550 775	 225 400	 385 600	 550 775	 225 400	 385 600	 550 775	ps
t_{SKEW}	Within-Device Skew (note 2.)		60			60			60		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Rise/Fall Time (20 - 80%)	 275	 425	 650	 275	 425	 650	 275	 425	 650	ps

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.

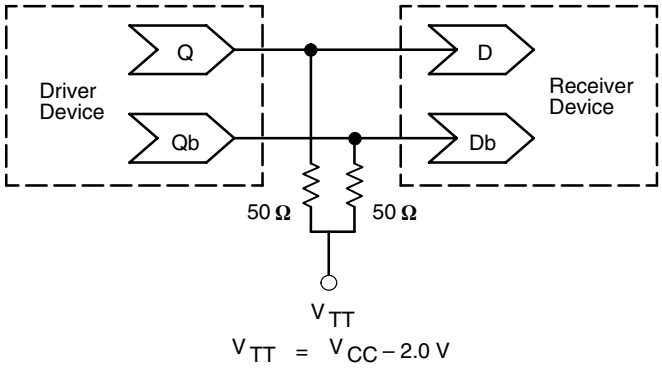


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E160, MC100E160

5V ECL 12-Bit Parity Generator/Checker

The MC10E/100E160 is a 12-bit parity generator/checker. The Q output is HIGH when an odd number of inputs are HIGH. A HIGH on the Enable input ($\overline{EN}$) forces the Q output LOW.

The 100 Series contains temperature compensation.

- Provides Odd-HIGH Parity of 12 Inputs
- Shiftable Output Register with Hold
- 900 ps Max. D to Q/$\overline{Q}$ Output
- Enable
- Asynchronous Register Reset
- Dual Clocks
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 1 KV HBM, > 75 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 312 devices

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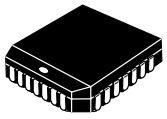
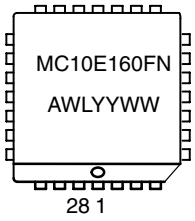
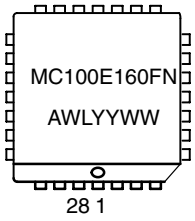


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAMS



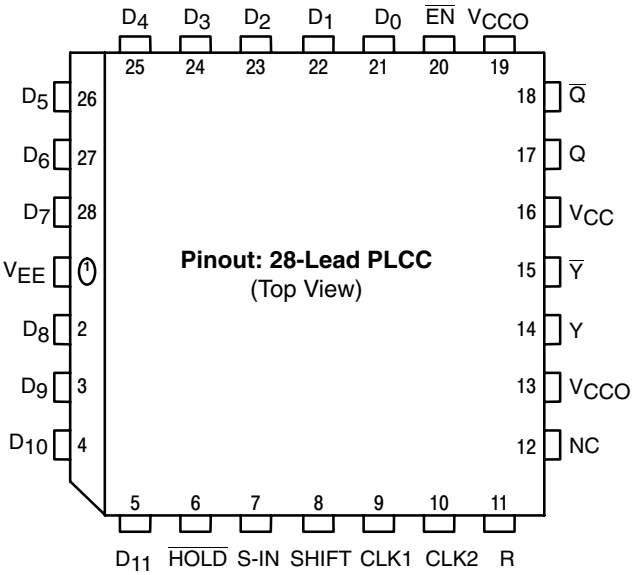
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week



ORDERING INFORMATION

Device	Package	Shipping
MC10E160FN	PLCC–28	37 Units/Rail
MC10E160FNR2	PLCC–28	500 Units/Reel
MC100E160FN	PLCC–28	37 Units/Rail
MC100E160FNR2	PLCC–28	500 Units/Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



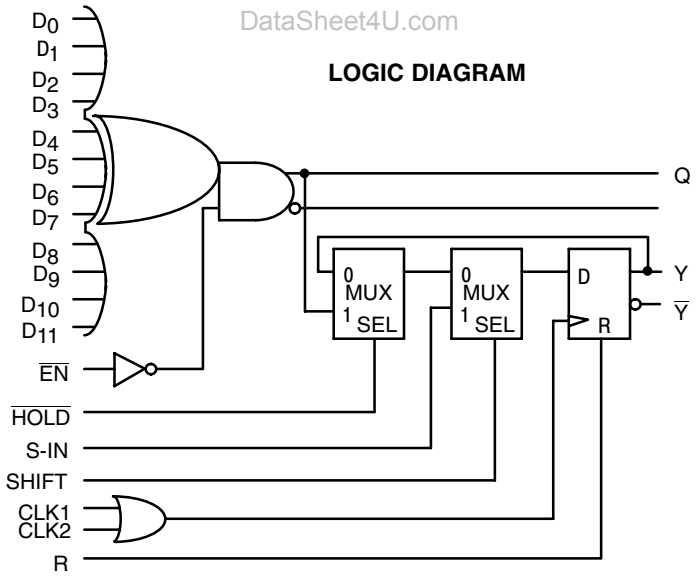
* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

PIN	FUNCTION
$D_0 - D_{11}$	ECL Data Inputs
S-IN	ECL Serial Data Input
$\overline{EN}$	ECL Enable, active LOW
$\overline{HOLD}$	ECL Hold, active LOW
SHIFT	ECL Shift, active HIGH
CLK1, CLK2	ECL Clock Inputs
R	ECL Reset Inputs
Q, $\overline{Q}$	ECL Direct Output
Y, $\overline{Y}$	ECL Register Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

LOGIC DIAGRAM



MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		82	98		82	98		82	98	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current CLK1, CLK2 R All Other Inputs			 200 300 150			 200 300 150			 200 300 150	 µA µA µA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		82	98		82	98		82	98	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current CLK1, CLK2 R All Other Inputs			 200 300 150			 200 300 150			 200 300 150	 µA µA µA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		82	98		82	98		94	113	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current										
	CLK1, CLK2			200			200			200	μA
	R			300			300			300	μA
	All Other Inputs			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		82	98		82	98		94	113	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
I_{IH}	Input HIGH Current										
	CLK1, CLK2			200			200			200	μA
	R			300			300			300	μA
	All Other Inputs			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH}	Propagation Delay to Output										ps
t_{PHL}	D to Q	400	650	950	400	650	950	400	650	950	
	$\overline{En}$ to Q	300	550	750	300	550	750	300	550	750	
	CLK to Y	275	500	700	275	500	700	275	500	700	
	R to Y	275	500	725	275	500	725	275	500	725	
t_s	Setup Time										ps
	D	1200	900		1200	900		1200	900		
	$\overline{HOLD}$	600	300		600	300		600	300		
	S-IN	350	150		350	150		350	150		
	SHIFT	500	250		500	250		500	250		
t_h	Hold Time										ps
	D	– 400	– 900		– 400	– 900		– 400	– 900		
	$\overline{HOLD}$	100	– 300		100	– 300		100	– 300		
	S-IN	300	–150		300	–150		300	–150		
	SHIFT	200	– 250		200	– 250		200	– 250		
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r	Rise/Fall Time										ps
t_f	(20 - 80%)	300	450	650	300	450	650	300	450	650	

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.

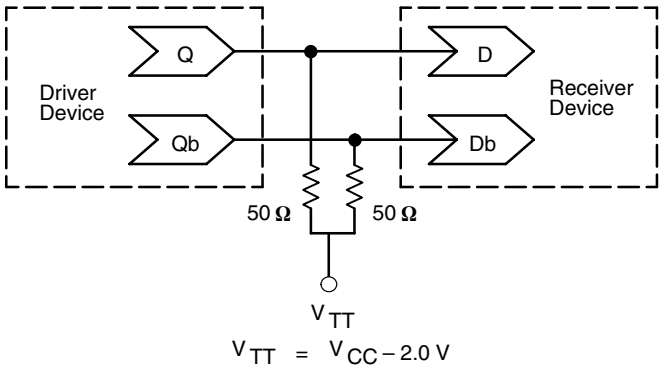


Figure 1. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E163, MC100E163

5V ECL 2-Bit 8:1 Multiplexer

The MC10E/100E163 contains two 8:1 multiplexers with differential outputs and common select inputs. The select inputs (SEL0, 1, 2) control which one of the eight data inputs (A_0 – A_7, B_0 – B_7) is propagated to the output.

The 100 Series contains temperature compensation.

- 850 ps Max. D to Output
- Differential Outputs
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 200 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 262 devices

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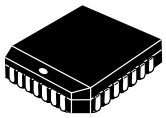
MARKING DIAGRAMS



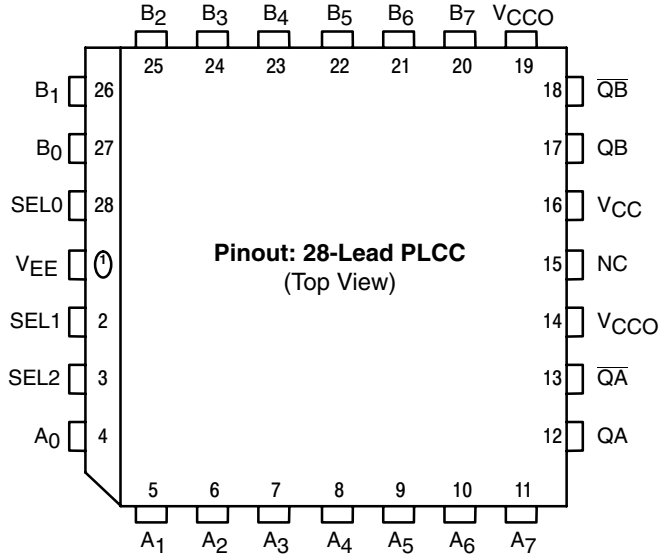
PLCC–28
FN SUFFIX
CASE 776

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E163FN	PLCC–28	37 Units/Rail
MC10E163FNR2	PLCC–28	500 Units/Reel
MC100E163FN	PLCC–28	37 Units/Rail
MC100E163FNR2	PLCC–28	500 Units/Reel

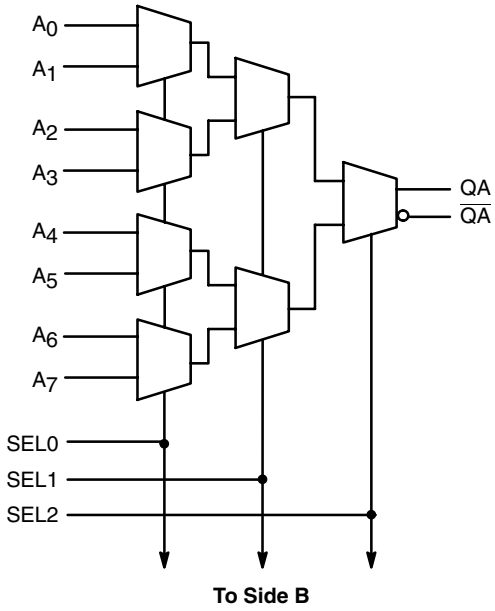
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



To Side B

PIN DESCRIPTION

PIN	FUNCTION
$A_0 – A_7$	ECL A Data Inputs
$B_0 – B_7$	ECL B Data Inputs
SEL0, 1, 2	ECL Select Inputs
QA, QB	ECL True Outputs
$\overline{QA}$, $\overline{QB}$	ECL Inverting Outputs
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

FUNCTION TABLE

SEL2	SEL1	SEL0	A/B Data
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		73	88		73	88		73	88	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		73	88		73	88		73	88	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		73	88		73	88		83	100	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		73	88		73	88		83	100	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH}	Propagation Delay to Output										ps
t_{PHL}	D	400	550	800	400	550	800	400	550	800	
	SEL0	525	725	950	525	725	950	525	725	950	
	SEL1	425	625	850	425	625	850	425	625	850	
	SEL2	350	525	725	350	525	725	350	525	725	
t_{SKEW}	Within-Device Skew (Note 2.)										ps
	An, Bn to Q		40			40			40		
	An, Am to QA		30			30			30		
	Bn, Bm to QB		30			30			30		
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r	Rise/Fall Time										ps
t_f	(20 - 80%)	275	375	575	275	375	575	275	375	575	

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Within-device skew is defined as identical transitions on similar paths through a device; n = 0-7, m n, m = 0-7.

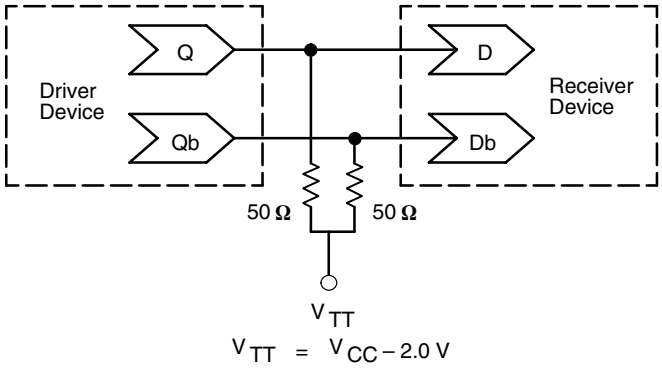


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E164, MC100E164

5V ECL 16:1 Multiplexer

The MC10E/100E164 is a 16:1 multiplexer with a differential output. The select inputs (SEL0, 1, 2, 3) control which one of the sixteen data inputs (A0 – A15) is propagated to the output.

Special attention to the design layout results in a typical skew between the 16 inputs of only 50 ps.

The 100 Series contains temperature compensation.

- 850 ps Data Input to Output
- Differential Output
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 200 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 213 devices

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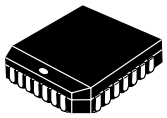
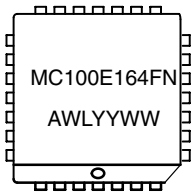


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAMS

28 1



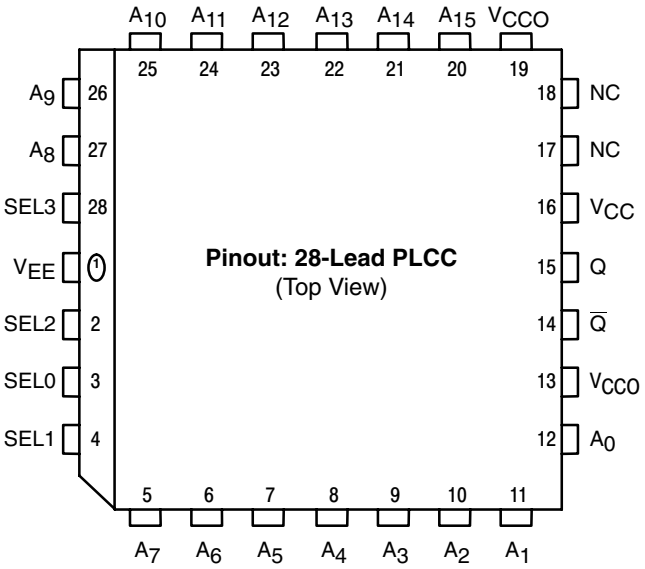
28 1

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E164FN	PLCC–28	37 Units/Rail
MC10E164FNR2	PLCC–28	500 Units/Reel
MC100E164FN	PLCC–28	37 Units/Rail
MC100E164FNR2	PLCC–28	500 Units/Reel

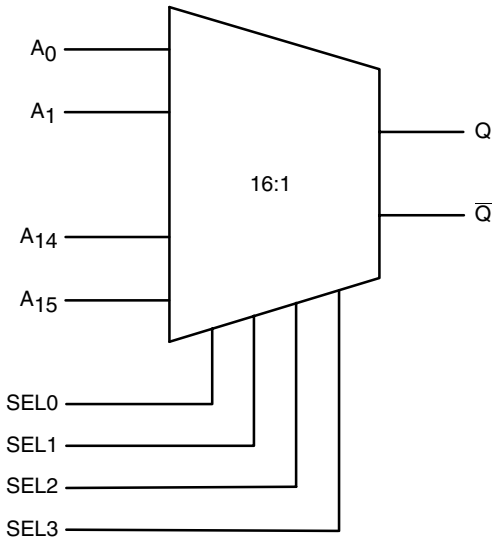
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN	FUNCTION
$A_0 - A_{15}$	ECL Data Inputs
SEL[0:3]	ECL Select Inputs
Q, $\overline{Q}$	ECL Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

FUNCTION TABLE

SEL3	SEL2	SEL1	SEL0	Data
L	L	L	L	A0
L	L	L	H	A1
L	L	H	L	A2
L	L	H	H	A3
L	H	L	L	A4
L	H	L	H	A5
L	H	H	L	A6
L	H	H	H	A7
H	L	L	L	A8
H	L	L	H	A9
H	L	H	L	A10
H	L	H	H	A11
H	H	L	L	A12
H	H	L	H	A13
H	H	H	L	A14
H	H	H	H	A15

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		59	71		59	71		59	71	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		59	71		59	71		59	71	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		59	71		59	71		68	81	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		59	71		59	71		68	81	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH}	Propagation Delay to Output										ps
t_{PHL}	A Input	350	600	850	350	600	850	350	600	850	
	SEL0	500	700	900	500	700	900	500	700	900	
	SEL1	400	675	900	400	675	900	400	675	900	
	SEL2	400	675	900	400	675	900	400	675	900	
	SEL3	400	550	700	400	550	700	400	550	700	
t_{SKEW}	Within Device Skew (Note 2.)		50			50			50		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r	Rise/Fall Times										ps
t_f	(20 - 80%)	275	400	550	275	400	550	275	400	550	

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Within Device skew is defined as the difference in the A to Q delay between the 16 different A inputs.

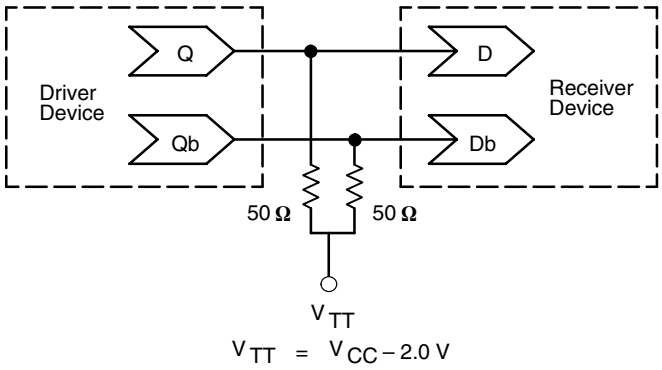


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E166, MC100E166

5V ECL 9-Bit Magnitude Comparator

The MC10E/100E166 is a 9-bit magnitude comparator which compares the binary value of two 9-bit words and indicates whether one word is greater than, or equal to, the other.

The 100 Series contains temperature compensation.

- 1100 ps Max. $\overline{A=B}$
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 200 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 354 devices

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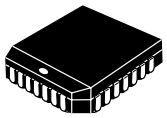


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAMS

28 1

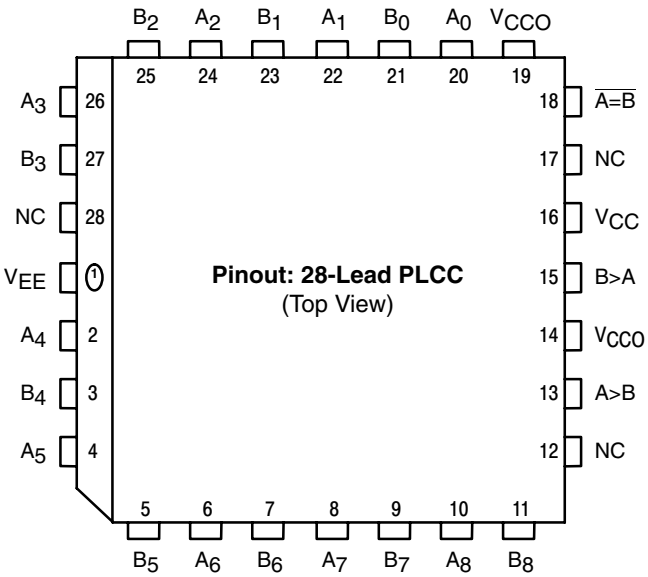
28 1

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E166FN	PLCC–28	37 Units/Rail
MC10E166FNR2	PLCC–28	500 Units/Reel
MC100E166FN	PLCC–28	37 Units/Rail
MC100E166FNR2	PLCC–28	500 Units/Reel

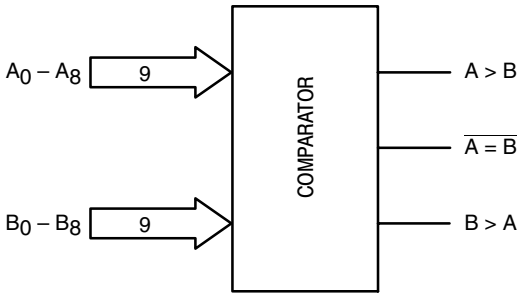
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO} ,and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN	FUNCTION
$A_0 – A_8$	ECL A Data Inputs
$B_0 – B_8$	ECL B Data Inputs
A > B	ECL A Greater than B Output
B > A	ECL B Greater than A Output
$\overline{A = B}$	ECL A Equal to B Output (active-LOW)
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		113	156		113	156		113	156	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		113	156		113	156		113	156	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		113	156		113	156		130	156	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		113	156		113	156		130	156	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH}	Propagation Delay to Output										ps
t_{PHL}	D to A = B	500	750	1100	500	750	1100	500	750	1100	
	D to A < B, A > B	500	850	1400	500	850	1400	500	850	1400	
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r	Rise/Fall Time										ps
t_f	(20 - 80%)	300	450	800	300	450	800	300	450	800	

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.

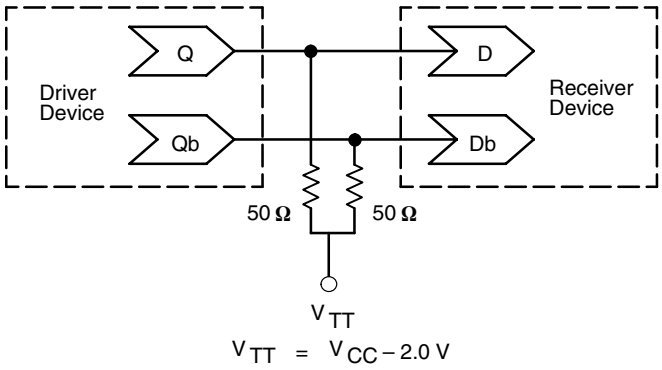


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E167, MC100E167

5V ECL 6-Bit 2:1 Mux-Register

The MC10E/100E167 contains six 2:1 multiplexers followed by D flip-flops with single-ended outputs. Input data are selected by the Select control, SEL. The selected data are transferred to the flip-flop outputs by a positive edge on CLK1 or CLK2 (or both). A HIGH on the Master Reset (MR) pin asynchronously forces all Q outputs LOW.

The 100 Series contains temperature compensation.

- 1000 MHz Min. Operating Frequency
- 800 ps Max. Clock to Output
- Single-Ended Outputs
- Asynchronous Master Resets
- Dual Clocks
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 1 KV HBM, > 75 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 323 devices

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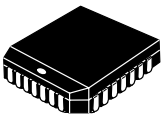
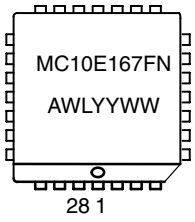
MARKING DIAGRAMS



PLCC–28
FN SUFFIX
CASE 776



28 1

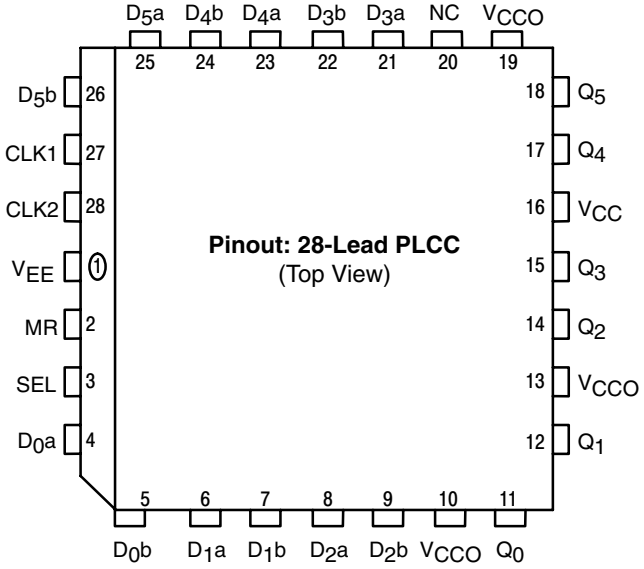
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

28 1

ORDERING INFORMATION

Device	Package	Shipping
MC10E167FN	PLCC–28	37 Units/Rail
MC10E167FNR2	PLCC–28	500 Units/Reel
MC100E167FN	PLCC–28	37 Units/Rail
MC100E167FNR2	PLCC–28	500 Units/Reel

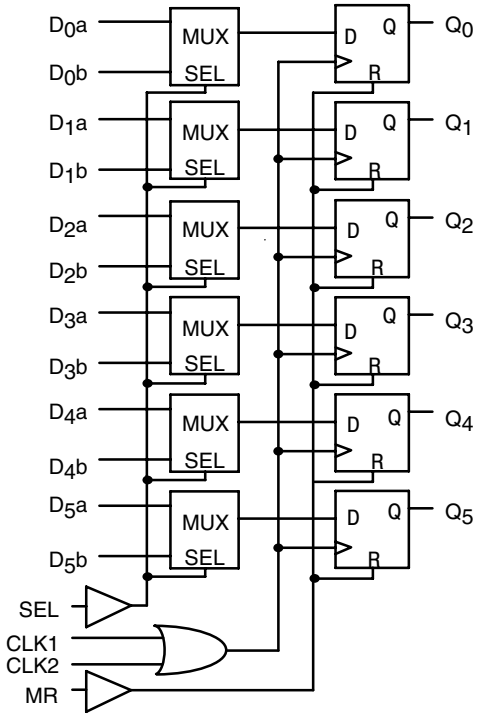
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN	FUNCTION
$D_0a – D_5a$	ECL Input Data a
$D_0b – D_5b$	ECL Input Data b
SEL	ECL Select Input
CLK1, CLK2	ECL Clock Inputs
MR	ECL Master Reset
$Q_0 – Q_5$	ECL Data Outputs
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

FUNCTIONS

SEL	DATA
H	a
L	b

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		94	113		94	113		94	113	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		94	113		94	113		94	113	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		94	113		94	113		108	130	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		94	113		94	113		108	130	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{MAX}	Maximum Toggle Frequency		TBD			>1.0			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output										ps
	Clk	450	650	800	450	650	800	450	650	800	
	MR	450	650	850	450	650	850	450	650	850	
t_s	Setup Time										ps
	D	100	– 50		100	– 50		100	– 50		
	SEL	275	125		275	125		275	125		
t_h	Hold Time										ps
	D	300	50		300	50		300	50		
	SEL	75	–125		75	–125		75	–125		
t_{RR}	Reset Recovery Time	750	550		750	550		750	550		ps
t_{PW}	Minimum Pulse Width										ps
	Clk, MR	400			400			400			
t_{SKEW}	Within-Device Skew (Note 2.)		75			75			75		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Rise/Fall Times										ps
	(20 - 80%)	300	450	800	300	450	800	300	450	800	

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.

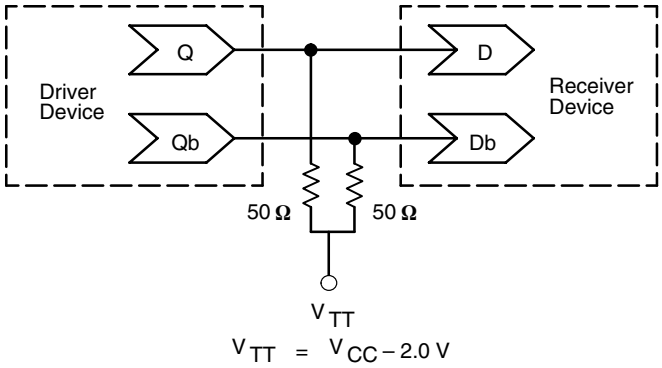


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E171, MC100E171

5V ECL 3-Bit 4:1 Multiplexer

The MC10E/100E171 contains three 4:1 multiplexers with differential outputs. Separate Select controls are provided for the leading 2:1 mux pairs (see logic symbol). The three Select inputs control which one of the four data inputs in each case is propagated to the corresponding output.

The 100 Series contains temperature compensation.

- 725 ps Max. D to Output
- Split Select
- Differential Outputs
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 200 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 203 devices

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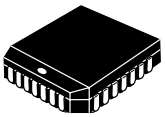
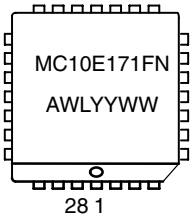
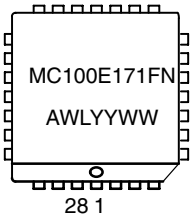


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAMS



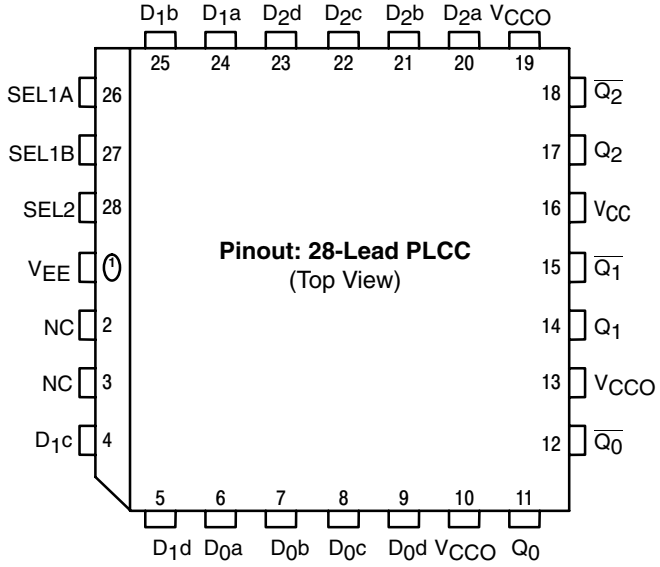


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E171FN	PLCC–28	37 Units/Rail
MC10E171FNR2	PLCC–28	500 Units/Reel
MC100E171FN	PLCC–28	37 Units/Rail
MC100E171FNR2	PLCC–28	500 Units/Reel

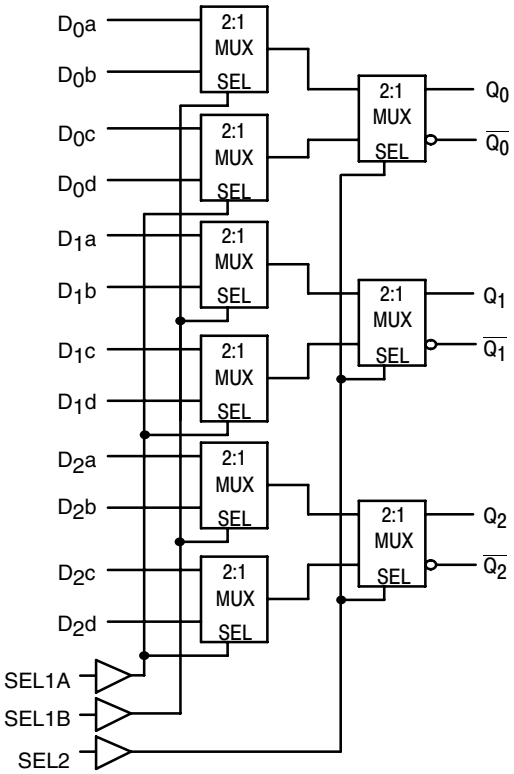
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN	FUNCTION
$D_0x - D_2x$	ECL Data Inputs
SEL1A, SEL1B	ECL First-stage Select Inputs
SEL2	ECL Second-stage Select Input
$Q_0 - Q_2$	ECL True Output
$\overline{Q}_0 - \overline{Q}_2$	ECL Inverted Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

FUNCTION TABLE

PIN	STATE	OPERATION
SEL2	H	Output c/d data
SEL1A	H	Input d data
SEL1B	H	Input b data

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		56	67		56	67		56	67	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		56	67		56	67		56	67	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		56	67		56	67		65	77	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		56	67		56	67		65	77	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH}	Propagation Delay to Output										ps
t_{PHL}	D	275	480	650	275	480	650	275	480	650	
	SEL1	450	650	850	450	650	850	450	650	850	
	SEL2	350	550	700	350	550	700	350	550	700	
t_{SKEW}	Within-Device Skew (Note 2.)										ps
	Dnm, Dnm to Qn		60			60			60		
	Da, Db, Dc, Dd to Q		40			40			40		
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r	Rise/Fall Time										ps
t_f	(20 - 80%)	300	475	650	300	475	650	300	475	650	

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Within-device skew is defined as identical transitions on similar paths through a device; n = 0,1,2 m = a,b,c,d.

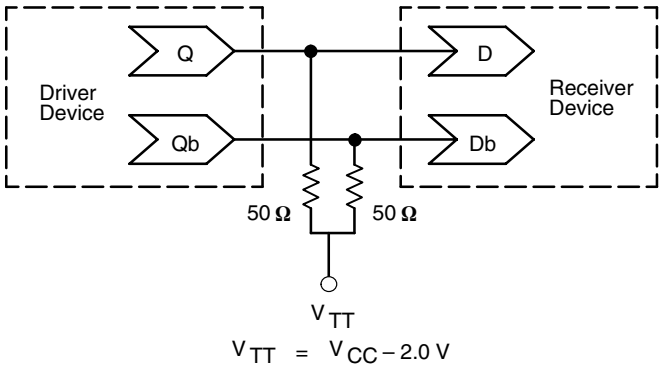


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E175, MC100E175

5V ECL 9-Bit Latch With Parity

The MC10E/100E175 is a 9-bit latch. It also features a tenth latched output, ODDPAR, which is formed as the odd parity of the nine data inputs (ODDPAR is HIGH if an odd number of the inputs are HIGH).

The E175 can also be used to generate byte parity by using D8 as the parity-type select (L = even parity, H = odd parity), and using ODDPAR as the byte parity output.

The LEN pin latches the data when asserted with a logical high and makes the latch transparent when placed at a logic low level.

- 9-Bit Latch
- Parity Detection/Generation
- 800 ps Max. D to Output
- Reset
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 1 KV HBM, > 75 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 416 devices

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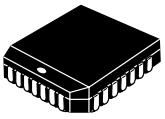
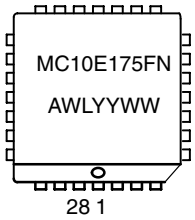


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAMS



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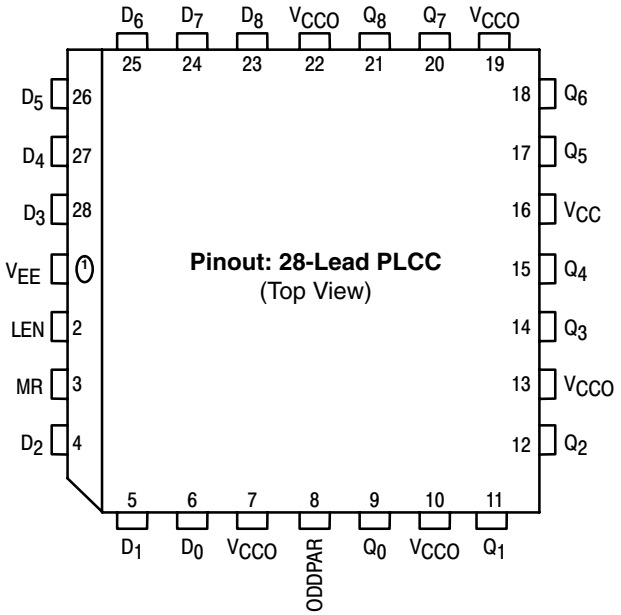
28 1

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E175FN	PLCC–28	37 Units/Rail
MC10E175FNR2	PLCC–28	500 Units/Reel
MC100E175FN	PLCC–28	37 Units/Rail
MC100E175FNR2	PLCC–28	500 Units/Reel

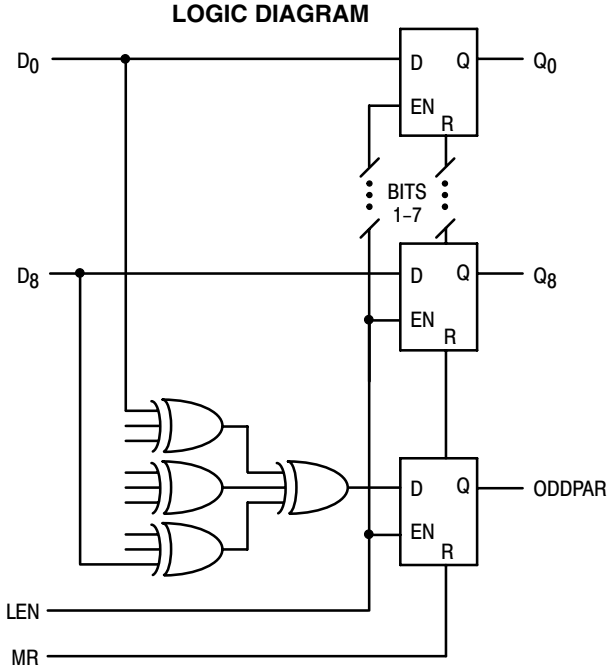
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN	FUNCTION
$D_0 – D_8$	ECL Data Inputs
LEN	ECL Latch Enable
MR	ECL Master Reset
$Q_0 – Q_8$	ECL Data Outputs
ODDPAR	ECL Parity Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

FUNCTION TABLE

D	EN	MR	Q	ODDPAR
H	L	L	H	H if odd no. of Dn HIGH
L	L	L	L	H if odd no. of Dn HIGH
X	H	L	Q_0	Q_0
X	X	H	L	L

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		110	132		110	132		110	132	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		110	132		110	132		110	132	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		110	132		110	132		127	152	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		110	132		110	132		127	152	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH}	Propagation Delay to Output										ps
t_{PHL}	D to Q	450	600	800	450	600	800	450	600	800	
	D to ODDPAR	850	1150	1450	850	1150	1450	850	1150	1450	
	LEN to Q	525	700	900	525	700	900	525	700	900	
	LEN to ODDPAR	525	700	900	525	700	900	525	700	900	
	MR to Q(t_{PHL})	525	700	900	525	700	900	525	700	900	
	MR to ODDPAR(t_{PHL})	525	700	900	525	700	900	525	700	900	
t_s	Setup Time										ps
	D (Q)	275	100		275			275			
	D (ODDPAR)	900	700		900			900			
t_h	Hold Time										ps
	D (Q)	175	–100		175			175			
	D (ODDPAR)	– 300	– 70		– 300			– 300			
t_{RR}	Reset Recovery Time	850	600		850	600		850	600		ps
t_{SKEW}	Within-Device Skew (Note 2.)										ps
	LEN, MR		75			75			75		
	D to Q		75			75			75		
	D to ODDPAR		200			200			200		
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r	Rise/Fall Times										ps
t_f	(20 - 80%)	300	500	800	300	500	800	300	500	800	

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.

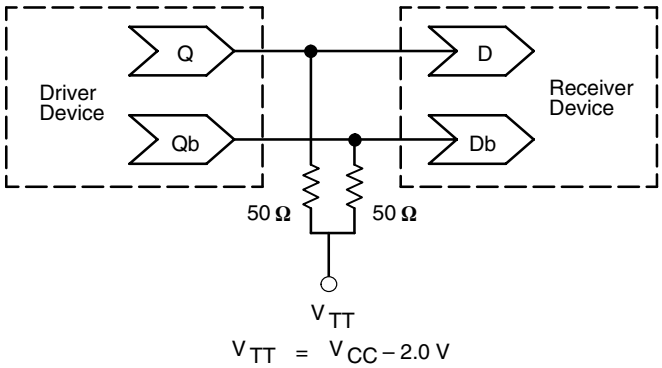


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
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AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E193, MC100E193

5V ECL Error Detection/ Correction Circuit

The MC10E/100E193 is an error detection and correction (EDAC) circuit. Modified Hamming parity codes are generated on an 8-bit word according to the pattern shown in the logic symbol. The P5 output gives the parity of the whole word. The word parity is also provided at the PGEN pin, after Odd/Even parity control and gating with the BPAR input. This output also feeds to a 1-bit shiftable register, for use as part of a scan ring.

Used in conjunction with 12-bit parity generators such as the E160, a SECDED (single error correction, double error detection) error system can be designed for a multiple of an 8-bit word.

The 100 Series contains temperature compensation.

- Hamming Code Generation
- 8-Bit Word, Expandable
- Provides Parity of Whole Word
- Scannable Parity Register
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 1 KV HBM, > 75 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 368 devices

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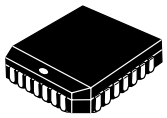
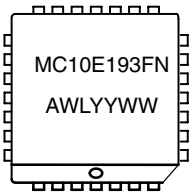


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAMS



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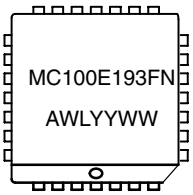


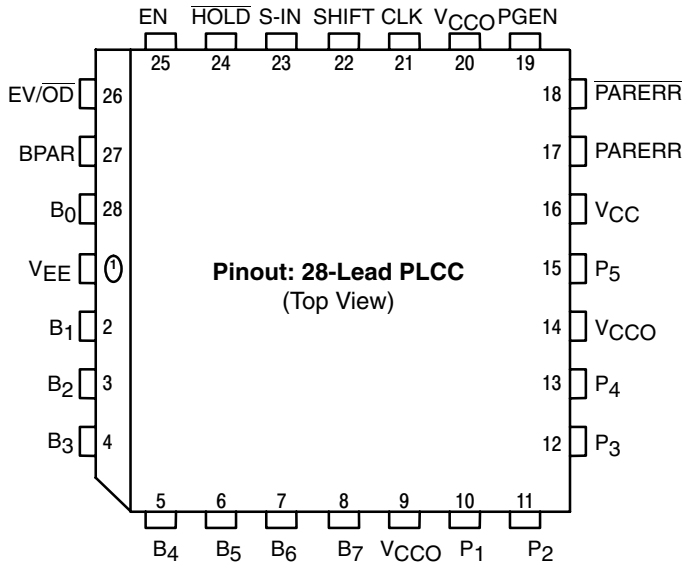
28 1

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E193FN	PLCC–28	37 Units/Rail
MC10E193FNR2	PLCC–28	500 Units/Reel
MC100E193FN	PLCC–28	37 Units/Rail
MC100E193FNR2	PLCC–28	500 Units/Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



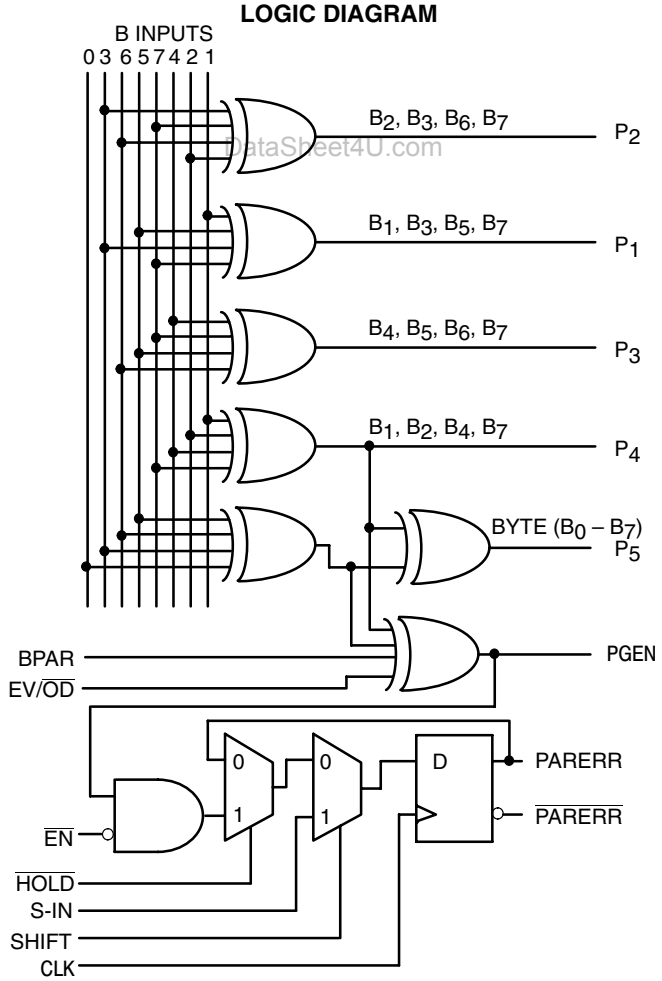
* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

PIN	FUNCTION
B0–B6	ECL Bit Inputs
P1–P5	ECL Parity Outputs
PARERR, $\overline{\text{PARERR}}$	ECL Parity Error Outputs
PGEN	ECL Word Parity Generator Output
CLK	ECL Clock Input
SHIFT	ECL Shift Input (Active–High)
S–IN	ECL Serial Data Input
$\overline{\text{HOLD}}$	ECL Hold (Active–Low)
EN	ECL Enable (Active–Low)
EV/$\overline{\text{DD}}$	ECL Even/Odd Contact
BPAR	ECL Bit Parity Gate Input
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

LOGIC DIAGRAM



MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		112	134		112	134		112	134	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		112	134		112	134		112	134	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		112	134		112	134		129	155	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		112	134		112	134		129	155	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH}	Propagation Delay to Output										ps
t_{PHL}	B to P1, P2, P3, P4	350	700	1000	350	700	1000	350	700	1000	
	B to P5	400	775	1150	400	775	1150	400	775	1150	
	EV/$\overline{OD}$, BPAR to PGEN	350	650	850	350	650	850	350	650	850	
	B to PGEN	600	1000	1450	600	1000	1450	600	1000	1450	
	CLK to PARERR	300	550	850	300	550	850	300	550	850	
t_S	Setup Time										ps
	SHIFT	400	150		400	150		400	150		
	S-IN	300	50		300	50		300	50		
	$\overline{HOLD}$	750	350		750	350		750	350		
	$\overline{EN}$	500	250		500	250		500	250		
	EV/$\overline{OD}$	1300	850		1300	850		1300	850		
	BPAR	1300	850		1300	850		1300	850		
	B	1700	1100		1700	1100		1700	1100		
t_h	Hold Time										ps
	SHIFT	200	–150		200	–150		200	–150		
	S-IN	300	– 50		300	– 50		300	– 50		
	$\overline{HOLD}$	100	– 350		100	– 350		100	– 350		
	$\overline{EN}$	100	– 250		100	– 250		100	– 250		
	EV/$\overline{OD}$	– 200	– 850		– 200	– 850		– 200	– 850		
	BPAR	– 200	– 850		– 200	– 850		– 200	– 850		
	B	– 300	–1100		– 300	–1100		– 300	–1100		
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r	Rise/Fall Times										ps
t_f	(20 - 80%)	300	700	1100	300	700	1100	300	700	1100	

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.

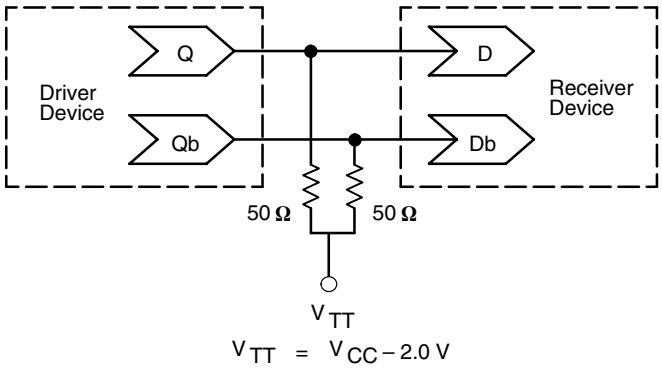


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E195, MC100E195

5V ECL Programmable Delay Chip

The MC10E/100E195 is a programmable delay chip (PDC) designed primarily for clock de-skewing and timing adjustment. It provides variable delay of a differential ECL input transition.

The delay section consists of a chain of gates organized as shown in the logic symbol. The first two delay elements feature gates that have been modified to have delays 1.25 and 1.5 times the basic gate delay of approximately 80 ps. These two elements provide the E195 with a digitally-selectable resolution of approximately 20 ps. The required device delay is selected by the seven address inputs D[0:6], which are latched on chip by a high signal on the latch enable (LEN) control.

Because the delay programmability of the E195 is achieved by purely differential ECL gate delays the device will operate at frequencies of >1.0 GHz while maintaining over 600 mV of output swing.

The E195 thus offers very fine resolution, at very high frequencies, that is selectable entirely from a digital input allowing for very accurate system clock timing.

An eighth latched input, D7, is provided for cascading multiple PDC's for increased programmable range. The cascade logic allows full control of multiple PDC's, at the expense of only a single added line to the data bus for each additional PDC, without the need for any external gating.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

- 2.0 ns Worst Case Delay Range
- ≈20 ps/Delay Step Resolution
- >1.0 GHz Bandwidth
- On Chip Cascade Circuitry
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 200 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8",
  Oxygen Index 28 to 34
- Transistor Count = 368 devices

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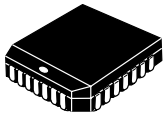
MARKING DIAGRAMS



PLCC–28
FN SUFFIX
CASE 776

28 1

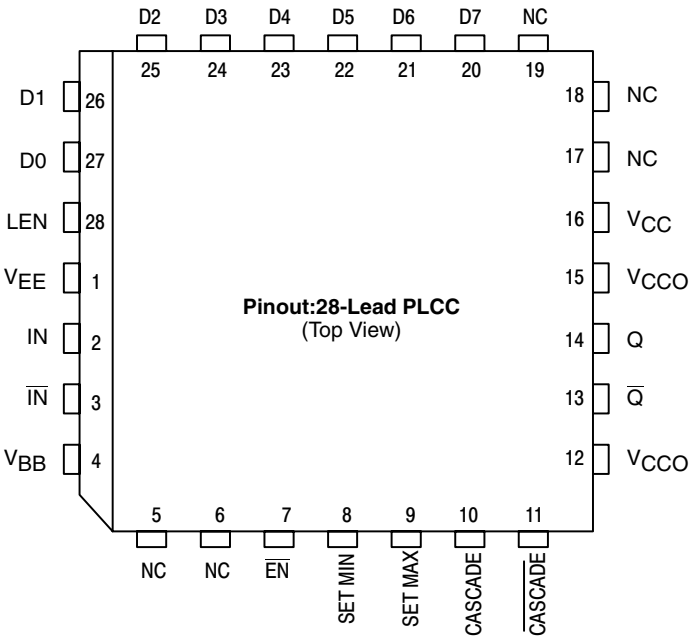
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

28 1

ORDERING INFORMATION

Device	Package	Shipping
MC10E195FN	PLCC–28	37 Units/Rail
MC10E195FNR2	PLCC–28	500 Units/Reel
MC100E195FN	PLCC–28	37 Units/Rail
MC100E195FNR2	PLCC–28	500 Units/Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



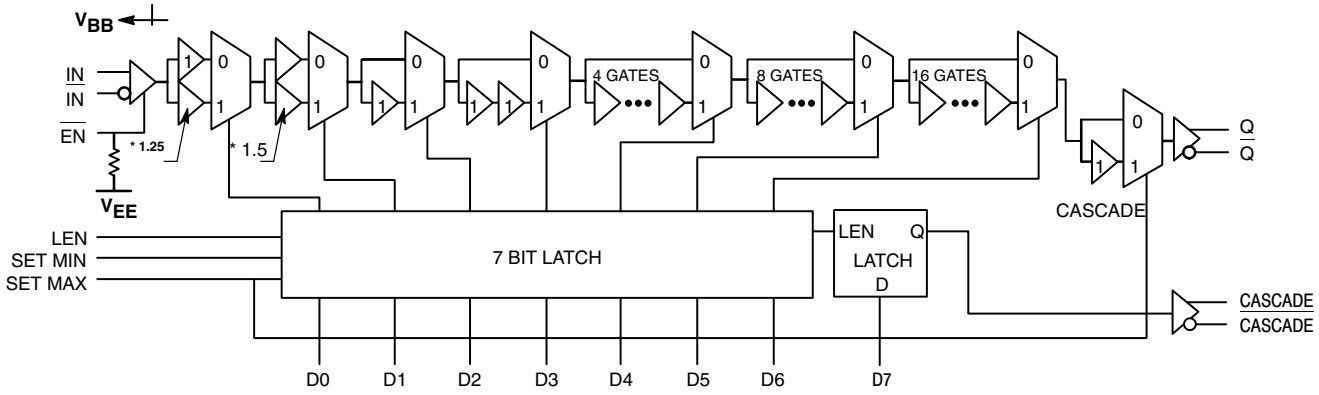
* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

PIN	FUNCTION
IN/$\overline{IN}$	ECL Signal Input
$\overline{EN}$	ECL Input Enable
D[0:7]	ECL Mux Select Inputs
Q/$\overline{Q}$	ECL Signal Output
LEN	ECL Latch Enable
SET MIN	ECL Min Delay Set
SET MAX	ECL Max Delay Set
CASCADE, $\overline{CASCADE}$	ECL Cascade Signal
V_{BB}	Reference Voltage Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

LOGIC DIAGRAM – SIMPLIFIED



* DELAYS ARE 25% OR 50% LONGER THAN STANDARD (STANDARD ≈ 80 PS)

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		130	156		130	156		130	156	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage (Single Ended)	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
V_{BB}	Output Voltage Reference	3.62		3.63	3.65		3.75	3.69		3.81	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)		TBD			TBD			TBD		V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		130	156		130	156		130	156	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
V_{BB}	Output Voltage Reference	–1.38		–1.37	–1.35		–1.25	–1.31		–1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)		TBD			TBD			TBD		V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		130	156		130	156		150	179	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)		TBD			TBD			TBD		V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		130	156		130	156		150	179	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)		TBD			TBD			TBD		V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency					> 1.0					GHz
t_{PLH} t_{PHL}	Propagation Delay										ps
	IN to Q; Tap = 0	1210	1360	1510	1240	1390	1540	1440	1590	1765	
	IN to Q; Tap = 127	3200	3570	3970	3270	3630	4030	3885	4270	4710	
	$\overline{EN}$ to Q; Tap = 0	1250	1450	1650	1275	1475	1675	1350	1650	1950	
	D7 to CASCADE	300	450	700	300	450	700	300	450	700	
t_{RANGE}	Programmable Range t_{PD} (max) – t_{PD} (min)	2000	2175		2050	2240		2375	2580		ps
Δt	Step Delay (Note 7.)										ps
	D0 High		17			17.5			21		
	D1 High		34			35			42		
	D2 High	55	68	105	55	70	105	65	84	120	
	D3 High	115	136	180	115	140	180	140	168	205	
	D4 High	250	272	325	250	280	325	305	336	380	
	D5 High	505	544	620	515	560	620	620	672	740	
	D6 High	1000	1088	1190	1030	1120	1220	1240	1344	1450	
Lin	Linearity (Note 8.)	D1	D0		D1	D0		D1	D0		
t_{SKEW}	Duty Cycle Skew t_{PHL}–t_{PLH} (Note 2.)		±30			±30			±30		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_s	Setup Time										ps
	D to LEN	200	0		200	0		200	0		
	D to IN (Note 3.)	800			800			800			
	$\overline{EN}$ to IN (Note 4.)	200			200			200			
t_h	Hold Time										ps
	LEN to D	500	250		500	250		500	250		
	IN to $\overline{EN}$ (Note 5.)	0			0			0			
t_R	Release Time										ps
	$\overline{EN}$ to IN (Note 6.)	300			300			300			
	SET MAX to LEN	800			800			800			
	SET MIN to LEN	800			800			800			
t_{jit}	Jitter (Note 9.)		<5.0			<5.0			<5.0		ps
t_r t_f	Output Rise/Fall Time										ps
	20–80% (Q)	125	225	325	125	225	325	125	225	325	
	20–80% (CASCADE)	300	450	650	300	450	650	300	450	650	

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Duty cycle skew guaranteed only for differential operation measured from the cross point of the input to the cross point of the output.
3. This setup time defines the amount of time prior to the input signal the delay tap of the device must be set.
4. This setup time is the minimum time that $\overline{EN}$ must be asserted prior to the next transition of IN/$\overline{IN}$ to prevent an output response greater than ±75 mV to that IN/$\overline{IN}$ transition.
5. This hold time is the minimum time that $\overline{EN}$ must remain asserted after a negative going IN or positive going $\overline{IN}$ to prevent an output response greater than ±75 mV to that IN/IN transition.
6. This release time is the minimum time that $\overline{EN}$ must be deasserted prior to the next IN/$\overline{IN}$ transition to ensure an output response that meets the specified IN to Q propagation delay and transition times.
7. Specification limits represent the amount of delay added with the assertion of each individual delay control pin. The various combinations of asserted delay control inputs will typically realize D0 resolution steps across the specified programmable range.
8. The linearity specification guarantees to which delay control input the programmable steps will be monotonic (i.e. increasing delay steps for increasing binary counts on the control inputs Dn). Typically the device will be monotonic to the D0 input, however under worst case conditions and process variation, delays could decrease slightly with increasing binary counts when the D0 input is the LSB. With the D1 input as the LSB the device is guaranteed to be monotonic over all specified environmental conditions and process variation.
9. The jitter of the device is less than what can be measured without resorting to very tedious and specialized measurement techniques.

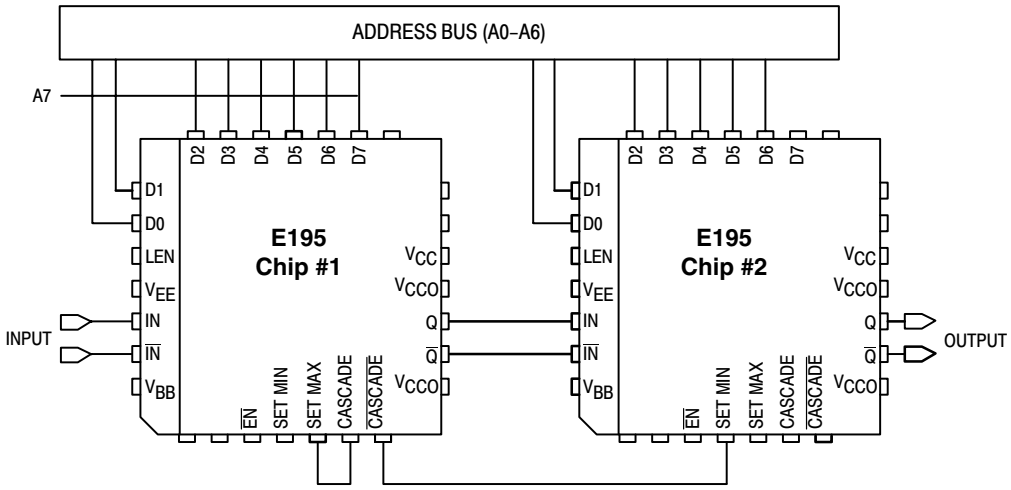


Figure 1. Cascading Interconnect Architecture

Cascading Multiple E195's

To increase the programmable range of the E195 internal cascade circuitry has been included. This circuitry allows for the cascading of multiple E195's without the need for any external gating. Furthermore this capability requires only one more address line per added E195. Obviously cascading multiple PDC's will result in a larger programmable range however this increase is at the expense of a longer minimum delay.

Figure 1 illustrates the interconnect scheme for cascading two E195's. As can be seen, this scheme can easily be expanded for larger E195 chains. The D7 input of the E195 is the cascade control pin. With the interconnect scheme of Figure 1 when D7 is asserted it signals the need for a larger programmable range than is achievable with a single device.

An expansion of the latch section of the block diagram is pictured below. Use of this diagram will simplify the explanation of how the cascade circuitry works. When D7 of chip #1 above is low the cascade output will also be low while the cascade bar output will be a logical high. In this condition the SET MIN pin of chip #2 will be asserted and thus all of the latches of chip #2 will be reset and the device will be set at its minimum delay. Since the RESET and SET inputs of the latches are overriding any changes on the A0–A6 address bus will not affect the operation of chip #2.

Chip #1 on the other hand will have both SET MIN and SET MAX de-asserted so that its delay will be controlled entirely by the address bus A0–A6. If the delay needed is greater than can be achieved with 31.75 gate delays (1111111 on the A0–A6 address bus) D7 will be asserted to signal the need to cascade the delay to the next E195 device. When D7 is asserted the SET MIN pin of chip #2 will be de-asserted and the delay will be controlled by the A0–A6 address bus. Chip #1 on the other hand will have its SET MAX pin asserted resulting in the device delay to be independent of the A0–A6 address bus.

When the SET MAX pin of chip #1 is asserted the D0 and D1 latches will be reset while the rest of the latches will be set. In addition, to maintain monotonicity an additional gate delay is selected in the cascade circuitry. As a result when D7 of chip #1 is asserted the delay increases from 31.75 gates to 32 gates. A 32 gate delay is the maximum delay setting for the E195.

To expand this cascading scheme to more devices one simply needs to connect the D7 input and CASCADE outputs of the current most significant E195 to the new most significant E195 in the same manner as pictured in Figure 1. The only addition to the logic is the increase of one line to the address bus for cascade control of the second PDC.

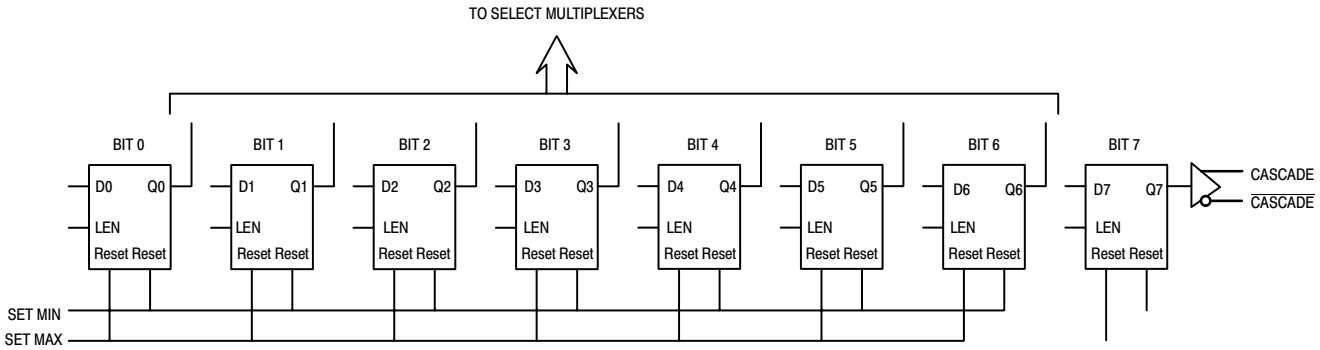


Figure 2. Expansion of the Latch Section of the E195 Block Diagram

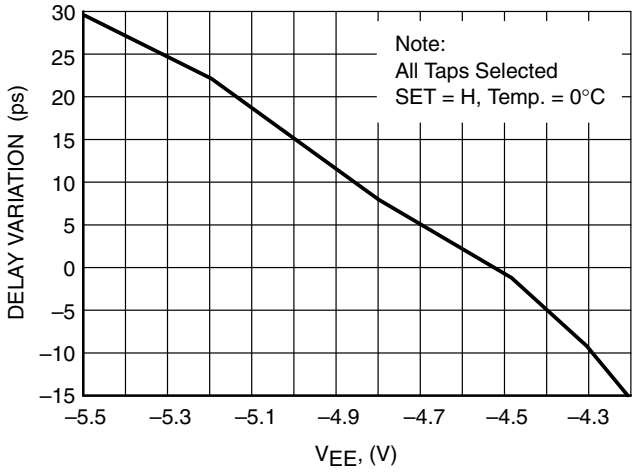


Figure 3. Change in Delay vs. Change in Supply Voltage

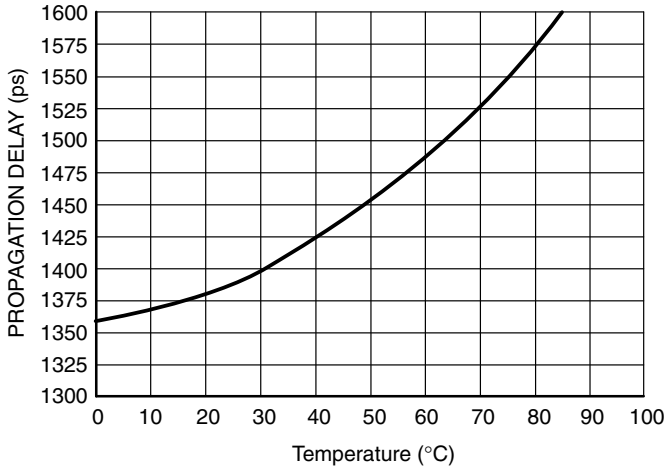


Figure 4. Delay vs. Temperature (Fixed Path)

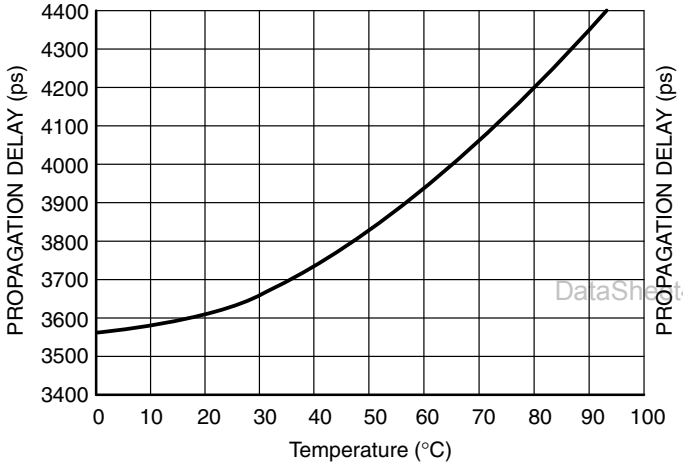


Figure 5. Delay vs. Temperature (Max. Delay).

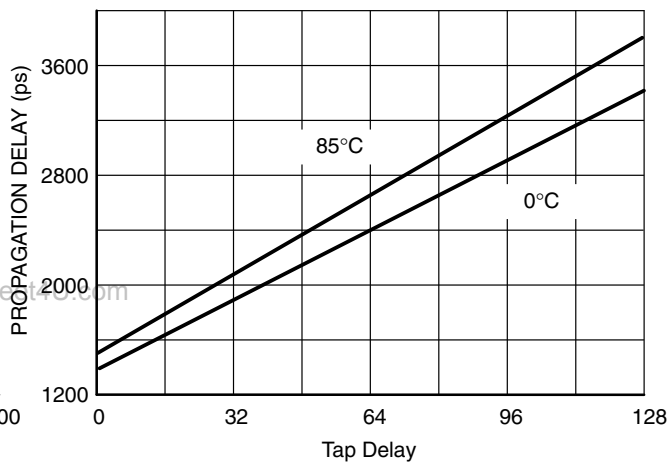


Figure 6. 100E195 Temperature Effects on Delay.

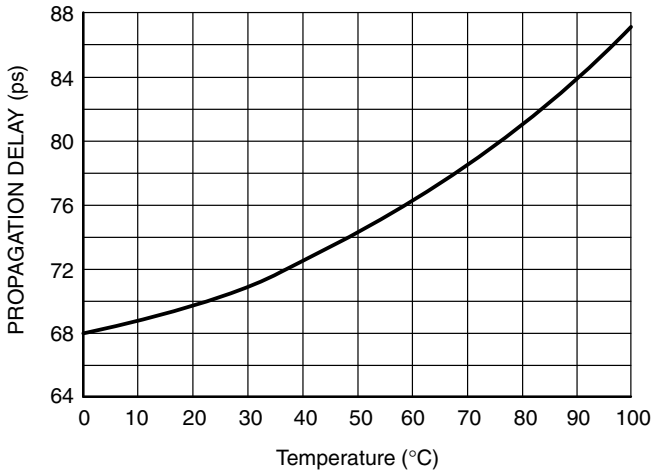


Figure 7. Delay vs. Temperature (Per Gate).

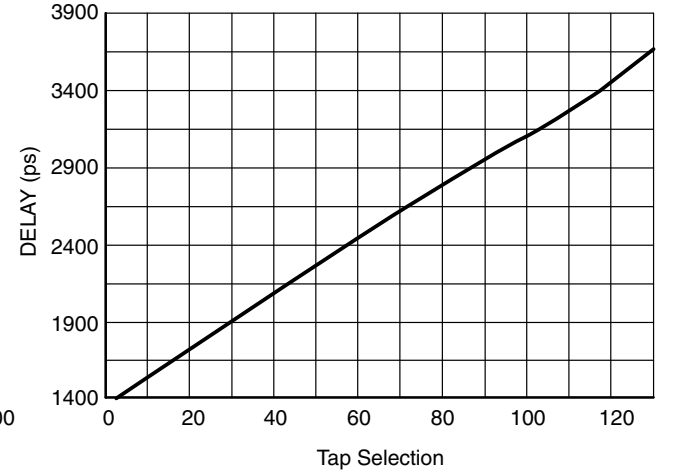


Figure 8. E195 Delay Linearity.

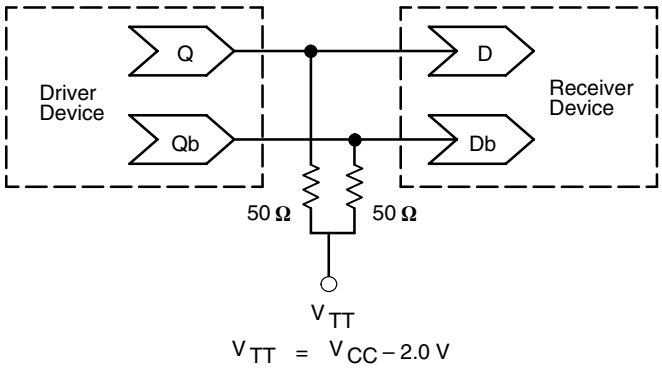


Figure 9. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E196, MC100E196

5V ECL Programmable Delay Chip

The MC10E/100E196 is a programmable delay chip (PDC) designed primarily for very accurate differential ECL input edge placement applications.

The delay section consists of a chain of gates and a linear ramp delay adjust organized as shown in the logic symbol. The first two delay elements feature gates that have been modified to have delays 1.25 and 1.5 times the basic gate delay of approximately 80 ps. These two elements provide the E196 with a digitally-selectable resolution of approximately 20 ps. The required device delay is selected by the seven address inputs D[0:6], which are latched on chip by a high signal on the latch enable (LEN) control.

The FTUNE input takes an analog voltage and applies it to an internal linear ramp for reducing the 20 ps L.S.B. minimum resolution still further. The FTUNE input is what differentiates the E196 from the E195.

An eighth latched input, D7, is provided for cascading multiple PDC's for increased programmable range. The cascade logic allows full control of multiple PDC's, at the expense of only a single added line to the data bus for each additional PDC, without the need for any external gating.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

- 2.0 ns Worst Case Delay Range
- ≈20 ps/Delay Step Resolution
- Linear Input for Tighter Resolution
- >1.0 GHz Bandwidth
- On Chip Cascade Circuitry
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 1 KV HBM, > 75 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8",
  Oxygen Index 28 to 34
- Transistor Count = 425 devices

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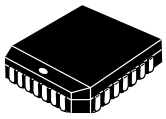
MARKING DIAGRAMS



PLCC–28
FN SUFFIX
CASE 776

28 1

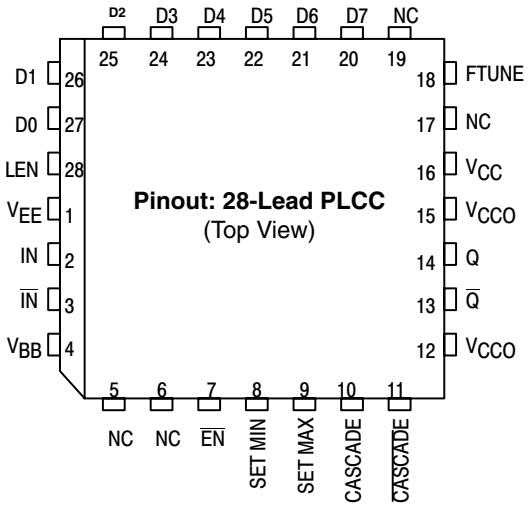
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

28 1

ORDERING INFORMATION

Device	Package	Shipping
MC10E196FN	PLCC–28	37 Units/Rail
MC10E196FNR2	PLCC–28	500 Units/Reel
MC100E196FN	PLCC–28	37 Units/Rail
MC100E196FNR2	PLCC–28	500 Units/Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



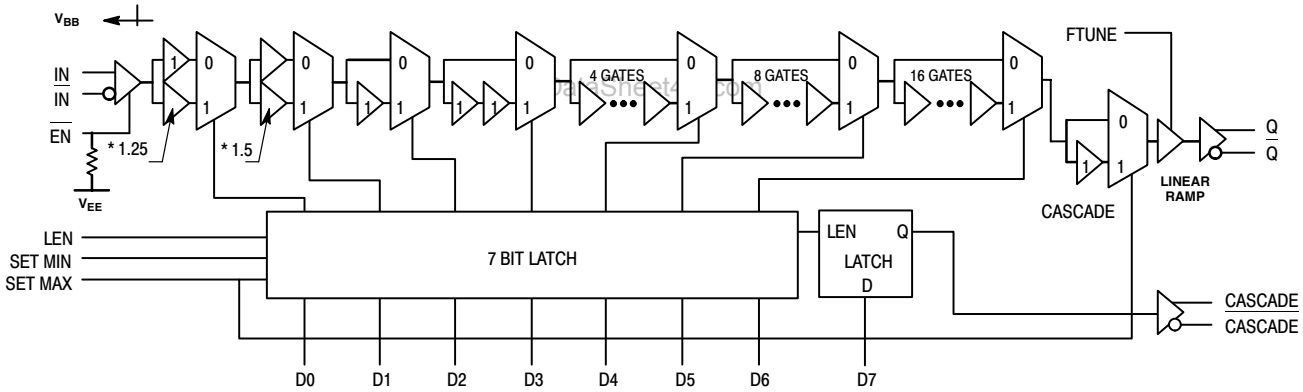
* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

PIN	FUNCTION
IN/$\overline{IN}$	ECL Signal Input
$\overline{EN}$	ECL Input Enable (H Forces Q Low)
D[0:7]	ECL Mux Select Inputs
Q/$\overline{Q}$	ECL Signal Output
LEN	ECL Latch Enable
SET MIN	ECL Min Delay Set
SET MAX	ECL Max Delay Set
CASCADE	ECL Cascade Signal
FTUNE	ECL Linear Voltage Input
V_{BB}	Reference Voltage Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

LOGIC DIAGRAM – SIMPLIFIED



* DELAYS ARE 25% OR 50% LONGER THAN STANDARD (STANDARD ≈ 80 PS)

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		130	156		130	156		130	156	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage (Single Ended)	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
V_{BB}	Output Voltage Reference	3.62		3.63	3.65		3.75	3.69		3.81	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)		TBD			TBD			TBD		V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		130	156		130	156		130	156	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
V_{BB}	Output Voltage Reference	–1.38		–1.37	–1.35		–1.25	–1.31		–1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)		TBD			TBD			TBD		V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		130	156		130	156		150	179	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)		TBD			TBD			TBD		V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		130	156		130	156		150	179	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)		TBD			TBD			TBD		V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

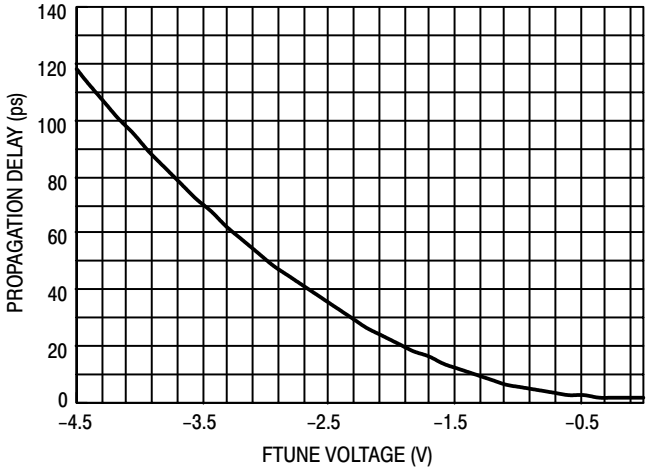
AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{MAX}	Maximum Toggle Frequency		TBD			>1.0			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay										ps
	IN to Q; Tap = 0	1210	1360	1510	1240	1390	1540	1440	1590	1765	
	IN to Q; Tap = 127	3320	3570	3820	3380	3630	3880	3920	4270	4720	
	$\overline{EN}$ to Q; Tap = 0	1250	1450	1650	1275	1475	1675	1350	1650	1950	
	D7 to CASCADE	300	450	700	300	450	700	300	450	700	
t_{RANGE}	Programmable Range										ps
	t_{PD} (max) – t_{PD} (min)	2000	2175		2050	2240		2375	2580		
Δt	Step Delay (Note 7.)										ps
	D0 High		17			17.5			21		
	D1 High		34			35			42		
	D2 High	55	68	105	55	70	105	65	84	120	
	D3 High	115	136	180	115	140	180	140	168	205	
	D4 High	250	272	325	250	280	325	305	336	380	
	D5 High	505	544	620	515	560	620	620	672	740	
	D6 High	1000	1088	1190	1030	1120	1220	1240	1344	1450	
Lin	Linearity (Note 8.)	D1	D0		D1	D0		D1	D0		
t_{SKEW}	Duty Cycle Skew										ps
	t_{PHL}–t_{PLH} (Note 2.)		±30			±30			±30		
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_s	Setup Time										ps
	D to LEN	200	0		200	0		200	0		
	D to IN (Note 3.)	800			800			800			
	$\overline{EN}$ to IN (Note 4.)	200			200			200			
t_h	Hold Time										ps
	LEN to D	500	250		500	250		500	250		
	IN to $\overline{EN}$ (Note 5.)	0			0			0			
t_R	Release Time										ps
	$\overline{EN}$ to IN (Note 6.)	300			300			300			
	SET MAX to LEN	800			800			800			
	SET MIN to LEN	800			800			800			
t_{jit}	Jitter (Note 9.)		<5.0			<5.0			<5.0		ps
t_r t_f	Output Rise/Fall Time										ps
	20–80% (Q)	125	225	325	125	225	325	125	225	325	
	20–80% (CASCADE)	300	450	650	300	450	650	300	450	650	

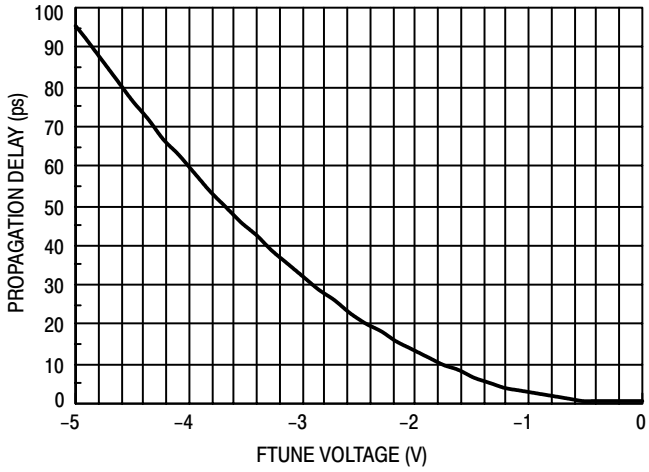
1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Duty cycle skew guaranteed only for differential operation measured from the cross point of the input to the cross point of the output.
3. This setup time defines the amount of time prior to the input signal the delay tap of the device must be set.
4. This setup time is the minimum time that $\overline{EN}$ must be asserted prior to the next transition of IN/$\overline{IN}$ to prevent an output response greater than ±75 mV to that IN/$\overline{IN}$ transition.
5. This hold time is the minimum time that $\overline{EN}$ must remain asserted after a negative going IN or positive going $\overline{IN}$ to prevent an output response greater than ±75 mV to that IN/IN transition.
6. This release time is the minimum time that $\overline{EN}$ must be de–asserted prior to the next IN/$\overline{IN}$ transition to ensure an output response that meets the specified IN to Q propagation delay and transition times.
7. Specification limits represent the amount of delay added with the assertion of each individual delay control pin. The various combinations of asserted delay control inputs will typically realize D0 resolution steps across the specified programmable range.
8. The linearity specification guarantees to which delay control input the programmable steps will be monotonic (i.e. increasing delay steps for increasing binary counts on the control inputs Dn). Typically the device will be monotonic to the D0 input, however under worst case conditions and process variation, delays could decrease slightly with increasing binary counts when the D0 input is the LSB. With the D1 input as the LSB the device is guaranteed to be monotonic over all specified environmental conditions and process variation.
9. The jitter of the device is less than what can be measured without resorting to very tedious and specialized measurement techniques.

ANALOG INPUT CHARACTERISTICS

Ftune = V_{CC} to V_{EE}



Propagation Delay versus Ftune Voltage (100E196)



Propagation Delay versus Ftune Voltage (10E196)

USING THE FTUNE ANALOG INPUT

The analog FTUNE pin on the E196 device is intended to add more delay in a tunable gate to enhance the 20 ps resolution capabilities of the fully digital E195. The level of resolution obtained is dependent on the number of increments applied to the appropriate range on the FTUNE pin.

To provide this further level of resolution (See Logic Diagram), the FTUNE pin must be capable of adjusting the additional delay finer than the 20 ps digital resolution. From the provided graphs one sees that this requirement is easily achieved as over the entire FTUNE voltage range a 100 ps additional delay can be achieved. This extra analog range ensures that the FTUNE pin will be capable even under worst case conditions of covering the digital resolution.Typically the analog input will be driven by an external DAC to provide a digital control with very fine analog output steps. The final resolution of the device will be dependent on the width of the DAC chosen.

To determine the voltage range necessary for the FTUNE input, the graphs provided should be used. As an example if a tuning range of 40 ps is selected to cover worst case conditions and ensure coverage of the digital range, from the 100E196 graph a voltage range of –3.25 V to –4.0 V would be necessary on the FTUNE pin. Obviously there are numerous voltage ranges which can be used to cover a given delay range, users are given the flexibility to determine which one best fits their designs.

Cascading Multiple E196's

To increase the programmable range of the E196 internal cascade circuitry has been included. This circuitry allows for the cascading of multiple E196's without the need for any external gating. Furthermore this capability requires only one more address line per added E196. Obviously cascading multiple PDC's will result in a larger programmable range, however, this increase is at the expense of a longer minimum delay.

Figure 1 illustrates the interconnect scheme for cascading two E196's. As can be seen, this scheme can easily be expanded for larger E196 chains. The D7 input of the E196 is the cascade control pin. With the interconnect scheme of Figure 1 when D7 is asserted it signals the need for a larger programmable range than is achievable with a single device.

An expansion of the latch section of the block diagram is pictured below. Use of this diagram will simplify the explanation of how the cascade circuitry works. When D7 of chip #1 above is low the cascade output will also be low while the cascade bar output will be a logical high. In this condition the SET MIN pin of chip #2 will be asserted and thus all of the latches of chip #2 will be reset and the device will be set at its minimum delay. Since the RESET and SET inputs of the latches are overriding any changes on the A0–A6 address bus will not affect the operation of chip #2.

Chip #1 on the other hand will have both SET MIN and SET MAX de-asserted so that its delay will be controlled entirely by the address bus A0–A6. If the delay needed is greater than can be achieved with 31.75 gate delays (1111111 on the A0–A6 address bus) D7 will be asserted to signal the need to cascade the delay to the next E196 device. When D7 is asserted the SET MIN pin of chip #2 will be

de-asserted and the delay will be controlled by the A0–A6 address bus. Chip #1 on the other hand will have its SET MAX pin asserted resulting in the device delay to be independent of the A0–A6 address bus.

When the SET MAX pin of chip #1 is asserted the D0 and D1 latches will be reset while the rest of the latches will be set. In addition, to maintain monotonicity an additional gate delay is selected in the cascade circuitry. As a result when D7 of chip #1 is asserted the delay increases from 31.75 gates to 32 gates. A 32 gate delay is the maximum delay setting for the E196.

When cascading multiple PDC's it will prove more cost effective to use a single E196 for the MSB of the chain while using E195 for the lower order bits. This is due to the fact that only one fine tune input is needed to further reduce the delay step resolution.

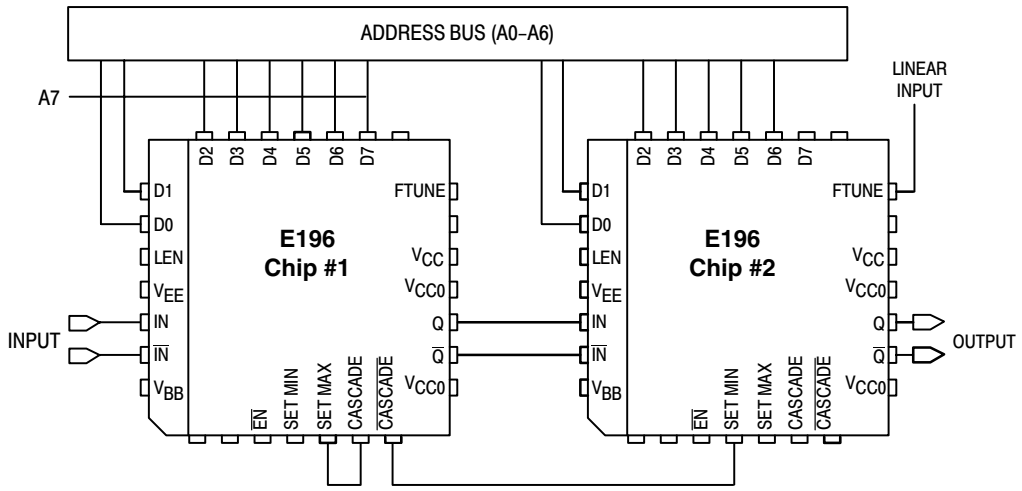


Figure 1. Cascading Interconnect Architecture

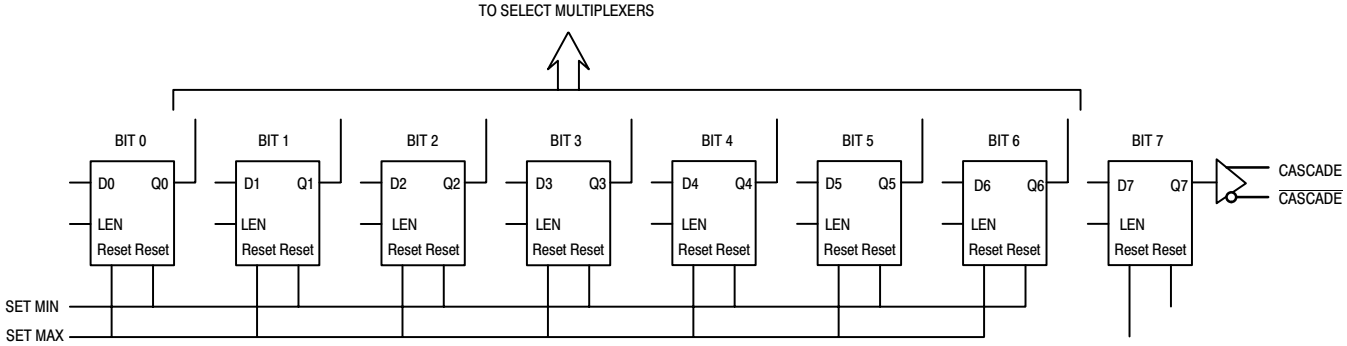


Figure 2. Expansion of the Latch Section of the E196 Block Diagram

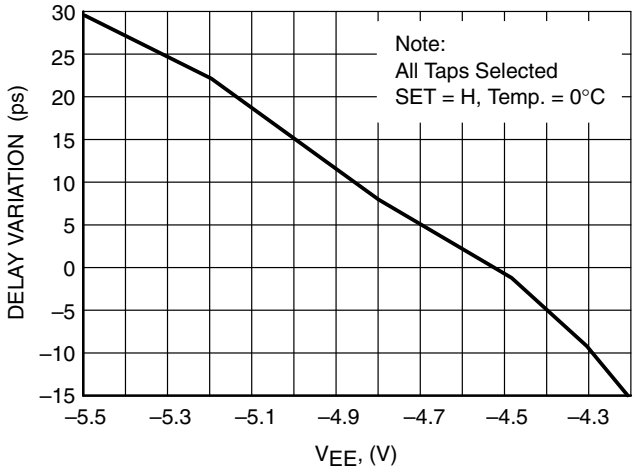


Figure 3. Change in Delay vs. Change in Supply Voltage

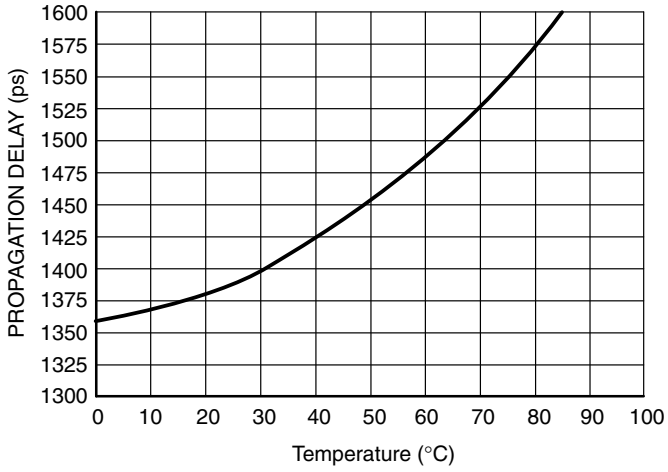


Figure 4. Delay vs. Temperature (Fixed Path)

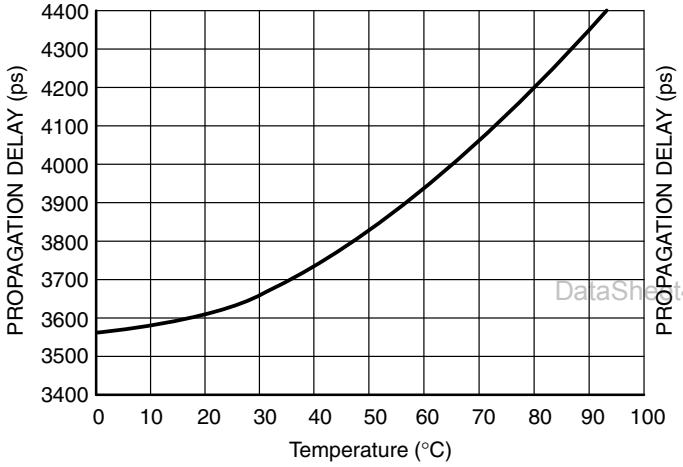


Figure 5. Delay vs. Temperature (Max. Delay).

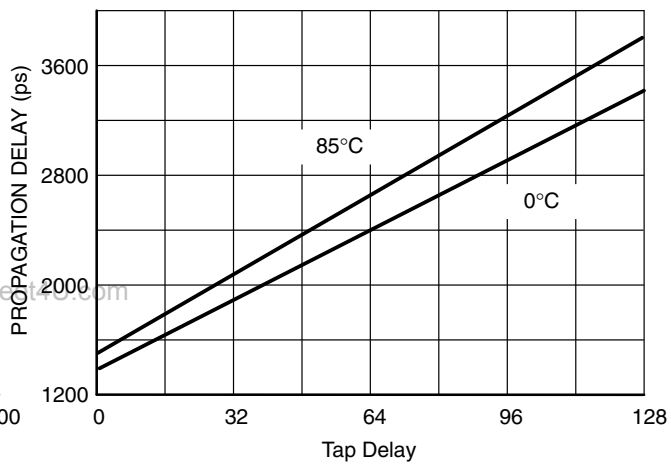


Figure 6. 100E195 Temperature Effects on Delay.

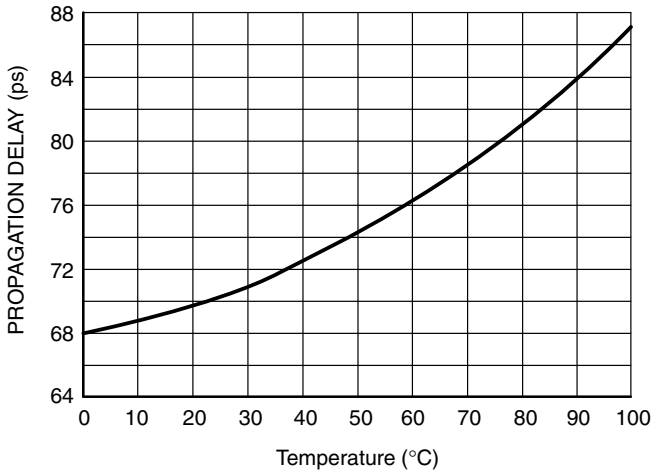


Figure 7. Delay vs. Temperature (Per Gate).

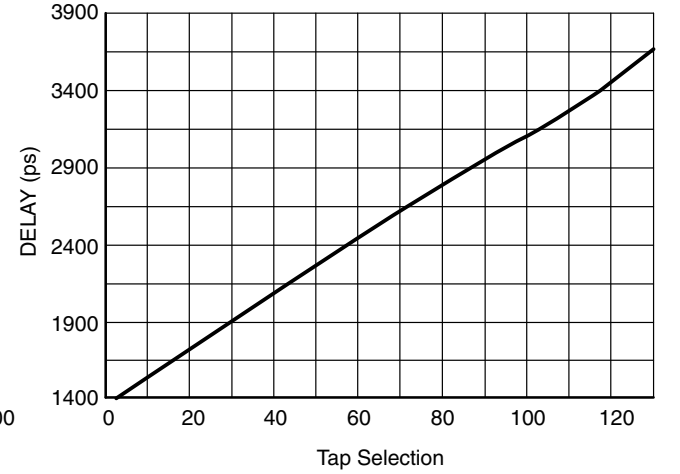


Figure 8. E195 Delay Linearity.

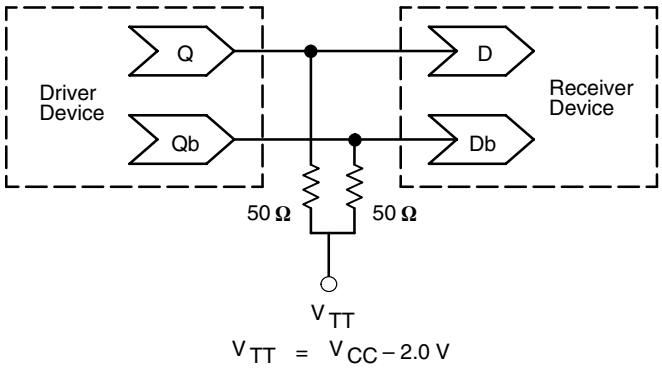


Figure 9. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E197

Advance Information
5V ECL Data Separator

The MC10E197 is an integrated data separator designed for use in high speed hard disk drive applications. With data rate capabilities of up to 50 Mb/s the device is ideally suited for today's and future state-of-the-art hard disk designs.

The E197 is typically driven by a pulse detector which reads the magnetic information from the storage disk and changes it into ECL pulses. The device is capable of operating on both 2:7 and 1:7 RLL coding schemes. Note that the E197 does not do any decoding but rather prepares the disk data for decoding by another device.

For applications with higher data rate needs, such as tape drive systems, the device accepts an external VCO. The frequency capability of the integrated VCO is the factor which limits the device to 50 Mb/s.

A special anti-equivocation circuit has been employed to ensure timely lock-up when the arriving data and VCO edges are coincident.

Unlike the majority of the devices in the ECLinPS family, the E197 is available in only 10H compatible ECL. The device is available in the standard 28-lead PLCC.

Since the E197 contains both analog and digital circuitry, separate supply and ground pins have been provided to minimize noise coupling inside the device. The device can operate on either standard negative ECL supplies or, as is more common, on positive voltage supplies.

The 100 Series contains temperature compensation.

- 2:7 and 1:7 RLL Format Compatible
- Fully Integrated VCO for 50 Mb/s Operation
- External VCO Input for Higher Operating Frequency
- Anti-equivocation Circuitry to Ensure PLL Lock
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 1 KV HBM, > 75 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8",
  Oxygen Index 28 to 34
- Transistor Count = 483 devices

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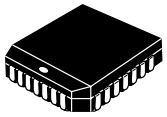
MARKING DIAGRAMS



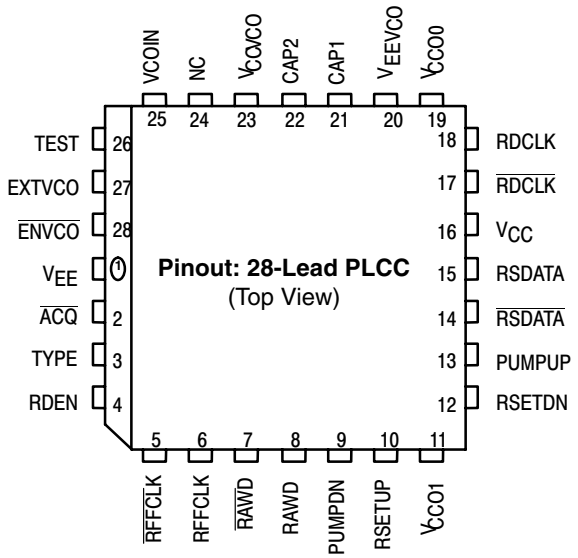
PLCC–28
FN SUFFIX
CASE 776

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E197FN	PLCC–28	37 Units/Rail
MC10E197FNR2	PLCC–28	500 Units/Reel
MC100E197FN	PLCC–28	37 Units/Rail
MC100E197FNR2	PLCC–28	500 Units/Reel

This document contains information on a new product. Specifications and information herein are subject to change without notice.



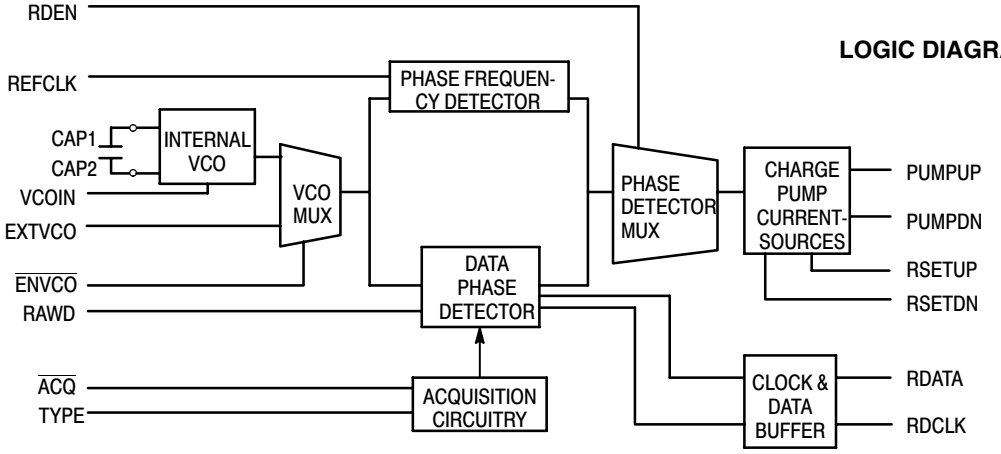
LOGIC DIAGRAM AND PINOUT ASSIGNMENT

* All V_{CC} and V_{CCOX} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTIONS

PIN	FUNCTION
REFCLK	ECL Reference clock equivalent to one clock cycle per decoding window.
REFCLK	ECL Reference clock equivalent to one clock cycle per decoding window.
RDEN	ECL Enable data synchronizer when HIGH. When LOW enable the phase/frequency detector steered by REFCLK.
RAWD	ECL Data Input to Synchronizer logic.
VCOIN	ECL VCO control voltage input
CAP1/CAP2	ECL VCO frequency controlling capacitor inputs
$\overline{ENVCO}$	ECL VCO select pin. LOW selects the internal VCO and HIGH selects the external VCO input. Pin floats LOW when left open.
EXTVCO	ECL External VCO pin selected when ENVCO is HIGH
$\overline{ACQ}$	ECL Acquisition circuitry select pin. This pin must be driven HIGH at the end of the data sync field for some sync field types.
TYPE	ECL Selects between the two types of commonly used sync fields. When LOW it selects a sync field interspersed with 3 zeroes (2:7 RLL code). When HIGH it selects a sync field interspersed with 2 zeroes (1:7 RLL code).
TEST	ECL Input included to initialize the clock flip-flop for test purposes only. Pin should be left open (LOW) in actual application.
PUMPUP	ECL Open collector charge pump output for the signal pump
PUMPDN	ECL Open collector charge pump output for the reference pump
RSETUP	ECL Current setting resistor for the signal pump
RSETDN	ECL Current setting resistor for the reference pump
RDATA	ECL Synchronized data output
RDCLK	ECL Synchronized clock output
V_{CC}, V^{CCOX}, V_{CCVCO}	Most positive supply rails. Digital and analog supplies are independent on chip
V_{EE}, V_{EEVCO}	Most negative supply rails. Digital and analog supplies are independent on chip



LOGIC DIAGRAM

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current	90	150	180	90	150	180	90	150	180	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current	90	150	180	90	150	180	90	150	180	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

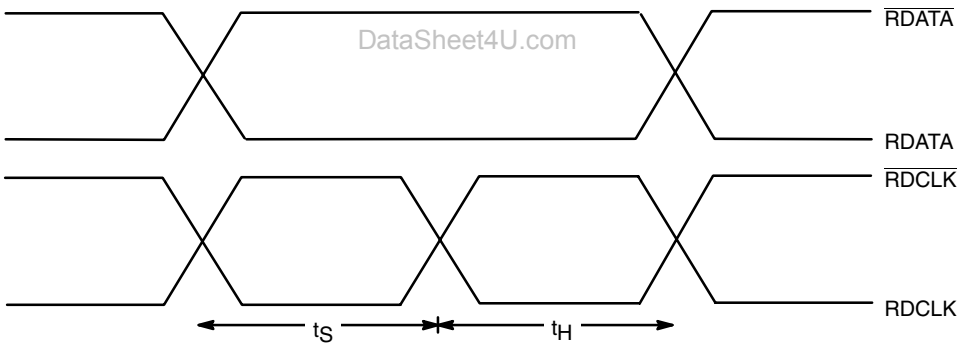
NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{VCO}	Frequency of the VCO (Note 6.)	150			150			150			MHz
	Tuning Ratio (Note 7.)	1.53		1.87	1.53		1.87	1.53		1.87	
t_S	Time from RDATA Valid to Rising Edge of RDCLK (Notes 5.)	T_{VCO} – 550			T_{VCO} – 500			T_{VCO} – 500			ps
t_H	Time from Rising Edge of RDCLK to RDATA invalid (Notes 5.)	T_{VCO}			T_{VCO}			T_{VCO}			ps
t_{SKEW}	Skew Between RDATA and $\overline{RDATA}$			300			300			300	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps

1. V_{EE} can vary +0.46 V / –0.06 V
2. Applies to the input current for each input except VCOIN
3. For a nominal set current of 3.72 mA, the resistor values for RSETUP and RSETDN should be 130Ω(0.1%). Assuming no variation between these two resistors, the current match between the PUMPUP and PUMPDN output signals should be within ±3%. I_{SET} is calculated as (V_{EE}+ 1.3v – V_{BE})/R; where R is RSETUP or RSETDN and a nominal value for V_{BE} is 0.85 volts.
4. Output leakage current of the PUMPUP or PUMPDN output signals when at a LOW level.
5. T_{VCO} is the period of the VCO.
6. The VCO frequency determined with VCOIN = V_{EE} + 0.5 volts and using a 10pF tuning capacitor.
7. The tuning ratio is defined as the ratio of f_{VCOMAX} to F_{VCOMIN} where f_{VCOMAX} is measured at VCOIN = 1.3 V + V_{EE} and f_{VCOMAX} is measured at VCOIN = 2.6 V + V_{EE}.



SETUP AND HOLD TIMING DIAGRAMS

APPLICATIONS INFORMATION

General Operation

Operation

The E197 is a phase-locked loop circuit consisting of an internal VCO, a Data Phase detector with associated acquisition circuitry, and a Phase/Frequency detector (Figure 1). In addition, an enable pin(ENVCO) is provided to disable the internal VCO and enable the external VCO input. Hence, the user has the option of supplying the VCO signal.

The E197 contains two phase detectors: a data phase detector for synchronizing to the non-periodic pulses in the read data stream during the data read mode of operation, and a phase/ frequency detector for frequency (and phase) locking to an external reference clock during the "idle" mode of operation. The read enable (RDEN) pin muxes between these two detectors.

Data Read Mode

The data pins (RAWD) are enabled when the RDEN pin is placed at a logic high level, thus enabling the Data Phase detector (Figure1) and initiating the data read mode. In this mode, the loop is servoed by the timing information taken from the positive edges of the input data pulses. This phase detector samples positive edges from the RAWD signal and generates both a pump up and pump down pulse from any edge of the input data pulse. The leading edge of the pump up pulse is time modulated by the leading edge of the data signal, whereas the rising edge of the pump up pulse is generated synchronous to the VCO clock. The falling edge of the pump down pulse is synchronous to the falling edge of the VCO clock and the rising edge of the pump down signal is synchronous to the rising edge of the VCO clock. Since both edges of the VCO are used the internal clock a duty cycle of 50%. This pulse width modulation technique is used to generate the servoing signal which drives the VCO. The pump down signal is a reference pulse which is included to provide an evenly balanced differential system, thereby allowing the synthesis of a VCO input control signal after appropriate signal processing by the loop filter.

By using suitable external filter circuitry, a control signal for input into the VCO can be generated by inverting the pump down signal, summing the inverted signal with the pump up signal and averaging the result. The polarity of this control signal is defined as zero when the data edges lead the clock by a half clock cycle. If the data edges are advanced with respect to the zero polarity data/VCO edge relationship, the control signal is defined to have a negative polarity; whereas if the VCO is advanced with respect to the zero polarity data/VCO edge relationship, the control signal is defined to have a positive polarity. If there is no data edge present at the RAWD input, the corresponding pump up and pump down outputs are not generated and the resulting control output is zero.

Acquisition Circuitry

The acquisition circuitry is provided to assist the data phase detector in phase locking to the sync field that precedes the data. For the case in which lock-up is attempted when the data edges are coincident with the VCO edges, the pump down signal may enter an indeterminate state for an unacceptably long period due to the violation of internal set up and hold times. After an initial pump down pulse, the circuit blocks successive pump down pulses, and inserts extra pump up pulses, during portions of the sync field that are known to contain zeros. Thus, the data phase detector is forced to have a nonzero output during the lock-up period, and the restoring force ensures correction of the loop within an acceptable time. Hence, this circuitry provides a quasi-deterministic pump down output signal, under the condition of coincident data and VCO edges, allowing lock-up to occur with excessive delays.

The $\overline{ACQ}$ line is provided to disable (disable = HIGH) the acquisition circuit during the data portion of a sector block. Typically, this circuit is enabled at the beginning of the sync field by a one-shot timer to ensure a timely lock-up.

The TYPE line allows the choice between two sync field preamble types; transitions interspersed with two zeros between transitions. These types of sync fields are used with the 1:7 and 2:7 coding schemes, respectively.

Idle Mode

In the absence of data or when the drive is writing to the disk, PLL servoing is accomplished by pulling the read enable line (RDEN) low and providing a reference clock via the REFCLK pins. The condition whereby RDEN is low selects the Phase/Frequency detector (Figure 1) and the 10E197 is said to be operating in the "idle mode". In order to function as a frequency detector the input waveform must be periodic. The pump up and pump down pulses from the Phase/Frequency detector will have the same frequency, phase and pulse width only when the two clocks that are being compared have their positive edges aligned and are of the same frequency.

As with the data phase detector, by using suitable external filter circuitry, a VCO input control signal can be generated by inverting the pump down signal, summing the inverted signal with the pump up signal and averaging the result. The polarity of this control signal is defined as zero when all positive edges of both clocks are coincident. For the case in which the frequencies of the two clocks are the same but the clock edges of the reference clock are slightly advanced with respect to the VCO clock, the control clock is defined to have a positive polarity. A control signal with negative polarity occurs when the edges of the reference clock are delayed with respect to those of the VCO. If the frequencies of the two clocks are different, the clock with the most edges per unit time will initiate the most pulses and the polarity of the detector will reflect the frequency error. Thus, when the reference clock is high in frequency than the VCO clock the polarity of the control signal is positive; whereas a control signal with negative polarity occurs when the frequency of the reference clock is lower than the VCO clock.

Phase-Lock Loop Theory

Introduction

Phase lock loop (PLL) circuits are fundamentally feedback systems used to synchronize the frequency of an oscillator to an incoming signal. In addition to frequency synchronization, the PLL circuitry is designed to minimize the phase difference between the system input and output signals. A block diagram of a feedback control system is shown in Figure 1.

where:

A(s) is the product of the feed-forward transfer functions.

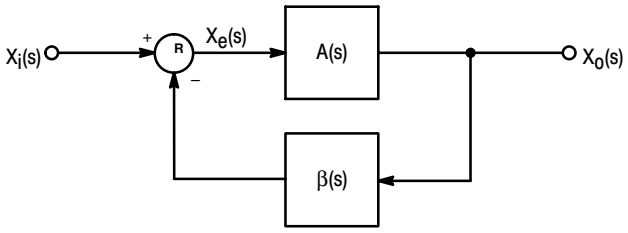


Figure 1. Feedback System

β(s) is the product of the feedback transfer functions.

The transfer function for this closed loop system is

$$\frac{X_O(s)}{X_i(s)} = \frac{A(s)}{1 + A(s)\beta(s)}$$

Typically, phase lock loops are modeled as feedback systems connected in a unity feedback configuration (β(s)=1) with a phase detector, a VCO (voltage controlled oscillator), and a loop filter in the feed-forward path, A(s). Figure 2 illustrates a phase lock loop as a feedback control system in block diagram form.

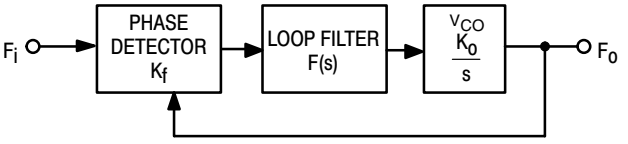


Figure 2. Phase Lock Loop Block Diagram

The closed loop transfer function is:

$$\frac{X_O(s)}{X_i(s)} = \frac{K_\phi \frac{K_O}{s} F(s)}{1 + K_\phi \frac{K_O}{s} F(s)}$$

where:

K_ϕ= the phase detector gain.
K_O= the VCO gain. Since the VCO introduces a pole at the origin of the s-plane, K_O is divided by s.
F(s) = the transfer function of the loop filter.

The 10E197 is designed to implement the phase detector and VCO functions in a unity feedback loop, while allowing the user to select the desired filter function.

Gain Constants

As mentioned, each of the three sections in the phase lock loop block diagram has an associated open loop gain constant. Further, the gain constant of the filter circuitry is composed of the product of three gain constants, one for each filter subsection. The open loop gain constant of the feed-forward path is given by

$$K_{ol} = K_\phi * K_o * K_1 * K_l * K_d \qquad \text{eqt. 1}$$

and obtained by performing a root locus analysis.

Phase Detector Gain Constant

The gain of the phase detector is a function of the operating mode and the data pattern. The 10E197 provides data separation for signals encoded in 2:7 or 1:7 RLL encoding schemes; hence, Tables 1 and 2 are coding tables for these schemes. Table 3 lists nominal phase detector gains for both 2:7 and 1:7 sync fields.

NRZ Data Sequence	Code Sequence
00 01	1000 0100
100 101 111	001000 100100 000100
1100 1101	00001000 00100100

Table 1. 2:7 RLL Encoding Table

NRZ Data Sequence	Code Sequence
00 01 10	X01 010 X00
1100 1101 1110 1111	010001 X00000 X00001 010000

An X in the leading bit of a code sequence is assigned the complement of the bit

Table 2. 1:7 RLL Encoding Table

Sync Pattern	Read Mode	Idle Mode
2:7	121 mV/radian	484 mV/radian
1:7	161 mV/radian	483 mV/radian

Table 3. Phase Detector Gain Constants

VCO Gain Constant

The gain of the VCO is a function of the tuning capacitor. For a value of 10pF a nominal value of the gain, K_O, is 20MHz per volt.

Filter Circuitry Gain Constant(s)

The open loop gain constant of the filter circuitry is given by:

$$K_{fc} = K_1 * K_I * K_d \qquad \text{eqt. 2}$$

The individual gain constants are defined in the appropriate subsections of this document.

Loop Filter

The two major functions of the loop filter are to remove any noise or high frequency components present in the phase detector output signal and, more importantly, to control the characteristics which determine the dynamic response of the phase lock loop; i.e. capture range, loop bandwidth, capture time, and transient response.

Although a variety of loop filter configurations exist, this section will only describe a filter capable of performing the signal processing as described in the Data Read Mode and the Idle Mode sections. The loop filter consists of a differential summing amplifier cascaded with an augmenting integrator which drives the VCOIN input to the 10E197 through a resistor divider network (Figure 3).

The transfer function and the element values for the loop filter are derived by dividing the filter into three cascaded subsections: filter input, augmenting integrator, and the voltage divider network (Figure 4).

Loop Filter Transfer Function

The open loop transfer function of the phase lock loop is the product of each individual filter subsection, as well as the phase detector and VCO. Thus, the open loop filter transfer function is:

$$F_o(s) = K_\phi * \frac{K_o}{s} * F_1(s) * F_I(s) * F_d(s)$$

where:

$$F_1(s) = K_1 * \frac{1}{(s + p_1)} * \frac{1}{[s^2 + (2\zeta\omega_{o1})\, s + \omega_{01}^2]}$$

$$F_I(s) = K_I * \frac{1}{s} * \frac{(s + z)}{[s^2 + (2\zeta\omega_{o2})\, s + \omega_{02}^2]}$$

$$F_d(s) = K_d * \frac{1}{(s + p_2)}$$

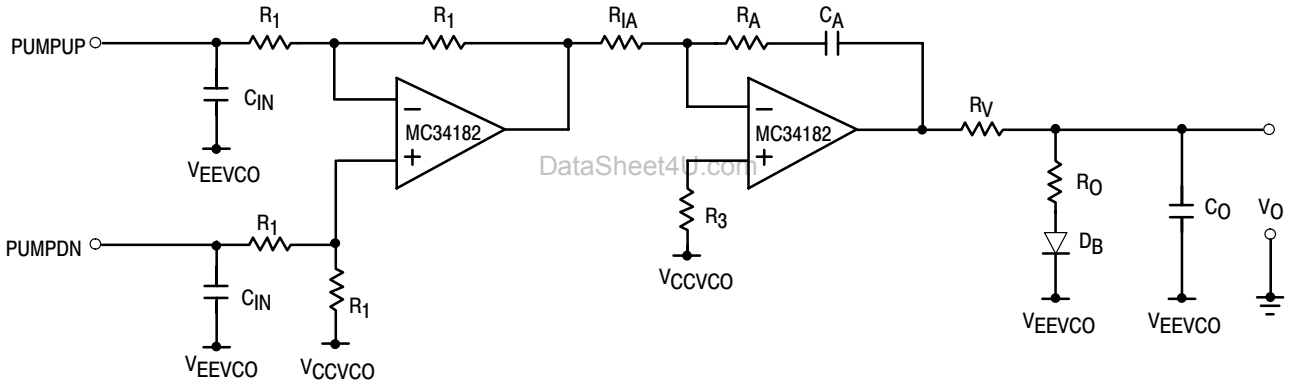


Figure 3. Loop Filter Circuitry

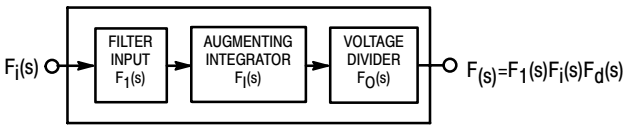


Figure 4. Loop Filter Block Diagram

A root locus analysis is performed on the open loop transfer function to determine the final pole-zero locations and the open loop gain constant for the phase lock loop. Note that the open loop gain constant impacts the crossover frequency and that a lower frequency crossover point means a much more efficient filter. Once these positions and constants are determined the component values may be calculated.

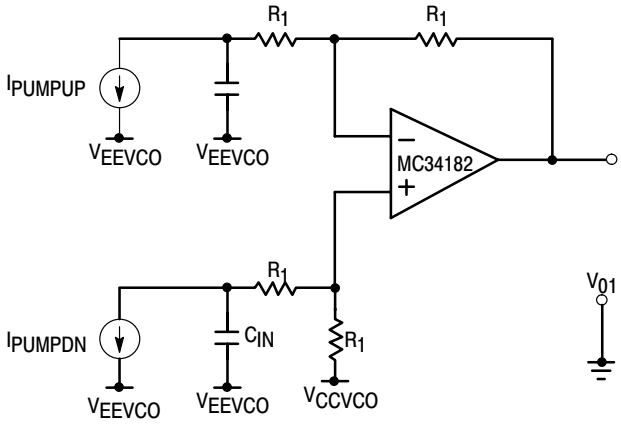


Figure 5. Filter Input Subsection

Filter Input

The primary function of the filter input subsection is to convert the output of the phase detector into a single ended signal for subsequent processing by the integrator circuitry. This subsection consists of the 10E197 charge pump current sinks, two shunt capacitors, and a differential summing amplifier (Figure 5).

Hence, this portion of the filter circuit contributes a real pole and two complex poles to the overall loop transfer function F(s). Before these pole locations are selected, appropriate values for the current setting resistors (RSETUP and RSETDN) must be ascertained. The goal in choosing these resistor values is to maximize the gain of the filter input subsection while ensuring the charge pump output transistors operate in the active mode. The filter input gain is maximized for a charge pump current of 1.1mA; a value of 464Ω for both RSETUP and RSETDN yields a nominal charge pump current of 1.1mA.

It should be noted that a dual bandwidth implementation of the phase lock loop may be achieved by modifying the current setting resistors such that an electronic switch enables one of two resistor configurations. Figure 6 shows a circuit configuration capable of providing this dual bandwidth function. Analysis of the filter input circuitry yields the transfer function:

$$F_1(s) = K_1 * \frac{1}{(s + p_1)} * \frac{1}{[s^2 + (2\zeta\omega_{o1})\, s + \omega_{o1}^2]}$$

The gain constant is defined as:

$$K_1 = A_1 * \frac{1}{C_{IN}} \qquad \text{eqt. 3}$$

where:

A_1 = op-amp gain constant for the selected pole positions.

C_{IN} = phase detector shunt capacitor.

The real pole is a function of the input resistance to the op-amp and the shunt capacitors connected to the phase detector output. For stability the real pole must be placed beyond the unity gain frequency; hence, this pole is typically placed midway between the unity crossover and phase detector sampling frequency, which should be about ten times greater.

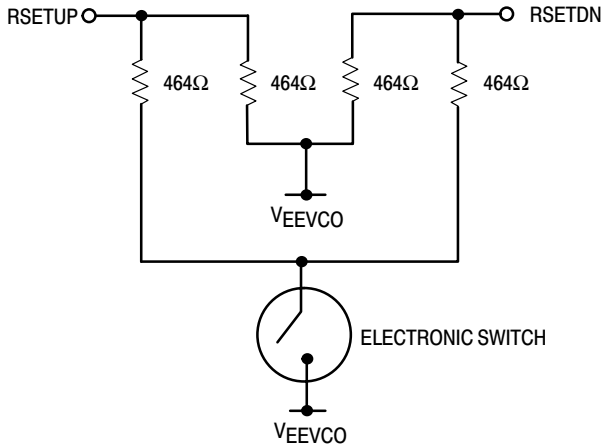


Figure 6. Dual Bandwidth Current Source Implementation

The second order pole set arises from the two pole model for an op-amp. The open loop gain and the first open loop pole for the op-amp are obtained from the data sheets. Typically, op-amp manufacturers do not provide information on the location of the second open loop pole; however, it can be approximated by measuring the roll off of the op-amp in the open loop configuration. The second pole is located where the gain begins to decrease at a rate of 40dB per decade. The inclusion of both poles in the differential summing amplifier transfer function becomes important when closing the feedback path around the op-amp because the poles migrate; and this migration must be accounted for to accurately determine the phase lock loop transient performance.

Typically the op-amp poles can be approximated by a pole pair occurring as a complex conjugate pair making an angle of 45° to the real axis of the complex frequency plane. Two constraints on the selection of the op-amp pole pair are that the poles lie beyond the crossover frequency and they are positioned for near unity gain operation. Performing a root locus analysis on the op-amp open loop configuration and adhering to the two constraints yields the pole positions contributed by the op-amp.

Determination of Element Values

Since the difference amplifier is configured to operate as a differential summer the resistor values associated with the amplifier are of equal value. Further, the typical input resistance to the summing amplifier is 1kΩ; thus, the op-amp resistors are set at 1 kΩ. Having set the input resistance to the op-amp and selected the position of the real pole, the value of the shunt capacitors is determined using the following relationship:

$$|p_1| = \frac{1}{2\pi R_1 C_{IN}} \qquad \text{eqt. 4}$$

Augmenting Integrator

The augmenting integrator consists of an active filter with a lag-lead network in the feedback path (Figure 7).

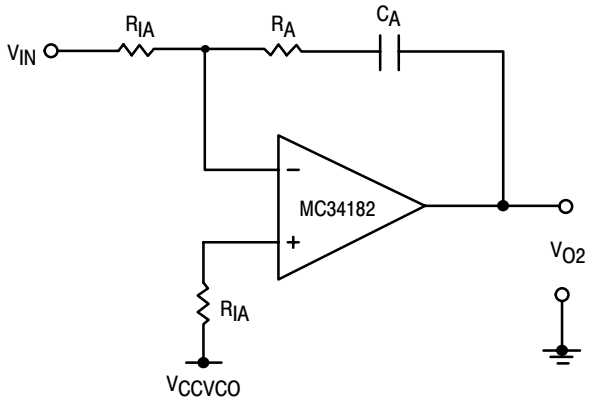


Figure 7. Integrator Subsection

Analysis of this portion of the filter circuit yields the transfer function:

$$F_1(s) = K_I * \frac{1}{s} * \frac{(s + z)}{[s^2 + (2\zeta\omega_{o2})s + \omega^2_{o2}]}$$

The gain constant is defined as:

$$K_I = A_I * \frac{R_A}{R_{IA}} \qquad \text{eqt. 5}$$

where:

A_I = op-amp gain constant for selected pole positions.

R_A = integrator feedback resistor.

R_{IA} = integrator input resistor.

The integrator circuit introduces a zero, a pole at the origin, and a second order pole set as described by the two pole model for an op-amp. As in the case of the differential summing amplifier, we assume the op-amp pole pair occur as a complex conjugate pair making an angle of 45° to the real axis of the complex frequency plane; are positioned for near unity gain operation; and are located beyond the crossover frequency. Since both the summing and integrating op-amps are realized by the same type of op-amp (MC34182D), the open loop pole positions for both amplifiers will be the same.

Further, the loop transfer function contains two poles located at the origin, one introduced by the integrator and the other by the VCO; hence a zero is necessary to compensate for the phase shift produced by these poles and ensure loop stability. The op-amp will be stable if the crossover point occurs before the transfer function phase angle becomes 180°. The zero should be positioned much less than one decade before the unity gain frequency.

As in the case of the filter input circuitry, the poles and zero from this analysis will be used as open loop poles and a zero when performing the root locus analysis for the complete system.

Determination of Element Values

The location of the zero is used to determine the element values for the augmenting integrator. The value of the capacitor, C_A, is selected to provide adequate charge storage when the loop is not sampling data. A value of 0.1μF is sufficient for most applications; this value may be increased when the RDCLK frequency is much lower than 4 MHz. The value of R_A is governed by:

$$|z| = \frac{1}{2\pi R_A C_A} \qquad \text{eqt. 6}$$

For unity gain operation of the integrating op-amp the value of RlA is selected such that:

$$R_{IA} = R_A \qquad \text{eqt. 7}$$

It should be noted that although the zero can be tuned by varying either R_A or C_A, caution must be exercised when adjusting the zero by varying C_A because the integrator gain is also a function of C_A. Further, the gain of the loop filter can be adjusted by changing the integrator input resistor R_{IA}.

Voltage Divider

The input range to the VCOIN input is from 1.3V + V_{EE} to 2.6V + V_{EE}; hence, the output from the augmenting amplifier section must be attenuated to meet the VCOIN constraints. A simple voltage divider network provides the necessary attenuation (Figure 8).

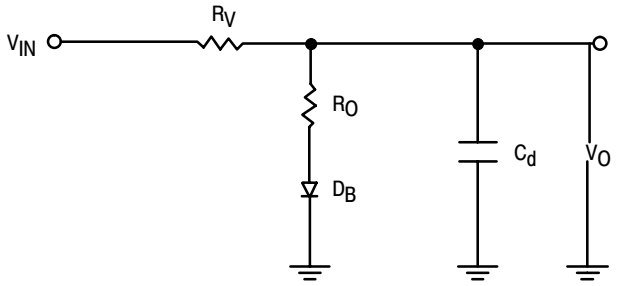


Figure 8. Voltage Divider Subsection

In addition, a shunt filter capacitor connected between the VCOIN input pin and V_{EE} provides the voltage divider subsection with a single time constant transfer function that adds a pole to the overall loop filter. The transfer function for the voltage divider network is:

$$F_d(s) = K_d * \frac{1}{(s + p_2)}$$

The gain constant, K_d, is defined as:

$$K_d = \frac{1}{R_v C_d} \qquad \text{eqt. 9}$$

he value of K_d is easily extracted by rearranging Equation 1:

$$K_d = \frac{K_{ol}}{K_\phi * K_o * K_1 * K_I} \qquad \text{eqt. 10}$$

The gain constant K_d is set such that the output from the integrator circuit is within the range 1.3V +V_{EE} to 2.6V +V_{EE}. The pole for the voltage divider network should be positioned an octave beyond that for the filter input.

Determination of Element Values

Once the pole location and the gain constant K_d are established the resistor values for the voltage divider network are determined using the design guidelines mentioned above and from the following relationship:

$$\frac{K_d}{2\pi|p_2|} = \frac{R_o}{R_o + R_v}$$

Having determined the resistor values, the filter capacitor is calculated by rearranging Equation 9:

$$C_d = \frac{1}{R_v K_d} \qquad \text{eqt. 9a}$$

Finally, a bias diode is included in the voltage divider network to provide temperature compensation. The finite resistance of this diode is neglected for these calculations.

Calculations For a 2:7 Coding Scheme

Introduction

The circuit component values are calculated for a 2:7 coding scheme employing a data rate of 23Mbit/sec. Since the number of bits is doubled when the data is encoded, the data clock is at half the frequency of the RDCLK signal. Thus, the operating frequency for these calculations is 46MHz. Further, the pole and zero positions are a function of the data rate; hence, the component values derived by these calculations must be scaled if a different operating frequency is used. Finally, it should be noted that the values are optimized for settling time.

The analysis is divided into three parts: static pole positioning, dynamic pole positioning, and dynamic zero positioning. Dynamic poles and zeros are those which the designer may position, to yield the desired dynamic response, through the judicious choice of element values. Static poles are not directly controlled by the choice of component values.

Static Poles

Each op-amp introduces a pair of "static" complex conjugate poles which must lie beyond the crossover frequency. As obtained from the data sheets and laboratory measurements, the two open loop poles for the MC34182D are:

$$P^*_{1a} = -0.1\text{Hz}$$

$$P^*_{1b} = -11.2\text{Hz}$$

Performing a root locus analysis and following the two guidelines previously stated, an acceptable pole set is:

$$P_{1a} = -5.65 + j5.65\text{MHz}$$

$$P_{1b} = -5.65 - j5.65\text{MHz}$$

Both op-amps introduce a set of static complex conjugate poles at these positions for a total of four poles. Further, the loop gain for each op-amp associated with these pole positions is determined from the root locus analysis to be:

$$A_1 = A_2 = 2.48\ e15\ \frac{V}{V}$$

In addition to the op-amps, the integrator and the VCO each contribute a static pole at the origin. Thus, there are a total of six static poles.

Dynamic Poles

The filter input and the voltage divider sections each contribute a dynamic pole. As stated previously, the filter input pole should be positioned midway between the unity crossover point and the phase detector sampling frequency. Hence, the open loop filter input pole position is selected as:

$$P^*_1 = -1.24\text{MHz}$$

The voltage divider pole is set approximately one octave higher than the filter input pole. Thus the open loop voltage divider pole position is picked to be:

$$P^*_2 = -2.57\text{MHz}$$

Dynamic Zero

Finally, the zero is positioned much less than one decade before the crossover frequency; for this design the zero is placed at:

$$z = -311\text{Hz}$$

Once the dynamic pole and zero positions have been determined, the phase margin is determined using a Bode plot; if the phase margin is not sufficient, the dynamic poles may be moved to improve the phase margin. Finally, a root locus analysis is performed to obtain the optimum closed loop pole positions for the dynamic characteristics of interest.

Component Values

Having determined the closed loop pole and zero positions the component values are calculated. From the root locus analysis the dynamic pole and zero positions are:

$$P_1 = -573\text{kHz}$$

$$P_2 = -3.06\text{MHz}$$

$$z = -311\text{Hz}$$

Filter Input Subsection

Rearranging Equation 4:

$$C_{IN} = \frac{1}{2\pi R_1 |p_1|}$$

and substituting 573 kHz for the pole position and 1 kΩ for the resistor value yields:

$$C_{IN} = 278\ \text{pF}$$

Augmenting Integrator Subsection

Rearranging Equation 6:

$$R_A = \frac{1}{2\pi |z| C_A}$$

and substituting 311Hz for the zero position and 0.1μF for the capacitor value yields:

$$R_A = 5.11\text{k}\Omega$$

From Equation 7 the value for the other resistors associated with the integrator op-amp are set equal to R_A:

$$R_{IA} = R_A = 5.11\text{k}\Omega$$

Voltage Divider Subsection

The element values for the voltage divider network are calculated using the relationships presented in Equations 8, 9, and 10 with the constraint that this divider network must produce a voltage that lies within the range 1.3V + V_{EE} to 2.6V + V_{EE}.
Restating Equation 9,

$$K_d = \frac{K_{ol}}{K_\phi * K_o * K_1 * K_l}$$

From the root locus analysis K_{ol} is determined to be:

$$K_{ol} = 1.585\ e51 \frac{V}{mA\ sec^3}$$

From Equation 3

$$K_1 = A_1 * \frac{1}{C_{IN}}$$

and the gain constant K_1 is:

$$K_1 = 8.90\ e21 \frac{V}{mA\ sec}$$

From Equation 5

$$K_l = A_l * \frac{R_A}{R_{lA}}$$

and the gain constant K_l is:

$$K_l = 2.48\ e15 \frac{V}{V}$$

Having determined the gain constant K_d , the value of R_v, is selected such that the constraints $R_v > R_o$ and:

$$\frac{K_d}{2\pi |p_2|} = \frac{R_o}{R_o + R_v}$$

are fulfilled. The pole position P_2 is determined from the root locus analysis to be:

$$P_2 = -3.06MHz$$

Hence, R_v is selected to be:

$$R_v = 2.15k\Omega$$

and R_o is calculated to be:

$$R_o = 700\Omega$$

Finally, using Equation 8a:

$$C_d = \frac{1}{R_v K_d} \qquad \text{eqt. 8a}$$

the capacitor value, C_d is:

$$C_d = 98pF$$

Note that the voltage divider section can be used to set the gain, but the designer is cautioned to be sure the input value to VCOIN is within the correct range.

Component Scaling

As mentioned, these design equations were developed for a data rate of 23 Mbit/sec. If the data rate is different from the nominal design value the reactive elements must be scaled accordingly. The following equations are provided to facilitate scaling and were derived with the assumptions that a 2:7 coding scheme is used and that the RDCLK signal is twice the frequency of the data clock.

$$C_{IN} = 278 * \frac{46}{f} \quad (pF) \qquad \text{eqt. 11}$$

$$C_d = 98 * \frac{46}{f} \quad (pF) \qquad \text{eqt. 12}$$

where f is the RDCLK frequency in MHz.

Example for an 11 Mbit/sec Data Rate

As an example of scaling, assume the given filter and a 2:7 code are used but the data rate is 11Mbit/sec. The dynamic pole positions, and therefore the bandwidth of the loop filter, are a function of the data rate. Thus a slower data rate will force the dynamic poles and the bandwidth to move to a lower frequency. From Equation 11 the value of C_{IN} is:

$$C_{IN} = 581pF$$

and from Equation 12 the value of C_d is:

$$C_d = 205pF$$

Thus the element values for the filter are:
Filter Input Subsection:

$$C_{IN} = 581pF$$

$$R_1 = 1k\Omega$$

Integrator Subsection:

$$C_A = 0.1\mu F$$

$$R_A = 5.11k\Omega$$

$$R_{lA} = 5.11k\Omega$$

Voltage Divider Subsection:

$$C_d = 205pF$$

$$R_v = 2.15k\Omega$$

$$R_o = 700k\Omega$$

Note, the poles P_1 and P_2 are now located at:

$$P_1 = -274kHz$$

$$P_2 = -1.47MHz$$

And, the open loop filter unity crossover point is at 300kHz. The gain can be adjusted by changing the value of R_{IA} and the value of C_d. Varying the gain by changing C_d is not recommended because this will also move the poles, hence affect the dynamic 2 performance of the filter.

Calculations For a 1:7 Coding Scheme

Introduction

The circuit component values are calculated for a 1:7 coding scheme employing a data rate of 20Mbit/sec. Since the number of bits increases from two to three when the data is encoded, the data clock is at two-thirds the frequency of the RDCLK signal. Thus, the operating frequency for these calculations is 30MHz. As in the case of the 2:7 coding scheme the pole and zero positions are a function of the data rate, hence the component values derived by these calculations must be scaled if a different operating frequency is used.

Again, the analysis is divided into three parts: static pole positioning, dynamic pole positioning, and dynamic zero positioning.

Static Poles

As in the 2:7 coding example, an MC34182D op-amp is employed, hence the pole set is:

$$P_{1a} = -5.65 + j5.65MHz$$

$$P_{1b} = -5.65 - j5.65MHz$$

and the open loop gain is:

$$A_I = A_2 = 2.48\ e15\ \frac{V}{V}$$

Since the op-amps introduce a set of complex conjugate poles, a total of four poles are introduced by the op-amp. In addition, the integrator and the VCO each contribute a pole at the origin for a total of six static poles.

Dynamic Poles

The filter input and the voltage divider sections each contribute a dynamic pole. As stated previously, the filter input pole should be positioned midway between the unity crossover point and the phase detector sampling frequency. Hence, the open loop filter input pole position is selected as:

$$P^*_1 = -1.1MHz$$

The voltage divider pole is set approximately one octave higher than the filter input pole. Thus, the open loop voltage divider pole position is selected as:

$$P^*_2 = -2.28MHz$$

Dynamic Zero

Finally, the zero is positioned much less than one decade before the crossover frequency; for this design the zero is placed at:

$$z = -311Hz$$

Once the dynamic pole and zero positions have been determined, the phase margin is determined using a Bode plot; if the phase margin is not sufficient, the dynamic poles may be moved to improve the phase margin. Finally, a root locus analysis is performed to obtain the optimum closed loop pole positions for the dynamic characteristics of interest.

Component Values

Having determined the closed loop pole and zero positions the component values are calculated. From the root locus analysis the dynamic pole and zero positions are:

$$P_1 = -541kHz$$

$$P_2 = -2.73MHz$$

$$z = -311Hz$$

Filter Input Subsection

Rearranging Equation 4

$$C_{IN} = \frac{1}{2\pi R_1 |p_1|}$$

and substituting 541kHz for the pole position and 1.0kΩ for the resistor value yields:

$$C_{IN} = 294\ pF$$

Augmenting Integrator Subsection

Rearranging Equation 6

$$R_A = \frac{1}{2\pi\ |z| C_A}$$

and substituting 311Hz for the zero position and 0.1μF for the capacitor value yields:

$$R_A = 5.11k\Omega$$

From Equation 7 the value for the other resistors associated with the integrator op-amp are set equal to R_A:

$$R_{IA} = R_A = 5.11k\Omega$$

Voltage Divider Subsection

The element values for the voltage divider network are calculated using the relationships presented in Equations 8, 9, and 10 with the constraint that this divider network must produce a voltage that lies within the range 1.3V + V_{EE} to 2.6V + V_{EE}.

Restating Equation 9,

$$K_d = \frac{K_{ol}}{K_\phi * K_o * K_1 * K_l}$$

From the root locus analysis K_{ol} is determined to be:

$$K_{ol} = 1.258\ e51 \frac{V}{MA\ SEC^3}$$

From Equation 3:

$$K_1 = A_1 * \frac{1}{C_{IN}}$$

and the gain constant K_1:

$$K_1 = 8.42\ e21 \frac{V}{mA\ sec}$$

From Equation 5:

$$K_l = A_l * \frac{R_A}{R_{lA}}$$

and the gain constant K_l is:

$$K_l = 2.48\ e15 \frac{V}{V}$$

$$K_d = 2.98\ e6\ sec^{-1}$$

Having determined the gain constant K_d , the value of R_v, is selected such that the constraints $R_v > R_o$ and:

$$\frac{K_d}{2\pi |p_2|} = \frac{R_o}{R_o + R_v}$$

are fulfilled. The pole position P_2 is determined from the root locus analysis to be:

$$P_2 = -2.73MHz$$

Hence, R_v is selected to be:

$$R_v = 2.15k\Omega$$

and R_o is calculated to be:

$$R_o = 453\Omega$$

Finally, using Equation 8a:

$$C_d = \frac{1}{R_v K_d} \qquad \text{eqt. 8a}$$

the capacitor value, C_d is calculated to be:

$$C_d = 156pF$$

Again, note the voltage divider section can be used to set the gain, but the designer is cautioned to be sure the input value to VCOIN is within the correct range.

Component Scaling

As mentioned, these design equations were developed for a data rate of 20Mbit/sec. If the data rate is different from the nominal design value the reactive elements must be scaled accordingly. The following equations provided are to facilitate scaling and were derived with the assumptions that a 1:7 coding scheme is used and that the RDCLK signal is twice the frequency of the data clock:

$$C_{IN} = 294 * \frac{30}{f} \quad (pF) \qquad \text{eqt. 13}$$

$$C_d = 156 * \frac{30}{f} \quad (pF) \qquad \text{eqt. 14}$$

where f is the RDCLK frequency in MHz.

Example for an 10 Mbit/sec Data Rate

As an example of scaling, assume the given filter and a 1:7 code are used but the data rate is 10Mbit/sec. The dynamic pole positions and, therefore, the bandwidth of the loop filter, are a function of the data rate. Thus, a slower data rate will force the dynamic poles and the bandwidth to move to a lower frequency. From Equation 13 the value of C_{IN} is:

$$C_{IN} = 588pF$$

and from Equation 14 the value of C_d is:

$$C_d = 312pF$$

Thus, the element values for the filter are:
Filter Input Subsection:

$$C_{IN} = 588pF$$

$$R_1 = 1.0k\Omega$$

Integrator Subsection:

$$C_A = 0.1\mu F$$

$$R_A = 5.11k\Omega$$

$$R_{lA} = 5.11k\Omega$$

Voltage Divider Subsection:

$$C_d = 312pF$$

$$R_v = 2.15k\Omega$$

$$R_o = 453k\Omega$$

Note, the poles P_1 and P_2 are now located at:

$$P_1 = -271kHz$$

$$P_2 = -1.36MHz$$

And, the open loop filter unity crossover point is at 300kHz. As in the case of the 2:7 coding scheme, the gain can be adjusted by changing the value of R_{lA} and the value of C_d. Varying the gain by changing C_d is not recommended because this will also move the poles, hence affect the dynamic performance of the filter.

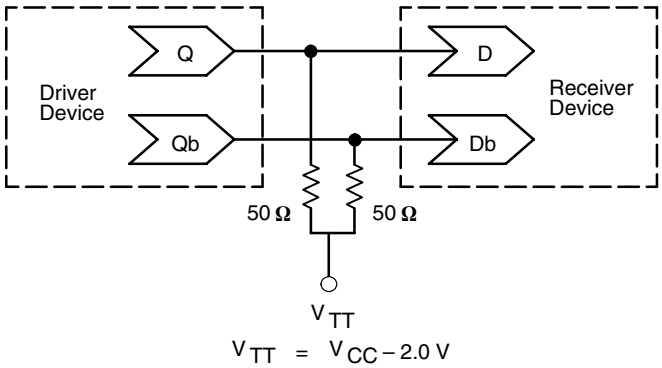


Figure 9. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC100E210

5V ECL Dual 1:4, 1:5 Differential Fanout Buffer

The MC100E210 is a low voltage, low skew dual differential ECL fanout buffer designed with clock distribution in mind. The device features two fanout buffers, a 1:4 and a 1:5 buffer, on a single chip. The device features fully differential clock paths to minimize both device and system skew. The dual buffer allows for the fanout of two signals through a single chip, thus reducing the skew between the two fundamental signals from a part–to–part skew down to an output–to–output skew. This capability reduces the skew by a factor of 4 as compared to using two LVE111's to accomplish the same task.

The lowest tpd delay time results from terminating only one output pair, and the greatest tpd delay time results from terminating all the output pairs. This shift is about 10–20 pS in tpd. The skew between any two output pairs within a device is typically about 25 nS. If other output pairs are not terminated, the lowest tpd delay time results from both output pairs and the skew is typically 25 nS. When all outputs are terminated, the greatest tpd (delay time) occurs and all outputs display about the same 10–20 pS increase in tpd, so the relative skew between any two output pairs remains about 25 nS.

For more information on using PECL, designers should refer to Application Note AN1406/D.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- Dual Differential Fanout Buffers
- 200 ps Part–to–Part Skew
- 50 ps Typical Output–to–Output Skew
- Low Voltage ECL/PECL Compatible
- The 100 Series Contains Temperature Compensation
- 28–lead PLCC Packaging
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at V_{EE}
- ESD Protection: >2KV HBM, >200V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8",
  Oxygen Index 28 to 34
- Transistor Count = 179 devices

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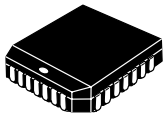
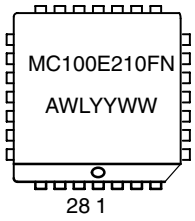


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAM



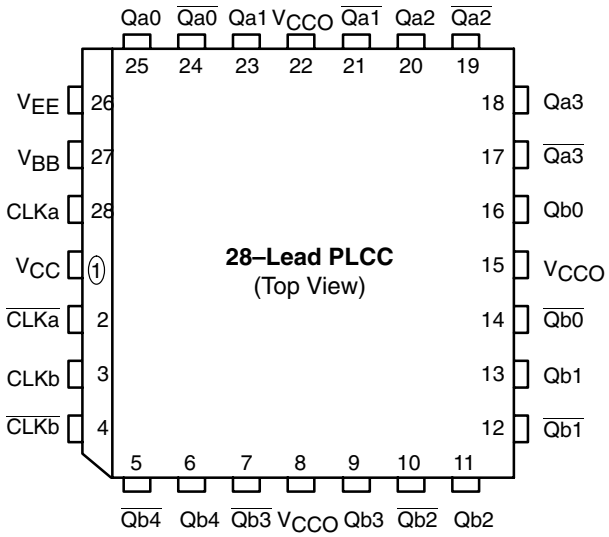
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

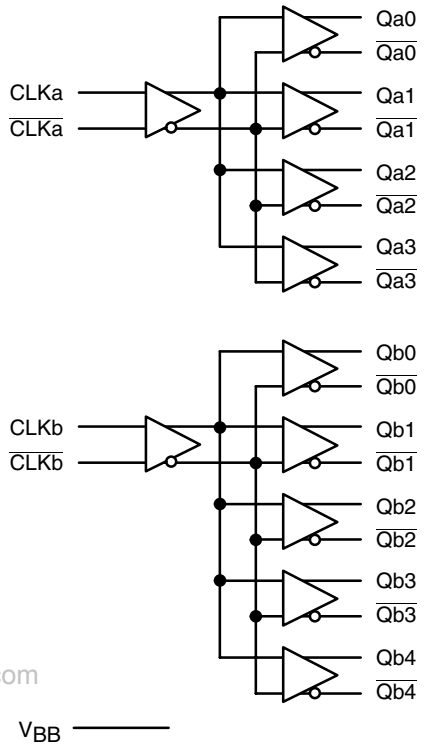
Device	Package	Shipping
MC100E210FN	PLCC–28	37 Units / Rail
MC100E210FNR2	PLCC–28	500 Tape & Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC SYMBOL



PIN DESCRIPTION

PIN	FUNCTION
CLKa, CLKb	ECL Differential Input Pairs
$\overline{CLKa}$, $\overline{CLKb}$	ECL Differential Input Pairs
Qa0:3, Qb0:4	ECL Differential Outputs
$\overline{Qa0:3}$, $\overline{Qb0:4}$	ECL Differential Outputs
V_{BB}	Reference Output Voltage
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur. V

PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current			55			55			65	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.7		4.6	2.7		4.6	2.7		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current			55			55			65	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.3		–0.4	–2.3		–0.4	–2.3		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

ECL DC CHARACTERISTICS

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage	–1.085	–1.005	–0.880	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	V
V_{OL}	Output LOW Voltage	–1.830	–1.695	–1.555	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	V
V_{IH}	Input HIGH Voltage	–1.165		–0.880	–1.165		–0.880	–1.165		–0.880	V
V_{IL}	Input LOW Voltage	–1.810		–1.475	–1.810		–1.475	–1.810		–1.475	V
V_{BB}	Output Reference Voltage	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{EE}	Power Supply Voltage	–5.25		–4.2	–5.25		–4.2	–5.25		–4.2	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{EE}	Power Supply Current			55			55			65	mA

PECL DC CHARACTERISTICS

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage (Note 1.)	3.915	3.995	4.12	3.975	4.045	4.12	3.975	4.045	4.12	V
V_{OL}	Output LOW Voltage (Note 1.)	3.170	3.305	3.445	3.19	3.295	3.38	3.19	3.295	3.38	V
V_{IH}	Input HIGH Voltage (Note 1.)	3.835		4.12	3.835		4.12	3.835		4.12	V
V_{IL}	Input LOW Voltage (Note 1.)	3.190		3.525	3.190		3.525	3.190		3.525	V
V_{BB}	Output Reference Voltage (Note 1.)	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{CC}	Power Supply Voltage	4.75		5.25	4.75		5.25	4.75		5.25	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{EE}	Power Supply Current			55			55			65	mA

1. These values are for V_{CC} = 5.0 V. Level Specifications will vary 1:1 with V_{CC}.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output IN (differential) (Note 2.) IN (single–ended) (Note 3.)	 475 400		 675 700	 500 450		 700 750	 500 450		 700 750	ps
t_{skew}	Within–Device Skew Qa to Qb Qa to Qa,Qb to Qb Part–to–Part Skew (Differential) (Note 4.)		50 50	75 75 200		50 30	75 50 200		50 30	75 50 200	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Minimum Input Swing (Note 5.)	500			500			500			mV
t_r/t_f	Output Rise/Fall Time (20%–80%)	200		600	200		600	200		600	ps

1. V_{EE} can vary +0.46 V / –0.8 V.
2. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
3. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
4. The within–device skew is defined as the worst case difference between any two similar delay paths within a single device.
5. V_{PP}(min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP}(min) is AC limited for the E210 as a differential input as low as 50 mV will still produce full ECL levels at the output.

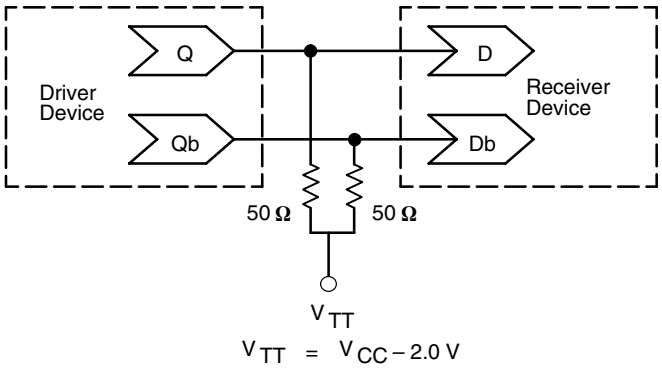


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

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AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E211, MC100E211

5V ECL 1:6 Differential Clock Distribution Chip

The MC10E/100E211 is a low skew 1:6 fanout device designed explicitly for low skew clock distribution applications.

The E211 features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open in which case it will be pulled LOW by the input pulldown resistor) the SEL pin will select the differential clock input.

Both a common enable and individual output enables are provided. When asserted the positive output will go LOW on the next negative transition of the CLK (or SCLK) input. The enabling function is synchronous so that the outputs will only be enabled/disabled when the outputs are already in the LOW state. In this way the problem of runt pulse generation during the disable operation is avoided. Note that the internal flip flop is clocked on the falling edge of the input clock edge, therefore all associated specifications are referenced to the negative edge of the CLK input.

The output transitions of the E211 are faster than the standard ECLinPS edge rates. This feature provides a means of distributing higher frequency signals than capable with the E111 device. Because of these edge rates and the tight skew limits guaranteed in the specification, there are certain termination guidelines which must be followed. For more details on the recommended termination schemes please refer to the applications information section of this data sheet.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

- Guaranteed Low Skew Specification
- Synchronous Enabling/Disabling
- Multiplexed Clock Inputs
- V_{BB} Output for Single-Ended Use
- Common and Individual Enable/Disable Control
- High Bandwidth Output Transistors
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 100 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 457 devices

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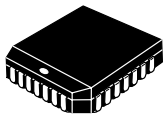


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAMS

28 1

28 1

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E211FN	PLCC–28	37 Units/Rail
MC10E211FNR2	PLCC–28	500 Units/Reel
MC100E211FN	PLCC–28	37 Units/Rail
MC100E211FNR2	PLCC–28	500 Units/Reel

FUNCTION TABLE

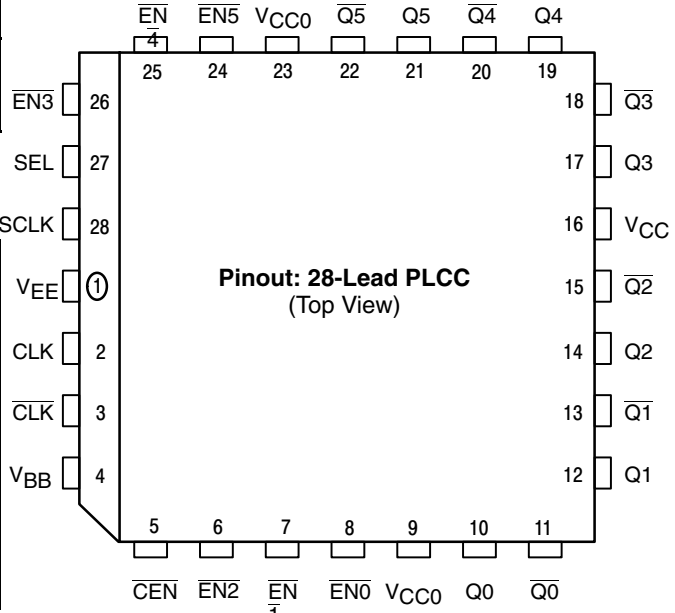
CLK	SCLK	SEL	$\overline{ENx}$	Q
H/L	X	L	L	CLK
X	H/L	H	L	SCLK
Z*	Z*	X	H	L

* Z = Negative transition of CLK or SCLK

PIN DESCRIPTION

PIN	FUNCTION
$\overline{EN0}$–$\overline{EN5}$	ECL Enable
SEL	ECL Select (Clock)
SCLK	ECL Single Clock
CLK, $\overline{CLK}$	ECL Differential Clock
$\overline{CEN}$	ECL Common Enable
Q0–Q5, $\overline{Q0}$–$\overline{Q5}$	ECL Differential Outputs
V_{BB}	Reference Voltage Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

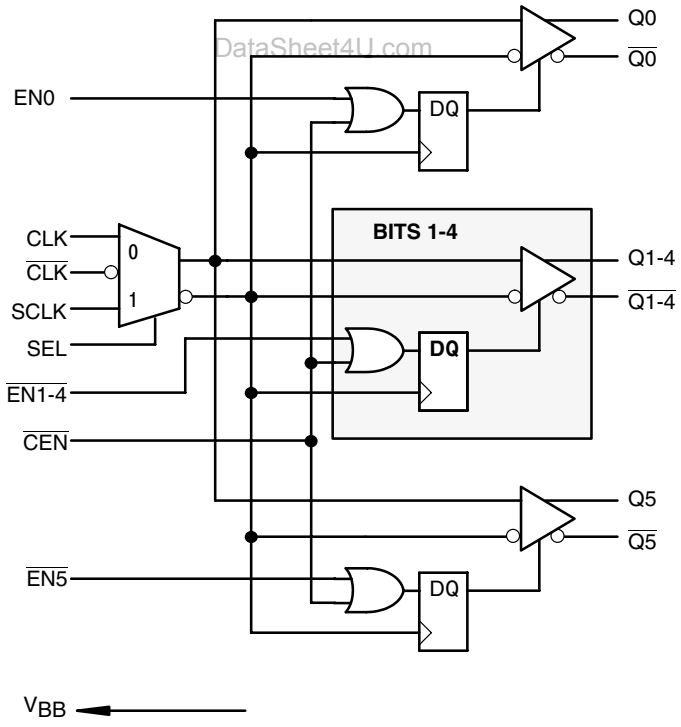
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Logic Diagram



MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		119	160		119	160		119	160	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage (Single Ended)	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
V_{BB}	Output Voltage Reference	3.62		3.63	3.65		3.75	3.69		3.81	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.4		4.6	2.4		4.6	2.4		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		119	160		119	160		119	160	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
V_{BB}	Output Voltage Reference	–1.38		–1.37	–1.35		–1.25	–1.31		–1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.6		–0.4	–2.6		–0.4	–2.6		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		119	160		119	160		137	164	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.4		4.6	2.4		4.6	2.4		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		119	160		119	160		137	164	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.6		–0.4	–2.6		–0.4	–2.6		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK to Q (Diff) CLK to Q (SE) SCLK to Q SEL to Q	 795 745 650 745	 930 930 900 970	 1065 1115 1085 1195	 805 755 650 755	 940 940 910 980	 1075 1125 1095 1205	 825 775 650 775	 960 960 930 1000	 1095 1145 1115 1225	ps
t_{PHL}	Disable Time CLK or SCLK to Q (Note 3.)		600	800		600	800		600	800	ps
t_{skew}	Part–to–Part Skew CLK (Diff) to Q CLK (SE), SCLK to Q Within-Device Skew (Note 2.)		 50	270 370 75		 50	270 370 75			270 370 75	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_s	Setup Time $\overline{EN}$x to CLK $\overline{CEN}$ to CLK (Note 3.)	 200 200	 –100 0		 200 200	 –100 0		 200 200	 –100 0		ps
t_h	Hold Time CLK to $\overline{EN}$x, $\overline{CEN}$ (Note 3.)	900	600		900	160		900	600		ps
V_{PP}	Minimum Input Swing (CLK) (Note 4.)	0.25		1.0	0.25		1.0	0.25		1.0	V
t_r t_f	Rise/Fall Times (20 – 80%)	 150		 400	 150		 400	 150		 400	ps

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Within-Device skew is defined for identical transitions on similar paths through a device.
3. Setup, Hold and Disable times are all relative to a falling edge on CLK or SCLK.
4. Minimum input swing for which AC parameters are guaranteed. Full DC ECL output swings will be generated with only 50mV input swings.

APPLICATIONS INFORMATION

General Description

The MC10E/100E211 is a 1:6 fanout tree designed explicitly for low skew high speed clock distribution. The device was targeted to work in conjunction with the E111 device to provide another level of flexibility in the design and implementation of clock distribution trees. The individual synchronous enable controls and multiplexed clock inputs make the device ideal as the first level distribution unit in a distribution tree. The device provides the ability to distribute a lower speed scan or test clock along with the high speed system clock to ease the design of system diagnostics and self test procedures. The individual enables could be used to allow for the disabling of individual cards on a backplane in fault tolerant designs.

Because of lower fanout and larger skews the E211 will not likely be used as an alternative to the E111 for the bulk of the clock fanout generation. Figure 1 shows a typical application combining the two devices to take advantage of the strengths of each.

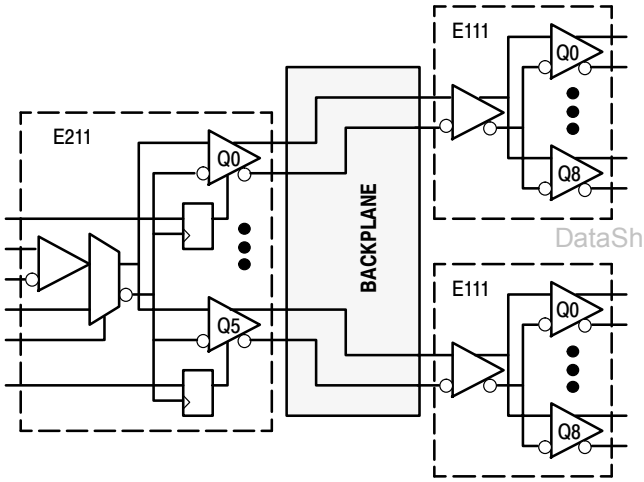


Figure 1. Standard E211 Application

Using the E211 in PECL Designs

The E211 device can be utilized very effectively in designs utilizing only a +5V power supply. Since the internal switching reference levels are biased off of the V_{CC} supply the input thresholds for the single-ended inputs will vary with V_{CC}. As a result the single-ended inputs should be driven by a device on the same board as the E211. Driving these inputs across a backplane where significant differences between the V_{CC}'s of the transmitter and receiver can occur can lead to AC performance and/or significant noise margin degradations. Because the differential I/O does not use a switching reference, and due to the CMR range of the E211, even under worst case V_{CC} situations between cards there will be no AC performance or noise margin loss for the differential CLK inputs.

For situations where TTL clocks are required the E211 can be interfaced with the H641 or H643 ECL to TTL Clock Distribution Chips. The H641 is a single supply 1:9 PECL to TTL device while the H643 is a 1:8 dual supply standard ECL to TTL device. By combining the superior skew performance of the E211, or E111, with the low skew translating capabilities of the H641 and H643 very low skew TTL clock distribution networks can be realized.

Handling Open Inputs and Outputs

All of the input pins of the E211 have a 50kΩ to 75kΩ pulldown resistor to pull the input to V_{EE} when left open. This feature can cause a problem if the differential clock inputs are left open as the input gate current source transistor will become saturated. Under these conditions the outputs of the CLK input buffer will go to an undefined state. It is recommended, if possible,that the SCLK input should be selected any time the differential CLK inputs are allowed to float. The SCLK buffer, under open input conditions, will maintain a defined output state and thus the Q outputs of the device will be in a defined state (Q = LOW). Note that if all of the inputs are left open the differential CLK input will be selected and the state of the Q outputs will be undefined.

With the simultaneous switching characteristics and the tight skew specifications of the E211 the handling of the unused outputs becomes critical. To minimize the noise generated on the die all outputs should be terminated in pairs, ie. both the true and compliment outputs should be terminated even if only one of the outputs will be used in the system. With both complimentary pairs terminated the current in the V_{CC} pins will remain essentially constant and thus inductance induced voltage glitches on V_{CC} will not occur. V_{CC} glitches will result in distorted output waveforms and degradations in the skew performance of the device.

The package parasitics of the 28-lead PLCC cause the signals on a given pin to be influenced by signals on adjacent pins. The E211 is characterized and tested with all of the outputs switching, therefore the numbers in the data book are guaranteed only for this situation. If all of the outputs of the E211 are not needed and there is a desire to save power the unused output pairs can be left unterminated. Unterminated outputs can influence the propagation delay on adjacent pins by 15ps - 20ps. Therefore under these conditions this 15ps - 20ps needs to be added to the overall skew of the device. Pins which are separated by a package corner are not considered adjacent pins in the context of propagation delay influence. Therefore as long as all of the outputs on a single side of the package are terminated the specification limits in the data sheet will apply.

APPLICATIONS INFORMATION

Differential versus Single-Ended Use

As can be seen from the data sheet, to minimize the skew of the E211 the device must be used in the differential mode. In the single-ended mode the propagation delays are dependent on the relative position of the V_{BB} switching reference. Any V_{BB} offset from the center of the input swing will add delay to either the T_{PLH} or T_{PHL} and subtract delay from the other. This increase and decrease in delay will lead to an increase in the duty cycle skew and thus part-to-part skew. The within-device skew will be independent of the V_{BB} and therefore will be the same regardless of whether the device is driven differentially or single-endedly.

For applications where part-to-part skew or duty cycle skew are not important the advantages of single-ended clock distribution may lead to its use. Using single-ended interconnect will reduce the number of signal traces to be routed, but remember that all of the complimentary outputs still need to be terminated therefore there will be no reduction in the termination components required. To use the E211 with a single-ended input the arrangement pictured in Figure 2b should be used. If the input to the differential CLK inputs are AC coupled as pictured in Figure 2a the dependence on a centered V_{BB} reference is removed. The situation pictured will ensure that the input is centered around the bias set by the V_{BB}. As a result when AC coupled the AC specification limits for a differential input can be used. For more information on AC coupling please refer to the interfacing section of the design guide in the ECLinPS data book.

Using the Enable Pins

Both the common enable ($\overline{CEN}$) and the individual enables ($\overline{ENx}$) are synchronous to the CLK or SCLK input depending on which is selected. The active low signals are clocked into the enable flip flops on the negative edges of the E211 clock inputs. In this way the devices will only be disabled when the outputs are already in the LOW state. The internal propagation delays are such that the delay to the output through the distribution buffers is less than that through the enable flip flops. This will ensure that the disabling of the device will not slice any time off the clock pulse. On initial power up the enable flip flops will randomly attain a stable state, therefore precautions should be taken on initial power up to ensure the E211 is in the desired state.

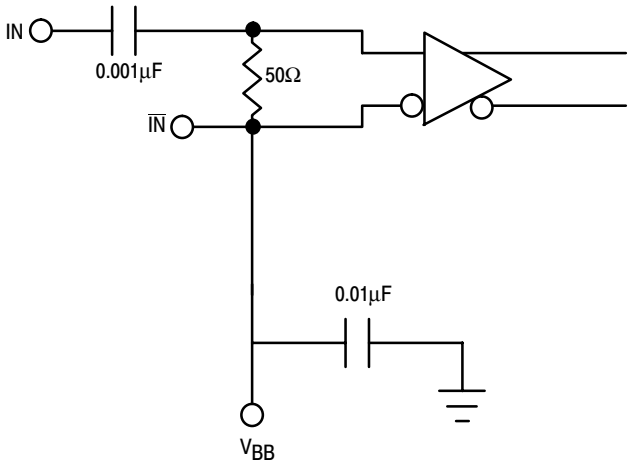


Figure 2a. AC Coupled Input

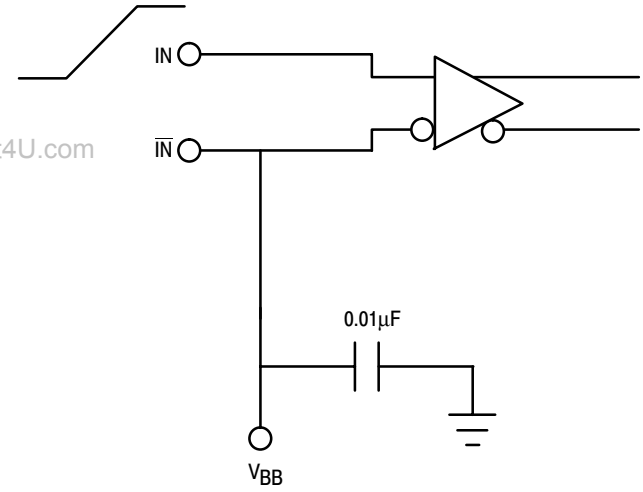


Figure 2b. Single-Ended Input

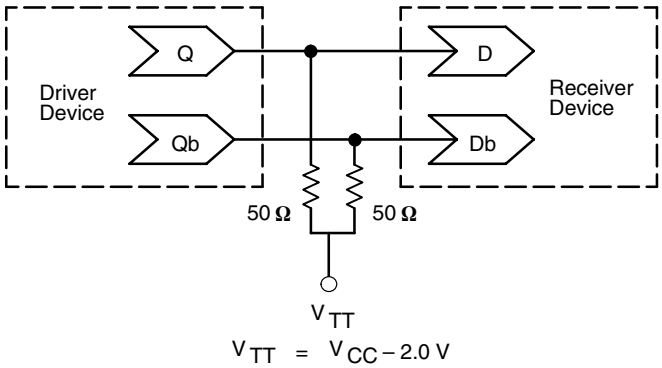


Figure 3. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E212, MC100E212

5V ECL 3-Bit Scannable Registered Address Driver

The MC10E/100E212 is a scannable registered ECL driver typically used as a fan-out memory address driver for ECL cache driving. In a VLSI array based CPU design, use of the E212 allows the user to conserve array output cell functionality and also output pins.

The input shift register is designed with control logic which greatly facilitates its use in boundary scan applications.

The 100 Series contains temperature compensation.

- Scannable Version E112 Driver
- 1025 ps Max. CLK to Output
- Dual Differential Outputs
- Master Reset
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 1 KV HBM, > 75 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 259 devices

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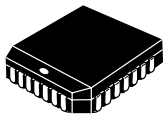


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAMS

28 1

28 1

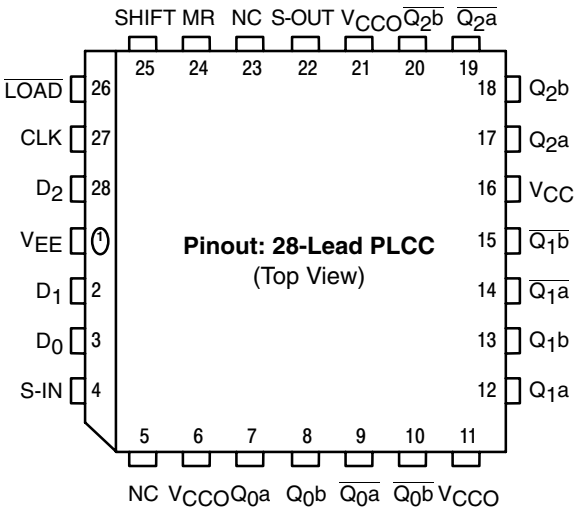
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E212FN	PLCC–28	37 Units/Rail
MC10E212FNR2	PLCC–28	500 Units/Reel
MC100E212FN	PLCC–28	37 Units/Rail
MC100E212FNR2	PLCC–28	500 Units/Reel

5

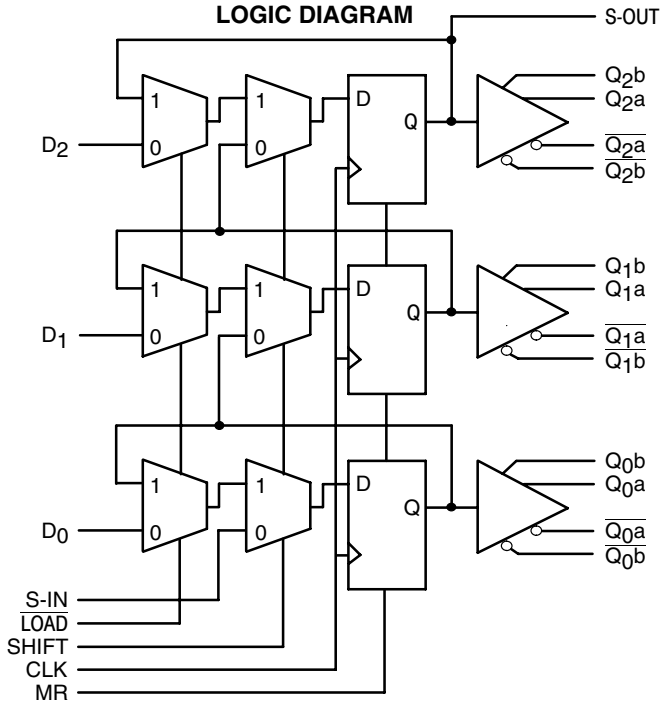
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN	FUNCTION
$D_0 - D_2$	ECL Data Inputs
S-IN	ECL Scan Input
$\overline{LOAD}$	ECL LOAD/HOLD Control
SHIFT	ECL Scan Control
CLK	ECL Clock
MR	ECL Reset
S-OUT	ECL Scan Output
Q[0:2]a, Q[0:2]b	ECL True Outputs
$\overline{Q}$[0:2]a, $\overline{Q}$[0:2]b	ECL Inverting Outputs
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

FUNCTION TABLE

$\overline{LOAD}$	SHIFT	MR	MODE
L	L	L	Load
H	L	L	Hold
X	H	L	Shift
X	X	H	Reset

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		80	96		80	96		80	96	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		80	96		80	96		80	96	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		80	96		80	96		92	110	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.4 6V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		80	96		80	96		92	110	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH}	Propagation Delay to Output										ps
t_{PHL}	CLK	575	800	1025	575	800	1025	575	800	1025	
	MR	575	800	1025	575	800	1025	575	800	1025	
	CLK to S-OUT	575	800	1025	575	800	1025	575	800	1025	
t_s	Setup Time										ps
	D	175	25		175	25		175	25		
	SHIFT	150	– 50		150	– 50		150	– 50		
	$\overline{LOAD}$	225	50		225	50		225	50		
	S-IN	150	– 50		150	– 50		150	– 50		
t_h	Hold Time										ps
	D	250	25		250	25		250	25		
	SHIFT	300	100		300	100		300	100		
	$\overline{LOAD}$	225	0		225	0		225	0		
	S-IN	300	100		300	100		300	100		
t_{RR}	Reset Recovery	600	350		600	350		600	350		ps
t_{SKEW}	Within-Device Skew (Note 2.)		100			100			100		ps
t_{SKEW}	Within-Gate Skew (Note 3.)		50			50			50		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r	Rise/Fall Times										ps
t_f	(20 - 80%)	275	425	650	275	425	650	275	425	650	

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.
3. Within-gate skew is defined as the difference in delays between various outputs of a gate when driven from the same input.

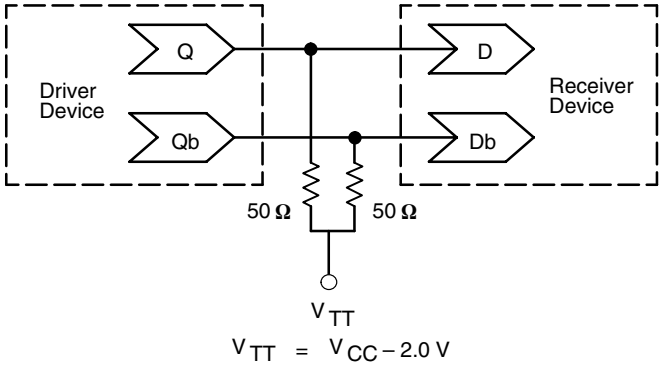


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E241, MC100E241

5V ECL 8-Bit Scannable Register

The MC10E/100E241 is an 8-bit shiftable register. Unlike a standard universal shift register such as the E141, the E241 features internal data feedback organized so that the SHIFT control overrides the HOLD/$\overline{\text{LOAD}}$ control. This enables the normal operations of HOLD and LOAD to be toggled with a single control line without the need for external gating. It also enables switching to scan mode with the single SHIFT control line.

The eight inputs $D_0 - D_7$ accept parallel input data, while S-IN accepts serial input data when in shift mode. Data is accepted a set-up time before the positive-going edge of CLK; shifting is also accomplished on the positive clock edge. A HIGH on the Master Reset pin (MR) asynchronously resets all the registers to zero.

The 100 Series contains temperature compensation.

- SHIFT overrides HOLD/$\overline{\text{LOAD}}$ Control
- 1000 ps Max. CLK to Q
- Asynchronous Master Reset
- Pin-Compatible with E141
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- ESD Protection: > 1 KV HBM, > 75 V MM
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 529 devices

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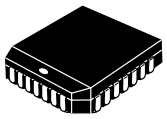
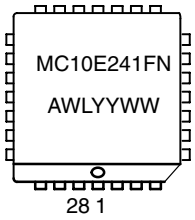


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAMS

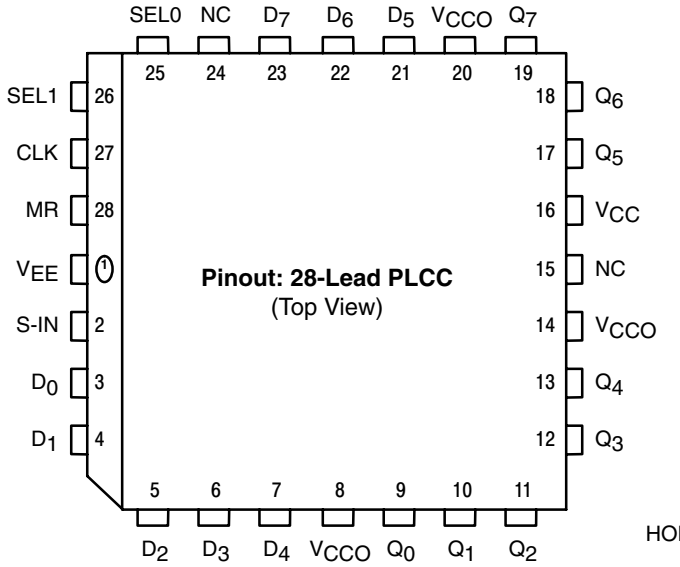


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E241FN	PLCC–28	37 Units/Rail
MC10E241FNR2	PLCC–28	500 Units/Reel
MC100E241FN	PLCC–28	37 Units/Rail
MC100E241FNR2	PLCC–28	500 Units/Reel

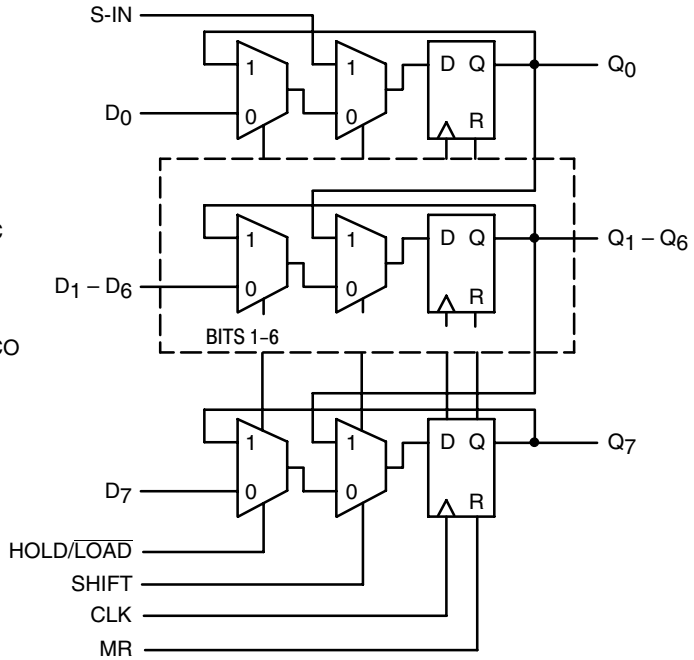
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN	FUNCTION
$D_0 – D_7$	ECL Parallel Date Inputs
S-IN	ECL Serial Data Inputs
SEL0	ECL SHIFT Control
SEL1	ECL HOLD/$\overline{\text{LOAD}}$ Control
CLK	ECL Clock
MR	ECL Master Reset
$Q_0 – Q_7$	ECL Data Outputs
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

FUNCTION TABLE

MR	SEL0	SEL1	Function
1	X	X	Outputs LOW
0	1	X	Shift Data
0	0	1	Hold Data
0	0	0	Load Data

X = Don't Care

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		125	150		125	150		125	150	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		125	150		125	150		125	150	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		125	150		125	150		144	173	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		125	150		125	150		144	173	mA
V_{OH}	Output HIGH Voltage	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
f_{SHIFT}	Max. Shift Frequency	700	900		700	900		700	900		MHz
t_{PLH} t_{PHL}	Propagation Delay to Output										ps
	Clk	625	750	975	625	750	975	625	750	975	
	MR	600	725	975	600	725	975	600	725	975	
t_s	Setup Time										ps
	D	175	25		175	25		175	25		
	SEL0 (SHIFT)	350	200		350	200		350	200		
	SEL1 (HOLD/$\overline{\text{LOAD}}$)	400	250		400	250		400	250		
	S-IN	125	–100		125	–100		125	–100		
t_h	Hold Time										ps
	D	200	– 25		200	– 25		200	– 25		
	SEL0 (SHIFT)	100	– 200		100	– 200		100	– 200		
	SEL1 (HOLD/$\overline{\text{LOAD}}$)	50	– 250		50	– 250		50	– 250		
	S-IN	300	100		300	100		300	100		
t_{RR}	Reset Recovery Time	900	600		900	600		900	600		ps
t_{PW}	Minimum Pulse Width										ps
	Clk, MR	400			400			400			
t_{SKEW}	Within-Device Skew (Note 2.)		60			60			60		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Rise/Fall Times										ps
	(20 - 80%)	300	525	800	300	525	800	300	525	800	

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.

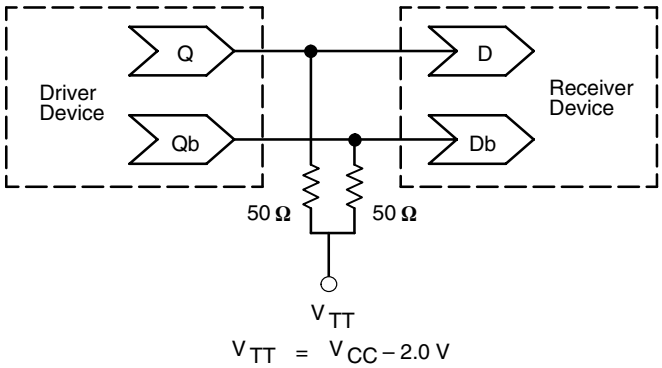


Figure 1. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E256, MC100E256

5V ECL 3-Bit 4:1 Mux-Latch

The MC10E/100E256 contains three 4:1 multiplexers followed by transparent latches with differential outputs. Separate Select controls are provided for the leading 2:1 mux pairs (see logic symbol).

When the Latch Enable (LEN) is LOW, the latch is transparent, and output data is controlled by the multiplexer select controls. A logic HIGH on LEN latches the outputs. The Master Reset (MR) overrides all other controls to set the Q outputs LOW.

The 100 Series contains temperature compensation.

- 950 ps Max. D to Output
- 850 ps Max. LEN to Output
- Split Select
- Differential Outputs
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 1 KV HBM, > 75 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 280 devices

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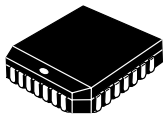
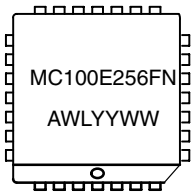
MARKING DIAGRAMS



PLCC–28
FN SUFFIX
CASE 776

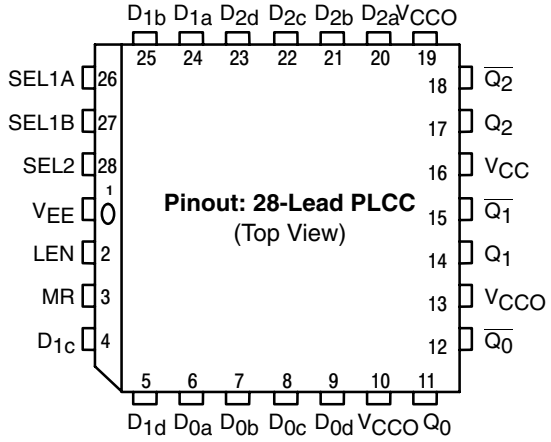
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week



ORDERING INFORMATION

Device	Package	Shipping
MC10E256FN	PLCC–28	37 Units/Rail
MC10E256FNR2	PLCC–28	500 Units/Reel
MC100E256FN	PLCC–28	37 Units/Rail
MC100E256FNR2	PLCC–28	500 Units/Reel

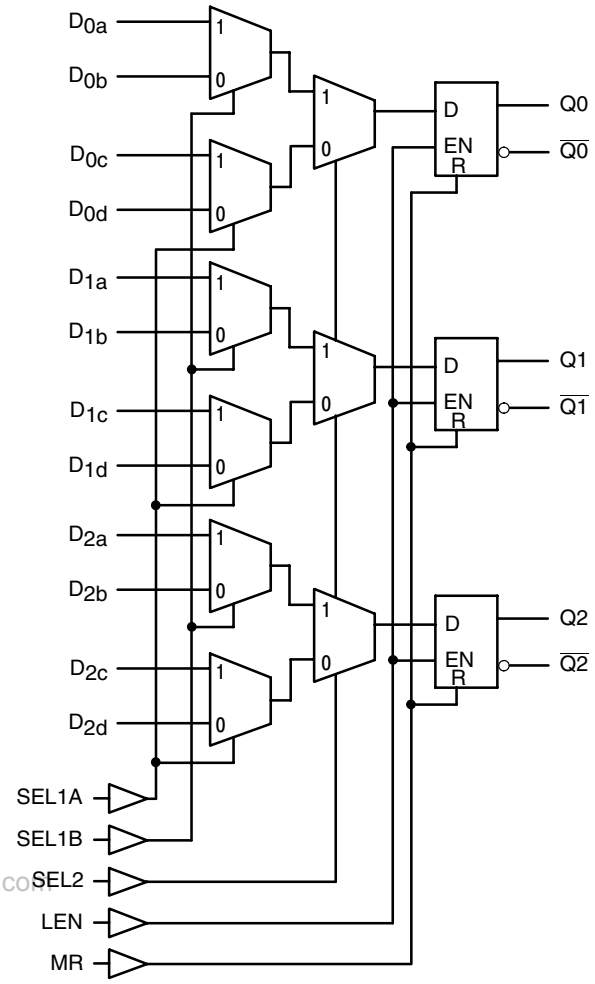
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN	FUNCTION
$D_{0x} - D_{2x}$	ECL Data Inputs
SEL1A, SEL1B	ECL First-stage Select Inputs
SEL2	ECL Second-stage Select Input
LEN	ECL Latch Enable
MR	ECL Master Reset
Q_0, $\overline{Q_0} - Q_2$, $\overline{Q_2}$	ECL Data Outputs
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply

FUNCTION TABLE

Pin	State	Operation
SEL2	H	Output c/d Data
SEL1A	H	Input d Data
SEL1B	H	Input b Data

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		69	83		69	83		69	83	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		69	83		69	83		69	83	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		69	83		69	83		79	96	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		69	83		69	83		79	96	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output										ps
	D	400	600	900	400	600	900	400	600	900	
	SEL1	550	775	1050	550	775	1050	550	775	1050	
	SEL2	450	650	900	450	650	900	450	650	900	
	LEN	350	500	800	350	500	800	350	500	800	
	MR	350	600	825	350	600	825	350	600	825	
t_s	Setup Time										ps
	D	400	275		400	275		400	275		
	SEL1	600	300		600	300		600	300		
	SEL2	500	250		500	250		500	250		
t_h	Hold Time										ps
	D	300	– 275		300	– 275		300	– 275		
	SEL1	100	– 300		100	– 300		100	– 300		
	SEL2	200	– 250		200	– 250		200	– 250		
t_{RR}	Reset Recovery Time	700	600		700	600		700	600		ps
t_{PW}	Minimum Pulse Width										ps
	MR	400			400			400			
t_{SKEW}	Within-Device Skew (Note 2.)		50			50			50		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Rise/Fall Times (20 - 80%)	275	475	700	275	475	700	275	475	700	ps

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.

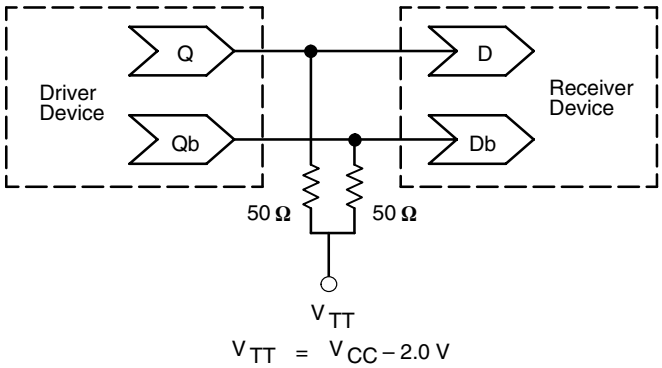


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC100E310

5V ECL Low Voltage 2:8 Differential Fanout Buffer

The MC100E310 is a low voltage, low skew 2:8 differential ECL fanout buffer designed with clock distribution in mind. The device features fully differential clock paths to minimize both device and system skew. The E310 offers two selectable clock inputs to allow for redundant or test clocks to be incorporated into the system clock trees.

The lowest tpd delay time results from terminating only one output pair, and the greatest tpd delay time results from terminating all the output pairs. This shift is about 10–20 pS in tpd. The skew between any two output pairs within a device is typically about 25 nS. If other output pairs are not terminated, the lowest tpd delay time results from both output pairs and the skew is typically 25 nS. When all outputs are terminated, the greatest tpd (delay time) occurs and all outputs display about the same 10–20 pS increase in tpd, so the relative skew between any two output pairs remains about 25 nS.

For more information on using PECL, designers should refer to ON Semiconductor Application Note AN1406/D.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- Dual Differential Fanout Buffers
- 200 ps Part–to–Part Skew
- 50 ps Output–to–Output Skew
- 28–lead PLCC Packaging
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at V_{EE}
- ESD Protection: >2KV HBM, >200V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 212 devices

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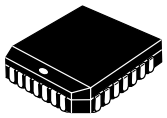
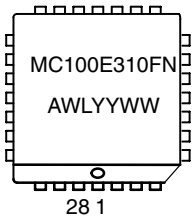


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAMS



28 1

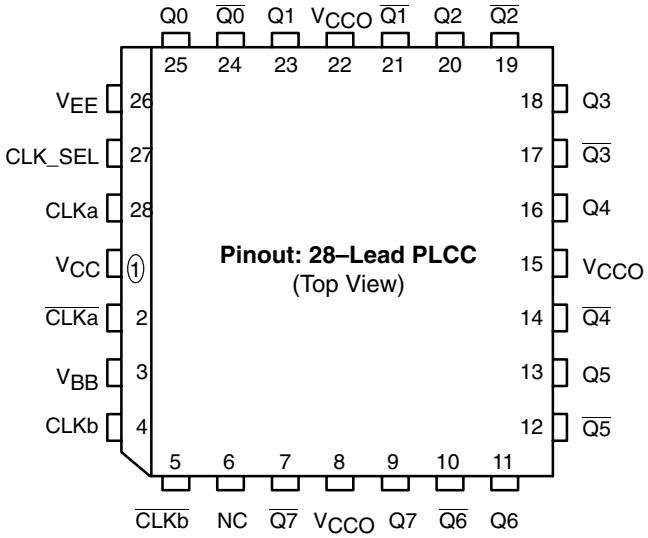
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC100E310FN	PLCC–28	37 Units/Rail
MC100E310FNR2	PLCC–28	500 Units/Reel

MC100E310

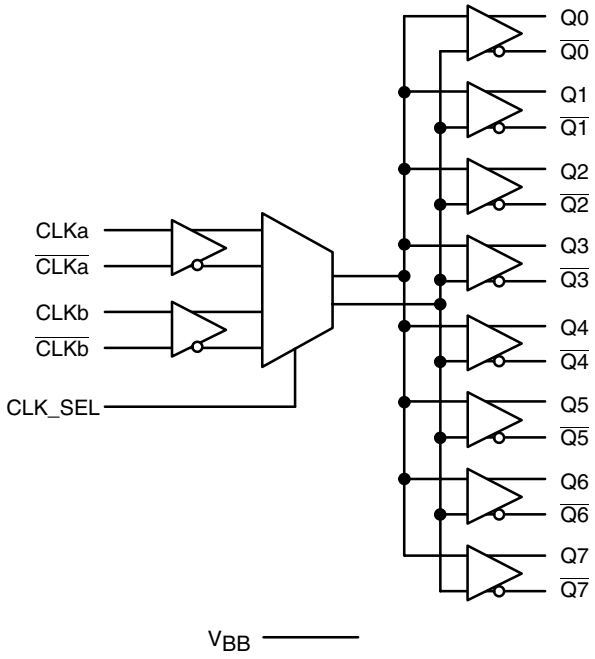
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC SYMBOL



PIN DESCRIPTION

PIN	FUNCTION
CLKa, CLKb;	ECL Differential Input Pairs
$\overline{CLKa}$, $\overline{CLKb}$	ECL Differential Input Pairs
Q0:7; $\overline{Q0}$:$\overline{7}$	ECL Differential Outputs
CLK_SEL	ECL Input Clock Select
V_{BB}	Reference Voltage Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

FUNCTION TABLE

CLK_SEL	Input Clock
0	CLKa Selected
1	CLKb Selected

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		55	60		55	60		65	70	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.7		4.6	2.7		4.6	2.7		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		55	60		55	60		65	70	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.3		–0.4	–2.3		–0.4	–2.3		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

MC100E310 ECL DC CHARACTERISTICS

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage	–1.085	–1.005	–0.880	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	V
V_{OL}	Output LOW Voltage	–1.830	–1.695	–1.555	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	V
V_{IH}	Input HIGH Voltage	–1.165		–0.880	–1.165		–0.880	–1.165		–0.880	–1.165		–0.880	V
V_{IL}	Input LOW Voltage	–1.810		–1.475	–1.810		–1.475	–1.810		–1.475	–1.810		–1.475	V
V_{BB}	Output Reference Voltage	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{EE}	Power Supply Voltage	–5.25		–4.2	–5.25		–4.2	–5.25		–4.2	–5.25		–4.2	V
I_{IH}	Input HIGH Current			150			150			150			150	μA
I_{EE}	Power Supply Current		55	60		55	60		55	60		65	70	mA

MC100E310 PECL DC CHARACTERISTICS

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage (Note 1.)	3.915	3.995	4.12	3.975	4.045	4.12	3.975	4.045	4.12	3.975	4.045	4.12	V
V_{OL}	Output LOW Voltage (Note 1.)	3.170	3.305	3.445	3.19	3.295	3.38	3.19	3.295	3.38	3.19	3.295	3.38	V
V_{IH}	Input HIGH Voltage (Note 1.)	3.835		4.12	3.835		4.12	3.835		4.12	3.835		4.12	V
V_{IL}	Input LOW Voltage (Note 1.)	3.190		3.525	3.190		3.525	3.190		3.525	3.190		3.525	V
V_{BB}	Output Reference Voltage (Note 1.)	3.62		3.74	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{CC}	Power Supply Voltage	4.75		5.25	4.75		5.25	4.75		5.25	4.75		5.25	V
I_{IH}	Input HIGH Current			150			150			150			150	μA
I_{EE}	Power Supply Current		55	60		55	60		55	60		65	70	mA

1. These values are for V_{CC} = 5.0 V. Level Specifications will vary 1:1 with V_{CC}.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output IN (differential) (Note 2.) IN (single–ended) (Note 3.)	 525 500		 725 750	 550 550		 750 800	 575 600		 775 850	ps
t_{skew}	Within–Device Skew (Note 4.) Part–to–Part Skew (Diff)			75 250			50 200			50 200	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Minimum Input Swing (Note 5.)	500			500			500			mV
t_r/t_f	Output Rise/Fall Time (20%–80%)	200		600	200		600	200		600	ps

1. V_{EE} can vary +0.46 V / –0.8 V.
2. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the ON Semiconductor High Performance ECL Data Book (DL140/D).
3. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the ON Semiconductor High Performance ECL Data Book (DL140/D).
4. The within–device skew is defined as the worst case difference between any two similar delay paths within a single device.
5. V_{PP}(min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP}(min) is AC limited for the E310 as a differential input as low as 50 mV will still produce full ECL levels at the output.

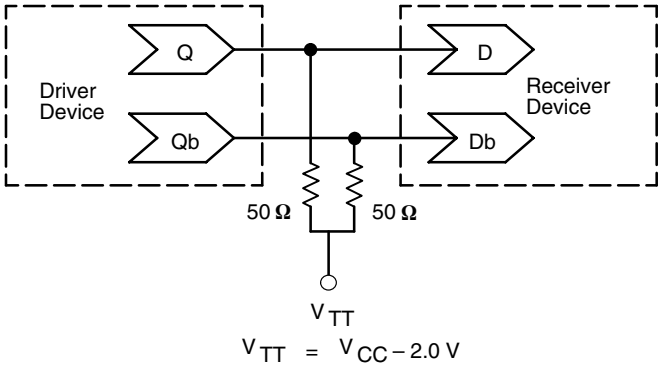


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E336, MC100E336

5V ECL 3-Bit Registered Bus Transceiver

The MC10E/MC100E336 contains three bus transceivers with both transmit and receive registers. The bus outputs ($\overline{BUS0}$–$\overline{BUS2}$) are specified for driving a 25 Ω bus; the receive outputs (Q0 – Q2) are specified for 50 Ω. The bus outputs feature a normal HIGH level (V_{OH}) and a cutoff LOW level — when LOW, the outputs go to –2.0 V and the output emitter-follower is "off", presenting a high impedance to the bus. The bus outputs also feature edge slow-down capacitors.

The Transmit Enable pins (TEN) control whether current data is held in the transmit register, or new data is loaded from the A/B inputs. A LOW on both of the Bus Enable inputs (BUSEN), when clocked through the register, disables the bus outputs to –2.0 V.

The receiver section clocks bus data into the receive registers, after gating with the Receive Enable ($\overline{RXEN}$) input.

All registers are clocked by a positive transition of CLK1 or CLK2 (or both).

Additional leadframe grounding is provided through the Ground pins (GND) which should be connected to 0 V. The GND pins are not electrically connected to the chip.

The 100 Series contains temperature compensation.

- 25 Ω Cutoff Bus Outputs
- 50 Ω Receiver Outputs
- Transmit and Receive Registers
- 1500 ps Max. Clock to Bus
- 1000 ps Max. Clock to Q
- Bus Outputs Feature Internal Edge Slow-Down Capacitors
- Additional Package Ground Pins
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 1 KV HBM, > 75 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8",
  Oxygen Index 28 to 34
- Transistor Count = 430 devices

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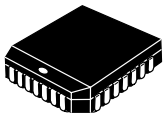
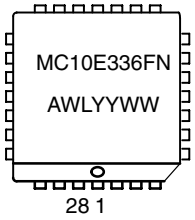
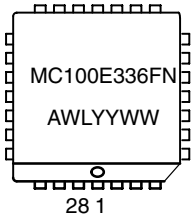


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAMS



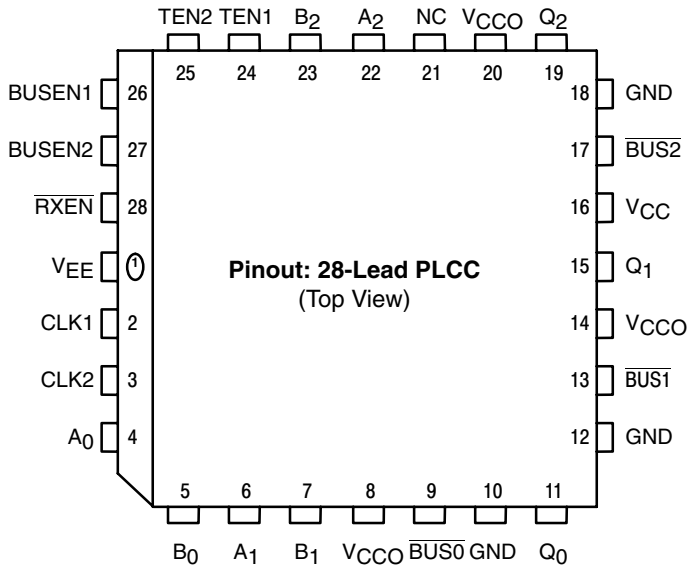


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E336FN	PLCC–28	37 Units/Rail
MC10E336FNR2	PLCC–28	500 Units/Reel
MC100E336FN	PLCC–28	37 Units/Rail
MC100E336FNR2	PLCC–28	500 Units/Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



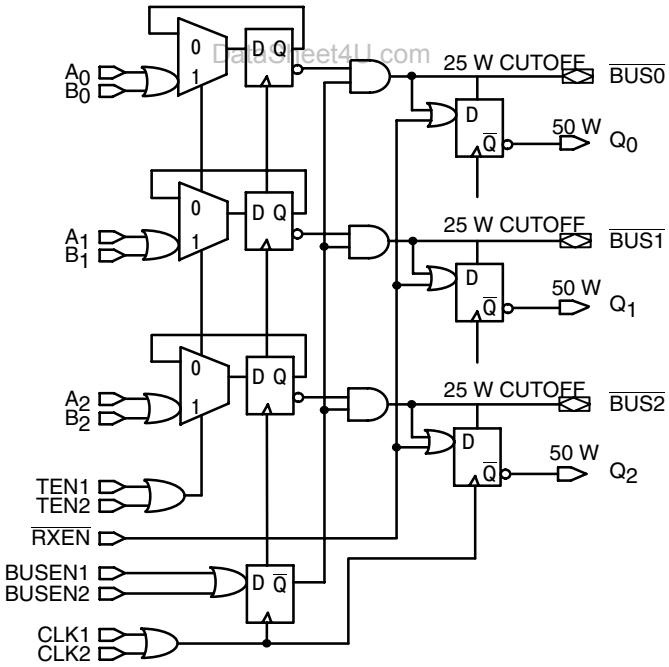
* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

PIN	FUNCTION
TEN1, TEN2	ECL Transit Enable
A0–A2	ECL Data Inputs A
B0–B2	ECL Data Inputs B
Q0–Q1	ECL Output
BUSEN1, BUSEN2	ECL Bus Enables
$\overline{BUS0}$–$\overline{BUS2}$	ECL Bus Outputs
$\overline{RXEN}$	ECL Receive Enable
CLK1, CLK2	ECL Clock Input
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
GND	Ground
NC	No Connect

LOGIC DIAGRAM



MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		125	150		125	150		125	150	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
V_{CUT}	Cut-off Output Voltage (Note 2.)	2.9		2.97	2.9		2.97	2.9		2.97	V
I_{IH}	Input HIGH Current $\overline{RXEN}$ All Other Inputs			 225 150			 225 150			 225 150	µA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC} –2.10 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		125	150		125	150		125	150	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
V_{CUT}	Cut-off Output Voltage (Note 2.)	2.9		2.97	2.9		2.97	2.9		2.97	V
I_{IH}	Input HIGH Current $\overline{RXEN}$ All Other Inputs			 225 150			 225 150			 225 150	µA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC} –2.10 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		125	150		125	150		144	173	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
V_{CUT}	Cut-off Output Voltage (Note 2.)	2.9		2.97	2.9		2.97	2.9		2.97	V
I_{IH}	Input HIGH Current $\overline{RXEN}$ All Other Inputs			 225 150			 225 150			 225 150	µA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC} –2.10 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		125	150		125	150		144	173	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
V_{CUT}	Cut-off Output Voltage (Note 2.)	2.9		2.97	2.9		2.97	2.9		2.97	V
I_{IH}	Input HIGH Current $\overline{RXEN}$ All Other Inputs			 225 150			 225 1502			 225 150	µA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		µA

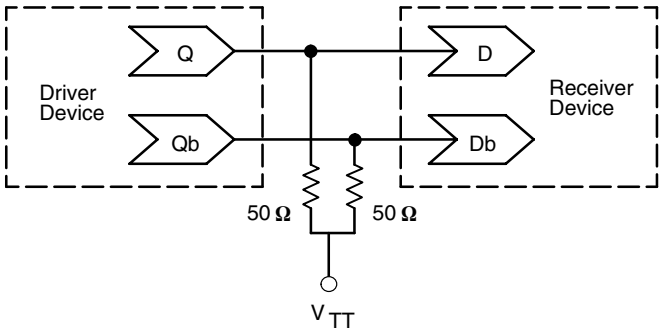
NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC} –2.10 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH}	Propagation Delay to Output										ps
t_{PHL}	Clk to Q	500	700	100	500	700	1000	500	700	1000	
	Clk to $\overline{BUS}$	825	1250	1800	825	1250	1800	825	1250	1800	
t_s	Setup Time										ps
	$\overline{BUS}$, $\overline{RXEN}$	150	–150		150	–150		150	–150		
	BUSEN	100	– 200		100	– 200		100	– 200		
	A, B Data	300	– 50		300	– 50		300	– 50		
	TEN	450	150		450	150		450	150		
t_h	Hold Time										ps
	$\overline{BUS}$, $\overline{RXEN}$	450	150		450	150		450	150		
	BUSEN	500	200		500	200		500	200		
	A, B Data	350	50		350	50		350	50		
	TEN	200	–150		200	–150		200	–150		
t_{PW}	Minimum Pulse Width										ps
	Clk	400			400			400			
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r	Rise/Fall Times										ps
t_f	20 - 80% (Qn)	300	450	700	300	450	700	300	450	700	
	20 - 80% ($\overline{BUSn}$ Rise)	500	800	1000	500	800	1000	500	800	1000	
	20 - 80% ($\overline{BUSn}$ Fall)	300	500	800	300	500	800	300	500	800	

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.



$V^{TT} = V_{CC}$ –2.10 V

Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
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AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E337, MC100E337

5V ECL 3-Bit Scannable Registered Bus Transceiver

The MC10E/100E337 is a 3-bit registered bus transceiver with scan. The bus outputs (BUS0–BUS2) are specified for driving a 25 Ω bus; the receive outputs (Q0 – Q2) are specified for 50 Ω The bus outputs feature a normal HIGH level (V_{OH}) and a cutoff LOW level — when LOW, the outputs go to – 2.0 V and the output emitter-follower is "off", presenting a high impedance to the bus. The bus outputs also feature edge slow-down capacitors.

Both drive and receive sides feature the same logic, including a loopback path to hold data. The HOLD/LOAD function is controlled by Transmit Enable (TEN) and Receive Enable (REN) on the transmit and receive sides respectively, with a HIGH selecting LOAD. Note that the implementation of the E337 Receive Enable differs from that of the E336.

A synchronous bus enable (SBUSEN) is provided for normal, non-scan operation. The asynchronous bus disable (ABUSDIS) disables the bus immediately for scan mode.

The $\overline{\text{SYNCEN}}$ input is provided for flexibility when re-enabling the bus after disabling with ABUSDIS, allowing either synchronous or asynchronous re-enabling. An alternative use is asynchronous-only operation with ABUSDIS, in which case $\overline{\text{SYNCEN}}$ is tied LOW, or left open. $\overline{\text{SYNCEN}}$ is implemented as an overriding SET control (active-LOW) to the enable flip-flop.

Scan mode is selected by a HIGH at the SCAN input. Scan input data is shifted in through S_IN and output data appears at the Q2 output.

All registers are clocked on the positive transition of CLK. Additional lead-frame grounding is provided through the Ground pins (GND) which should be connected to 0V. The GND pins are not electrically connected to the chip.

The 100 Series contains temperature compensation.

- Scannable Version of E336
- 25 Ω Cutoff Bus Outputs
- 50 Ω Receiver Outputs
- Scannable Registers
- Sync. and Async. Bus Enables
- Non-inverting Data Path
- 1500 ps Max. Clock to Bus (Data Transmit)
- 1000 ps Max. Clock to Q (Data Receive)
- Bus Outputs Feature Internal Edge Slow-Down Capacitors
- Additional Package Ground Pins
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 1 KV HBM, > 75 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8",
  Oxygen Index 28 to 34
- Transistor Count = 471 devices

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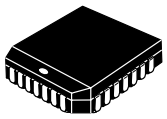
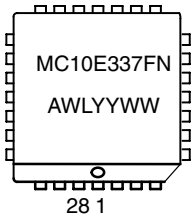


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAMS



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

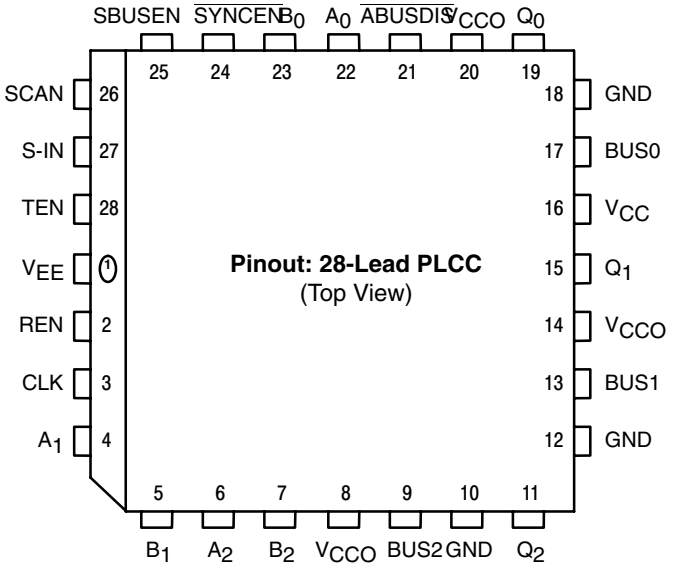
ORDERING INFORMATION

Device	Package	Shipping
MC10E337FN	PLCC–28	37 Units/Rail
MC10E337FNR2	PLCC–28	500 Units/Reel
MC100E337FN	PLCC–28	37 Units/Rail
MC100E337FNR2	PLCC–28	500 Units/Reel

PIN DESCRIPTION

PIN	FUNCTION
$A_0 - A_2$	ECL Data Inputs A
$B_0 - B_2$	ECL Data Inputs B
S-IN	ECL Serial (Scan) Data Input
TEN, REN	HOLD/$\overline{\text{LOAD}}$ Controls
SCAN	ECL Scan Control
$\overline{\text{ABUSDIS}}$	ECL Asynchronous Bus Disable
SBUSEN	ECL Synchronous Bus Enable
$\overline{\text{SYNCEN}}$	ECL Synchronous Enable Control
CLK	ECL Clock
BUS0 – BUS2	ECL 25Ω Cutoff Bus Outputs
$Q_0 - Q_2$	ECL Receive Data Outputs (Q2 serves as SCAN_OUT in scan mode)
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
GND	Ground

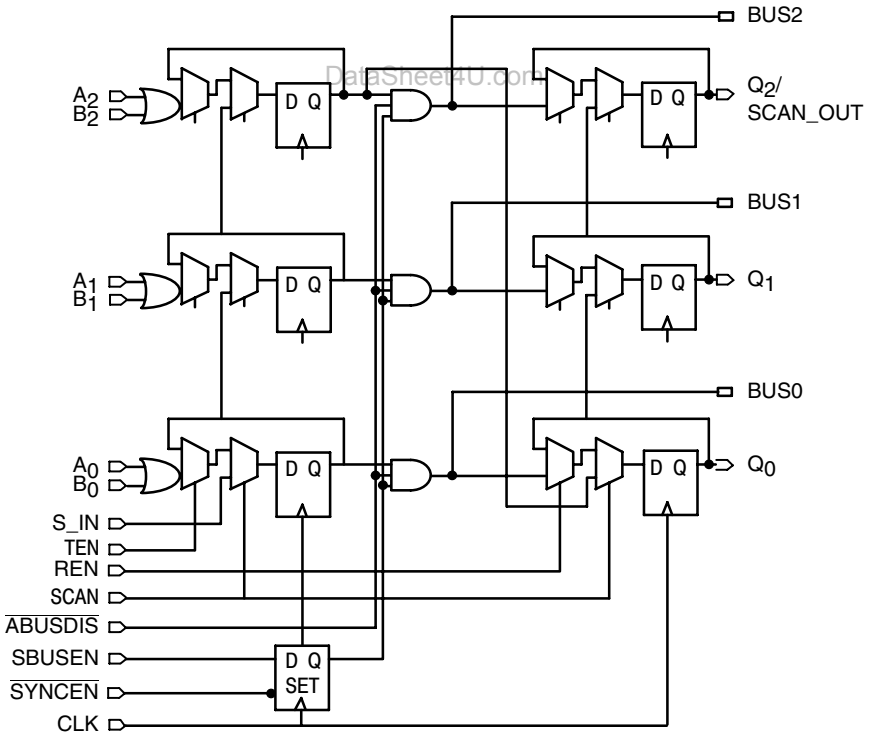
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		145	174		145	174		145	174	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
V_{CUT}	Cut-off Output Voltage (Note 2.)	2.9		2.97	2.9		2.97	2.9		2.97	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC} –2.10 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		145	174		145	174		145	174	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
V_{CUT}	Cut-off Output Voltage (Note 2.)	2.9		2.97	2.9		2.97	2.9		2.97	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC} –2.10 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		145	174		145	174		167	200	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
V_{CUT}	Cut-off Output Voltage (Note 2.)	2.9		2.97	2.9		2.97	2.9		2.97	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC} –2.10 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		145	174		145	174		167	200	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
V_{CUT}	Cut-off Output Voltage (Note 2.)	2.9		2.97	2.9		2.97	2.9		2.97	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC} –2.10 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} / t_{PHL}	Propagation Delay to Output										ps
	Clk to Q	450		1000	450		1000	450		1000	
	Clk to BUS	800		1800	800		1800	800		1800	
	$\overline{\text{ABUSDIS}}$	500		1500	500		1500	500		1500	
	$\overline{\text{SYNCEN}}$	800		1800	800		1800	800		1800	
t_s	Setup Time										ps
	BUS	350			350			350			
	SBUSEN	100			100			100			
	Data, S-IN	400			400			400			
	TEN, REN, SCAN	550			550			550			
t_h	Hold TIme										ps
	BUS	350			350			350			
	SBUSEN	500			500			500			
	Data, S-IN	350			350			350			
	TEN, REN, SCAN	200			200			200			
t_{PW}	Minimum Pulse Width										ps
	CLk	400			400			400			
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r / t_f	Rise/Fall Times										ps
	20 - 80% (Qn)	300		800	300		800	300		800	
	20 - 80% (BUSn Rise)	500		1000	500		1000	500		1000	
	20 - 80% (BUSn Fall)	300		800	300		800	300		800	

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
100 Series: V_{EE} can vary +0.46 V / –0.8 V.

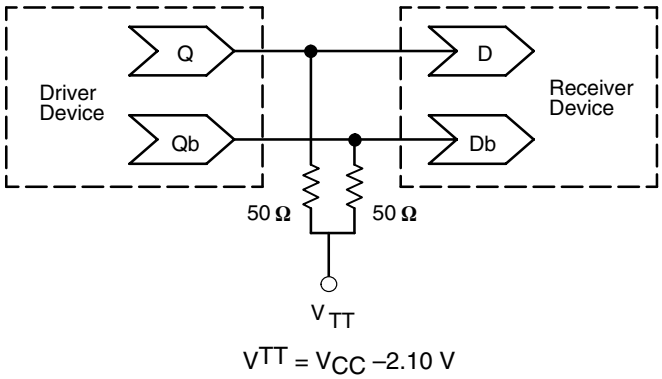


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E404, MC100E404

5V ECL Quad Differential AND/NAND

The MC10E404/100E404 is a 4-bit differential AND/NAND device. The differential operation of the device makes it ideal for pulse shaping applications where duty cycle skew is critical. Special design techniques were incorporated to minimize the skew between the upper and lower level gate inputs.

Because a negative 2-input NAND function is equivalent to a 2-input OR function, the differential inputs and outputs of the device also allow for its use as a fully differential 2 input OR/NOR function.

The output RISE/FALL times of this device are significantly faster than most other standard ECLinPS ™ devices resulting in an increased bandwidth.

The differential inputs have clamp structures which will force the Q output of a gate in an open input condition to go to a LOW state. Thus, inputs of unused gates can be left open and will not affect the operation of the rest of the device. Note that the input clamp will take affect only if both inputs fall 2.5 V below V_{CC}.

The 100 Series contains temperature compensation.

- Differential D and Q
- 700 ps Max. Propagation Delay
- High Frequency Outputs
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 1 KV HBM, > 75 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 274 devices

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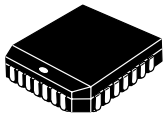
MARKING DIAGRAMS



PLCC–28
FN SUFFIX
CASE 776

28 1

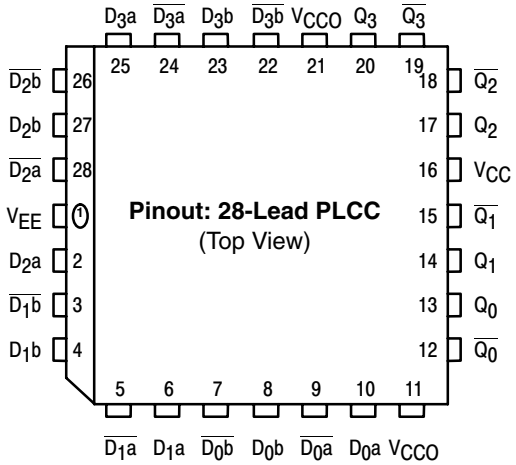
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

28 1

ORDERING INFORMATION

Device	Package	Shipping
MC10E404FN	PLCC–28	37 Units/Rail
MC10E404FNR2	PLCC–28	500 Units/Reel
MC100E404FN	PLCC–28	37 Units/Rail
MC100E404FNR2	PLCC–28	500 Units/Reel

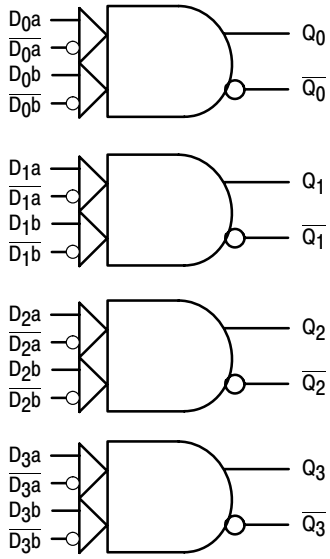
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN	FUNCTION
D[0:4], $\overline{D}$[0:4]	ECL Differential Data Inputs
Q[0:4], $\overline{Q}$[0:4]	ECL Differential Data Outputs
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply

FUNCTION TABLE

Da	Db	Q	$\overline{Da}$	$\overline{Db}$	$\overline{Q}$
L	L	L	L	L	L
L	H	L	L	H	H
H	L	L	H	L	H
H	H	H	H	H	H

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		106	127		106	127		106	127	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		106	127		106	127		106	127	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		106	127		106	127		122	146	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		106	127		106	127		122	146	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output										ps
	Da (Diff)	350	475	650	350	475	650	350	475	650	
	Da (SE)	300	475	700	300	475	700	300	475	700	
	Db (Diff)	375	500	675	375	500	675	375	500	675	
	Db (SE)	325	500	725	325	500	725	325	500	725	
t_{SKEW}	Within-Device Skew (Note 2.)		50			50			50		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}(AC)	Minimum Input Swing (Note 3.)	150			150			150			mV
t_r t_f	Rise/Fall Time (20 - 80%)	150		400	150		400	150		400	ps

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.
3. Minimum input swing for which AC parameters are guaranteed.

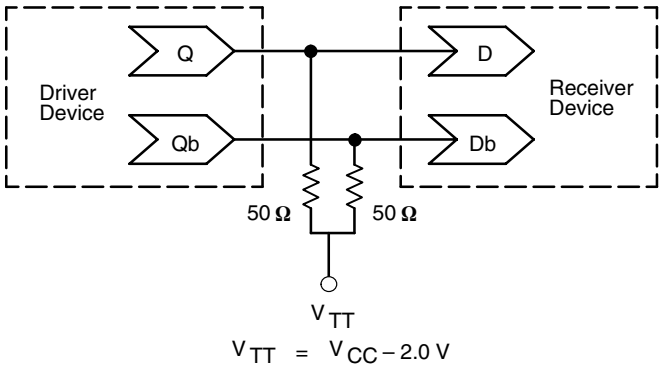


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E411

5V ECL 1:9 Differential PECL/NECL RAMBus Clock Buffer

The MC10E411 is a low skew 1-to-9 differential driver, designed with clock distribution in mind. The MC10E411's function and performance are similar to the popular MC10E111, with the added feature of 1.2 V output swings.

The output voltage swing of the E411 is larger than a standard ECL swing. The 1.2 V output swings provide a signal which can be AC coupled into RAMBus compatible input loads. The larger output swings are produced by lowering the V_{OL} of the device. With the exception of the lower V_{OL}, the E411 is identical to the MC10E111. Note that the larger output swings eliminate the possibility of temperature compensated outputs, thus the E411 is only available in the 10E style of ECL. In addition, because the V_{OL} is lower than standard ECL, the outputs cannot be terminated to –2.0 V. This data sheet provides a few termination alternatives.

The E411 is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate to gate skew within a device, and empirical modeling is used to determine process control limits that ensure consistent t_{pd} distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated, even if only one side is being used. In most applications, all nine differential pairs will be used and therefore terminated. In the case where fewer than nine pairs are used, it is necessary to terminate at least the output pairs on the same package side as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20 ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

The MC10E411, as with most other ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the E411 to be used for high performance clock distribution in +5.0 V systems. Designers can take advantage of the E411's performance to distribute low skew clocks across the backplane or the board. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For more information on using PECL, designers should refer to ON Semiconductor Application Note AN1406/D.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

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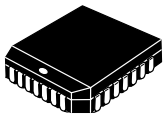
MARKING DIAGRAMS



PLCC–28
FN SUFFIX
CASE 776

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

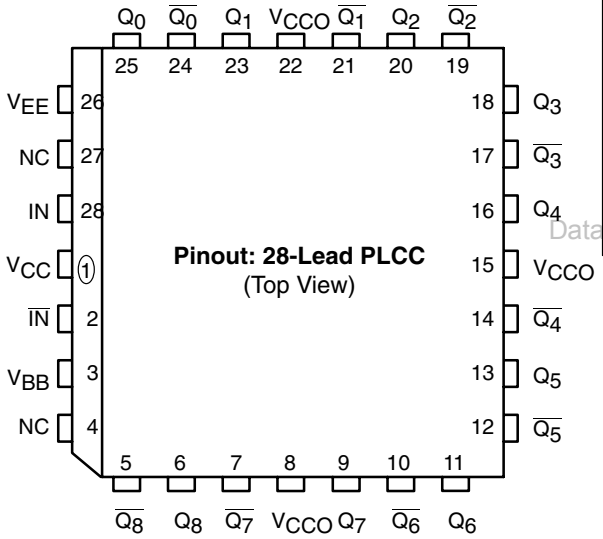
ORDERING INFORMATION

Device	Package	Shipping
MC10E411FN	PLCC–28	37 Units/Rail
MC10E411FNR2	PLCC–28	500 Units/Reel

MC10E411

- 200 ps Part-to-Part Skew
- 50 ps Output-to-Output Skew
- Differential Design
- V_{BB} Output
- Voltage Compensated Outputs
- V_{EE} Range of –4.5 to –5.5 V
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 200 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 180 devices

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



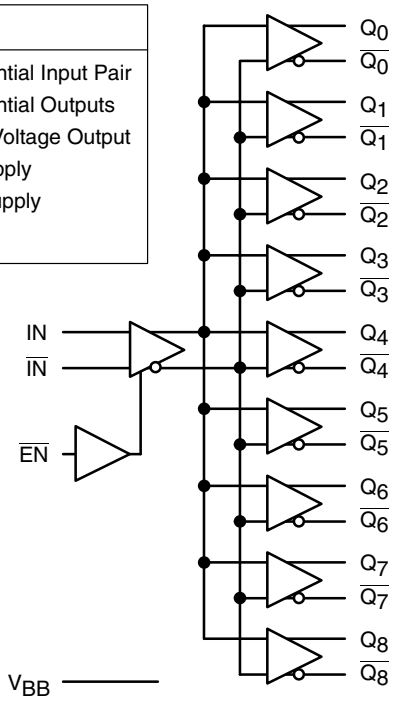
* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

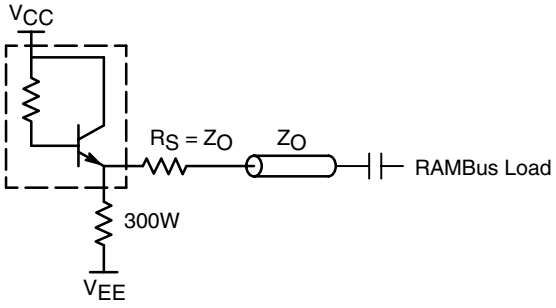
PIN DESCRIPTION

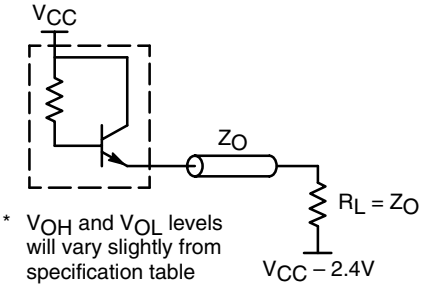
PIN	FUNCTION
IN, $\overline{IN}$	ECL Differential Input Pair
Q0, $\overline{Q0}$–Q8, $\overline{Q8}$	ECL Differential Outputs
V_{BB}	Reference Voltage Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

LOGIC SYMBOL



TERMINATION ALTERNATIVES





* V_{OH} and V_{OL} levels will vary slightly from specification table

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		55	65		55	65		55	65	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage (Single Ended)	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
V_{BB}	Output Voltage Reference	3.62		3.73	3.65		3.75	3.69		3.81	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.9		4.6	2.9		4.6	2.9		4.6	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.5 V / –0.5 V.
2. Outputs are terminated through a 300 ohm resistor to V_{EE}.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		55	65		55	65		55	65	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–2420		–2410	–2380	–2250	–2110	–2310		–2020	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
V_{BB}	Output Voltage Reference	–1.38		–1.27	–1.35		–1.25	–1.31		–1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.1		–2.4	–2.1		–0.4	–2.1		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.5 V / –0.5 V.
2. Outputs are terminated through a 300 ohm resistor to V_{EE}.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output IN (differential) (Note 2.) IN (single-ended) (Note 3.) $\overline{EN}$ to Q	 400 350 450		 600 650 850	 430 380 450		 630 680 850	 500 450 450		 700 750 850	ps
t_s	Setup Time (Note 4.) $\overline{EN}$ to IN	200	0		200	0		200	0		ps
t_H	Hold Time (Note 5.) IN to $\overline{EN}$	0	–200		0	–200		0	–200		ps
t_R	Release Time (Note 6.) $\overline{EN}$ to IN	300	100		300	100		300	100		ps
t_{skew}	Within-Device Skew (Note 7.) Part-to-Part Skew (Diff)			50 200			50 200			50 200	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Minimum Input Swing (Note 8.)	250		1000	250		1000	250		1000	mV
t_r/t_f	Output Rise/Fall Time (20%–80%)	275		600	275		600	275		600	ps

1. V_{EE} can vary +0.5 V / –0.5 V.
2. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
3. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
4. The setup time is the minimum time that $\overline{EN}$ must be asserted prior to the next transition of IN/$\overline{IN}$ to prevent an output response greater than ±75 mV to that IN/$\overline{IN}$ transition (see Figure 1).
5. The hold time is the minimum time that $\overline{EN}$ must remain asserted after a negative going IN or a positive going $\overline{IN}$ to prevent an output response greater than ±75 mV to that IN/$\overline{IN}$ transition (see Figure 2).
6. The release time is the minimum time that $\overline{EN}$ must be deasserted prior to the next IN/$\overline{IN}$ transition to ensure an output response that meets the specified IN to Q propagation delay and output transition times (see Figure 3).
7. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
8. V_{PP}(min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP}(min) is AC limited for the E411 as a differential input as low as 50 mV will still produce full ECL levels at the output.

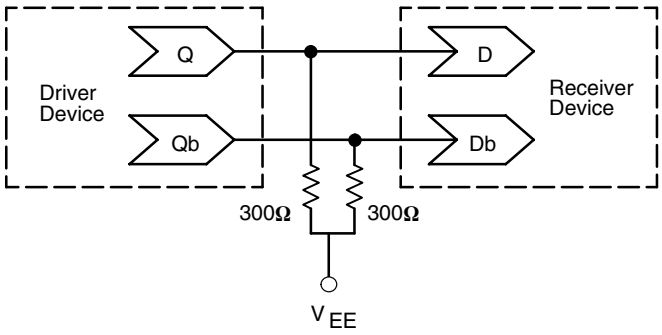


Figure 1. Termination for Output Driver and Device Evaluation of This Device (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E416, MC100E416

5V ECL Quint Differential Line Receiver

The MC10E416/100E416 is a 5-bit differential line receiving device. The 2.0 GHz of bandwidth provided by the high frequency outputs makes the device ideal for buffering of very high speed oscillators.

The design incorporates two stages of gain, internal to the device, making it an excellent choice for use in high bandwidth amplifier applications.

The differential inputs have internal clamp structures which will force the Q output of a gate in an open input condition to go to a LOW state. Thus, inputs of unused gates can be left open and will not affect the operation of the rest of the device. Note that the input clamp will take affect only if both inputs fall 2.5 V below V_{CC}.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

- Differential D and Q; V_{BB} available
- 600 ps Max. Propagation Delay
- High Frequency Outputs
- 2 Stages of Gain
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 200 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 201 devices

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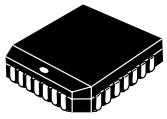
MARKING DIAGRAMS



PLCC–28
FN SUFFIX
CASE 776

28 1

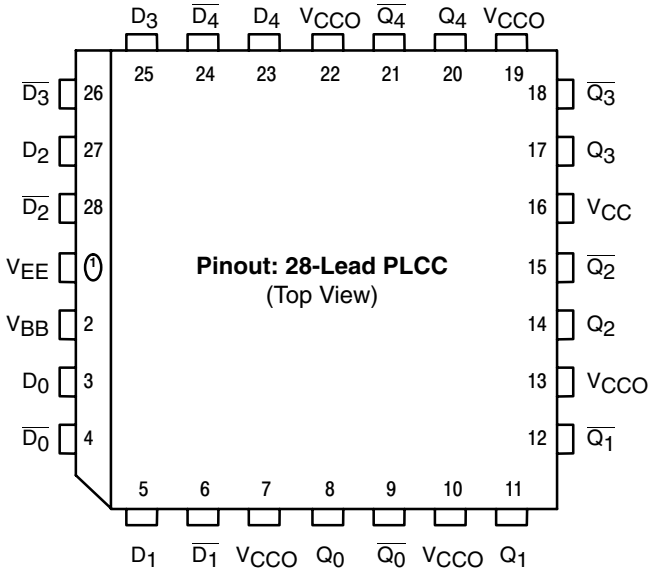
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

28 1

ORDERING INFORMATION

Device	Package	Shipping
MC10E416FN	PLCC–28	37 Units/Rail
MC10E416FNR2	PLCC–28	500 Units/Reel
MC100E416FN	PLCC–28	37 Units/Rail
MC100E416FNR2	PLCC–28	500 Units/Reel

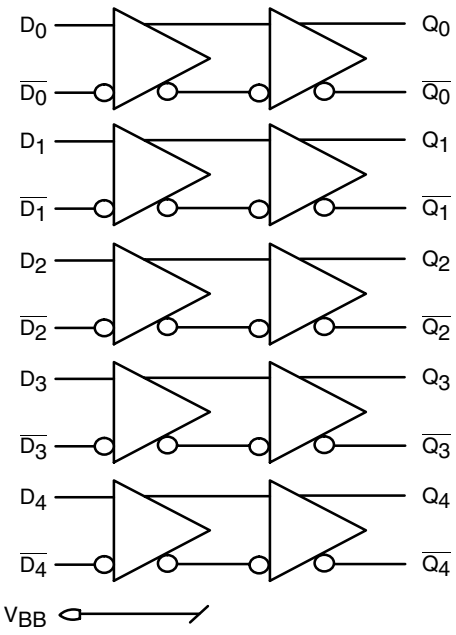
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN	FUNCTION
D[0:4], $\overline{D}$[0:4]	ECL Differential Data Inputs
Q[0:4], $\overline{Q}$[0:4]	ECL Differential Data Outputs
V_{BB}	Reference Voltage Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		135	162		135	162		135	162	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage (Single Ended)	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
V_{BB}	Output Voltage Reference	3.62		3.73	3.65		3.75	3.69		3.81	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.7		5.0	2.7		5.0	2.7		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		135	162		135	162		135	162	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
V_{BB}	Output Voltage Reference	–1.38		–1.27	–1.35		–1.25	–1.31		–1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.3		0.0	–2.3		0.0	–2.3		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		135	162		135	162		155	186	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.7		5.0	2.7		5.0	2.7		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		135	162		135	162		155	186	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.3		0.0	–2.3		0.0	–2.3		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{MAX}	Maximum Toggle Frequency		TBD			> 2.0			TBD		GHz
t_{PLH}	Propagation Delay to Output										ps
t_{PHL}	d(Diff)	250	350	500	250	350	500	250	350	500	
	D(SE)	200	350	550	200	350	550	200	350	550	
t_{SKEW}	Within-Device Skew (Note 2.)		50			50			50		ps
t_{SKEW}	Duty Cycle Skew										
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
	t_{PLH}-t_{PHL} (Note 3.)		±10			±10			±10		ps
$V_{PP(AC)}$	Minimum Input Swing (Note 4.)	150		1000	150		1000	150		1000	mV
t_r	Rise/Fall Time										
t_f	(20 - 80%)	100	200	350	100	200	350	100	200	350	ps

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.
3. Duty cycle skew defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.
4. Minimum input swing for which AC parameters are guaranteed.

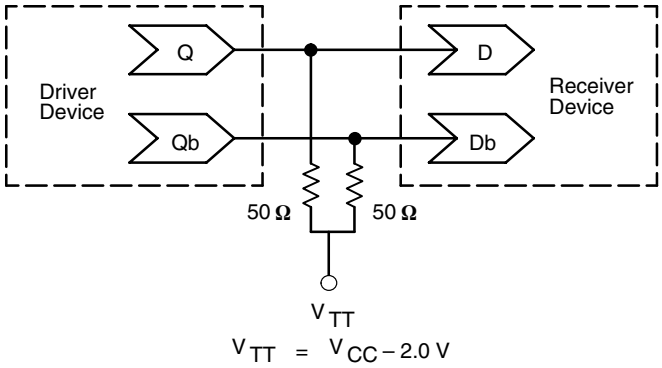


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E431, MC100E431

5V ECL 3-Bit Differential Flip-Flop

The MC10E/100E431 is a 3-bit flip-flop with differential clock, data input and data output.

The asynchronous Set and Reset controls are edge-triggered rather than level controlled. This allows the user to rapidly set or reset the flip-flop and then continue clocking at the next clock edge, without the necessity of de-asserting the set/reset signal (as would be the case with a level controlled set/reset).

The E431 is also designed with larger internal swings, an approach intended to minimize the time spent crossing the threshold region and thus reduce the metastability susceptibility window.

The differential input structures are clamped so that the inputs of unused registers can be left open without upsetting the bias network of the device. The clamping action will assert the $\overline{D}$ and the $\overline{CLK}$ sides of the inputs. Because of the edge triggered flip-flop nature of the device simultaneously opening both the clock and data inputs will result in an output which reaches an unidentified but valid state. Note that the input clamps only operate when both inputs fall to 2.5 V below V_{CC}.

The 100 Series contains temperature compensation.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- Edge-Triggered Asynchronous Set and Reset
- Differential D, CLK and Q; V_{BB} Reference Available
- 1100MHz Min. Toggle Frequency
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 1 KV HBM, > 75 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 348 devices

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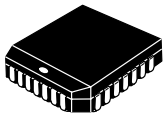
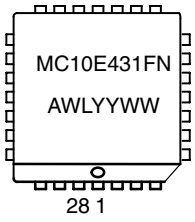
MARKING DIAGRAMS



PLCC–28
FN SUFFIX
CASE 776



28 1

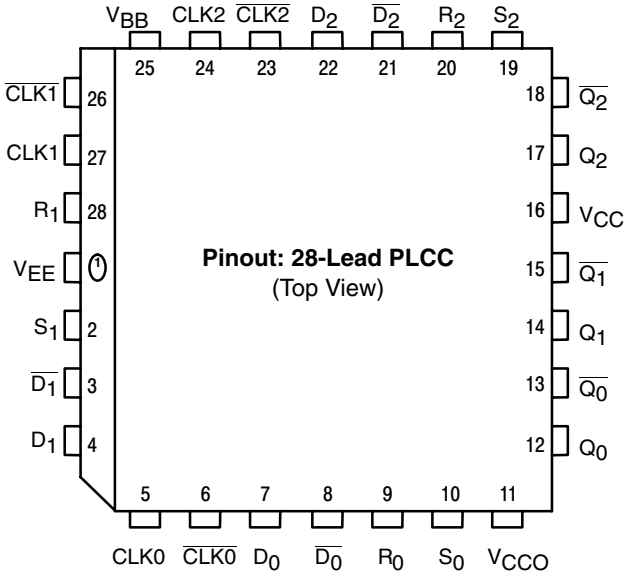
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

28 1

ORDERING INFORMATION

Device	Package	Shipping
MC10E431FN	PLCC–28	37 Units/Rail
MC10E431FNR2	PLCC–28	500 Units/Reel
MC100E431FN	PLCC–28	37 Units/Rail
MC100E431FNR2	PLCC–28	500 Units/Reel

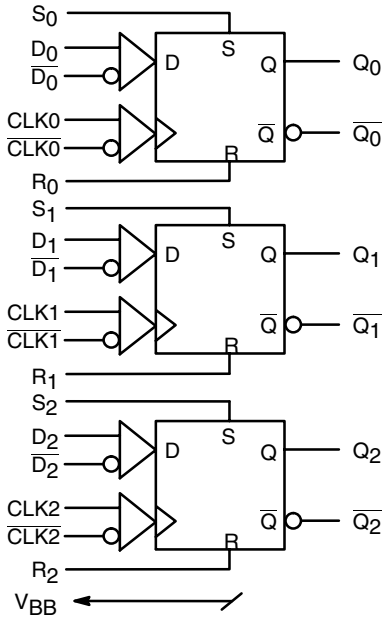
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN	FUNCTION
D[0:2], $\overline{D}$[0:2]	ECL Differential Data Inputs
CLK[0:2], $\overline{CLK}$[0:2]	ECL Differential Clock
S[0:2]	ECL Edge Triggered Set Inputs
R[0:2]	ECL Edge Triggered Reset Input
Q[0:2], $\overline{Q}$[0:2]	ECL Differential Data Outputs
V_{BB}	Reference Voltage Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply

FUNCTION TABLE

Dn	CLKn	Rn	Sn	Qn
L	Z	L	L	L
H	Z	L	L	H
X	X	Z	L	L
X	X	L	Z	H

Z = Low to high transition
X = Don't Care

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		110	132		110	132		110	132	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage (Single Ended)	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
V_{BB}	Output Voltage Reference	3.62		3.63	3.65		3.75	3.69		3.81	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.7		5.0	2.7		5.0	2.7		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		110	132		110	132		110	132	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
V_{BB}	Output Voltage Reference	–1.38		–1.37	–1.35		–1.25	–1.31		–1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.3		0.0	–2.3		0.0	–2.3		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		110	132		110	132		127	152	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.7		5.0	2.7		5.0	2.7		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		110	132		110	132		127	152	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.3		0.0	–2.3		0.0	–2.3		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency		TBD			1.1			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK (Diff) CLK (SE) R S	410 460 500 500	600 600 725 725	790 840 975 975	450 400 550 550	600 600 725 725	750 800 925 925	450 400 550 550	600 600 725 725	750 800 925 925	ps
t_S	Setup Time D R (Note 2.) S (Note 2.)	250 1100 1100	0 700 700		200 1000 1000	0 700 700		200 1000 1000	0 700 700		ps
t_H	Hold Time D	250	0		200	0		200	0		ps
t_{PW}	Minimum Pulse Width CLK	400			400			400			ps
t_{skew}	Within-Device Skew (Note 3.)		50						50		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Minimum Input Swing (Note 4.)	150		1000				150		1000	mV
t_r/t_f	Rise/Fall Times (20–80%)	250	450	700				275	450	650	ps

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. These setup times define the minimum time the CLK or SET/RESET input must wait after the assertion of the RESET/SET input to assure the proper operation of the flip-flop.
3. Within-device skew is defined as identical transitions on similar paths through a device.
4. Minimum input swing for which AC parameters are guaranteed.

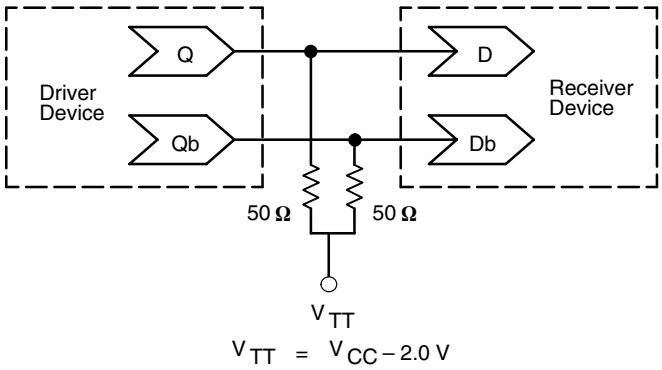


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E445, MC100E445

5V ECL 4-Bit Serial/Parallel Converter

The MC10/100E445 is an integrated 4-bit serial to parallel data converter. The device is designed to operate for NRZ data rates of up to 2.0 Gb/s. The chip generates a divide by 4 and a divide by 8 clock for both 4-bit conversion and a two chip 8-bit conversion function. The conversion sequence was chosen to convert the first serial bit to Q0, the second to Q1 etc.

Two selectable serial inputs provide a loopback capability for testing purposes when the device is used in conjunction with the E446 parallel to serial converter.

The start bit for conversion can be moved using the SYNC input. A single pulse applied asynchronously for at least two input clock cycles shifts the start bit for conversion from Qn to Qn–1. For each additional shift required an additional pulse must be applied to the SYNC input. Asserting the SYNC input will force the internal clock dividers to "swallow" a clock pulse, effectively shifting a bit from the Qn to the Qn–1 output (see Timing Diagram B).

The MODE input is used to select the conversion mode of the device. With the MODE input LOW, or open, the device will function as a 4-bit converter. When the mode input is driven HIGH the data on the output will change on every eighth clock cycle thus allowing for an 8-bit conversion scheme using two E445's. When cascaded in an 8-bit conversion scheme the devices will not operate at the 2.0 Gb/s data rate of a single device. Refer to the applications section of this data sheet for more information on cascading the E445.

Upon power-up the internal flip-flops will attain a random state. To synchronize multiple E445's in a system the master reset must be asserted.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

- On-Chip Clock ÷4 and ÷8
- 2.0 Gb/s Data Rate Capability
- Differential Clock and Serial Inputs
- V_{BB} Output for Single-Ended Input Applications
- Asynchronous Data Synchronization
- Mode Select to Expand to 8-Bits
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 100 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8",
  Oxygen Index 28 to 34
- Transistor Count = 528 devices

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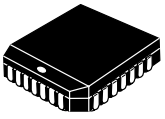
MARKING DIAGRAMS



PLCC–28
FN SUFFIX
CASE 776

28 1

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

28 1

ORDERING INFORMATION

Device	Package	Shipping
MC10E445FN	PLCC–28	37 Units/Rail
MC10E445FNR2	PLCC–28	500 Units/Reel
MC100E445FN	PLCC–28	37 Units/Rail
MC100E445FNR2	PLCC–28	500 Units/Reel

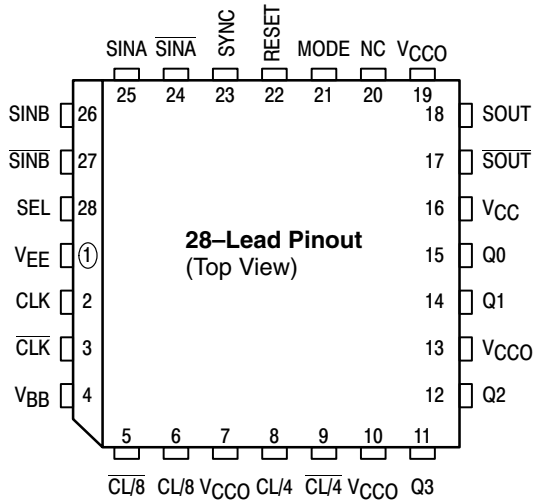
PIN DESCRIPTION

PIN	FUNCTION
SINA, $\overline{SINA}$	ECL Differential Serial Data Input A
SINB, $\overline{SINB}$	ECL Differential Serial Data Input B
SEL	ECL Serial Input Selector Pin
Q0–Q3	ECL Parallel Data Outputs
CLK, $\overline{CLK}$	ECL Differential Clock Inputs
CL/4, $\overline{CL/4}$	ECL Differential ÷4 Clock Output
CL/8, $\overline{CL/8}$	ECL Differential ÷8 Clock Output
MODE	ECL Conversion Mode 4-Bit/8-Bit
SYNCH	ECL Conversion Synchronizing Input
V_{BB}	Reference Voltage Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

FUNCTION TABLES

Mode	Conversion	SEL	Serial Input
L	4-Bit	H	A
H	8-Bit	L	B

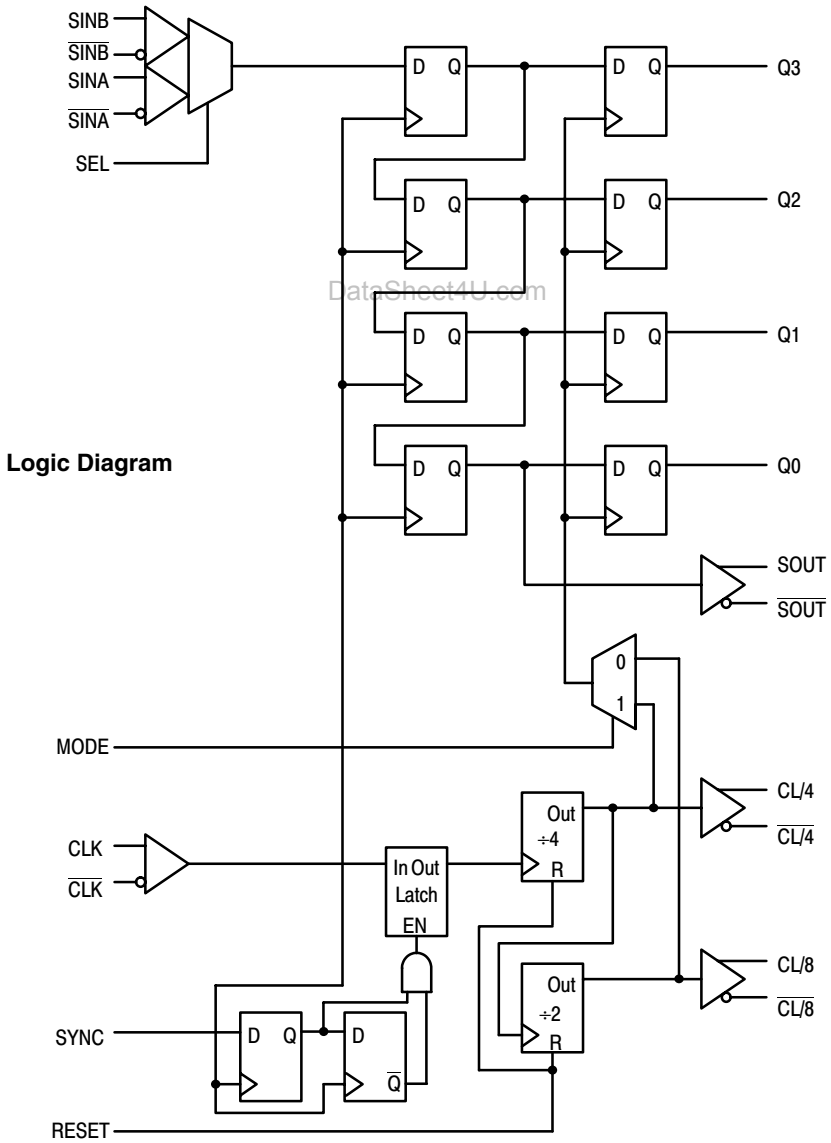
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Logic Diagram



MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		154	185		154	185		154	185	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
VOH_{sout}	Output HIGH Voltage sout/$\overline{sout}$	3975		4170	3975		4170	3975		4170	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage (Single Ended)	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
V_{BB}	Output Voltage Reference	3.62		3.63	3.65		3.75	3.69		3.81	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.2		4.6	2.2		4.6	2.2		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		154	185		154	185		154	185	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
VOH_{sout}	Output HIGH Voltage sout/$\overline{sout}$	–1025		–830	–1025		–830	–1025		–830	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
V_{BB}	Output Voltage Reference	–1.38		–1.37	–1.35		–1.25	–1.31		–1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.8		–0.4	–2.8		–0.4	–2.8		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		154	185		154	185		177	212	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
VOH_{sout}	Output HIGH Voltage sout/$\overline{sout}$	3975		4170	3975		4170	3975		4170	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.2		4.6	2.2		4.6	2.2		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C5			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		154	185		154	185		177	212	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
VOH_{sout}	Output HIGH Voltage sout/$\overline{sout}$	–1025		–830	–1025		–830	–1025		–830	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.8		–0.4	–2.8		–0.4	–2.8		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Conversion Frequency	2.0			2.0			2.0			Gb/s NRZ
t_{PLH} t_{PHL}	Propagation Delay to Output										ps
	CLK to Q, Reset to Q	1500	1800	2100	1500	1800	2100	1500	1800	2100	
	CLK to SOUT (Diff)	800	975	1150	800	975	1150	800	975	1150	
	CLK to CL/4(Diff)	1100	1325	1550	1100	1325	1550	1100	1325	1550	
	CLK to CL/8(Diff)	1100	1325	1550	1100	1325	1550	1100	1325	1550	
t_s	Setup Time										ps
	SINA, SINB	–100	–250		–100	–250		–100	–250		
	SEL	0	–200		0	–200		0	–200		
t_h	Hold Time										ps
	SINA, SINB, SEL	450	300		450	300		450	300		
t_{RR}	Reset Recovery Time	500	300		500	300		500	300		ps
t_{PW}	Minimum Pulse Width										ps
	CLK, MR	400			400			400			
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Rise/Fall Times 20%–80%										ps
	SOUT	100	225	350	100	225	350	100	225	350	
	Other	200	425	650	200	425	650	200	425	650	

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.

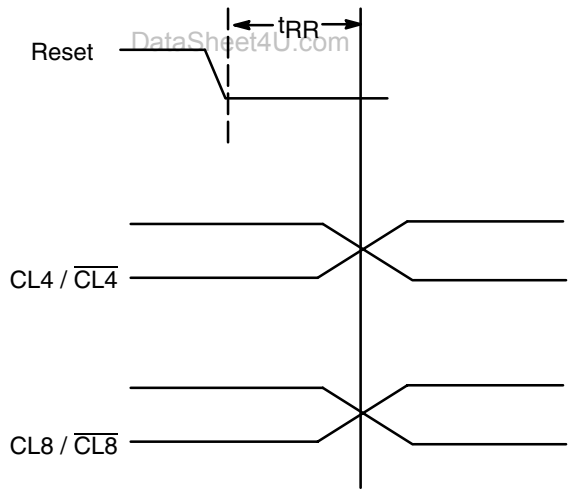
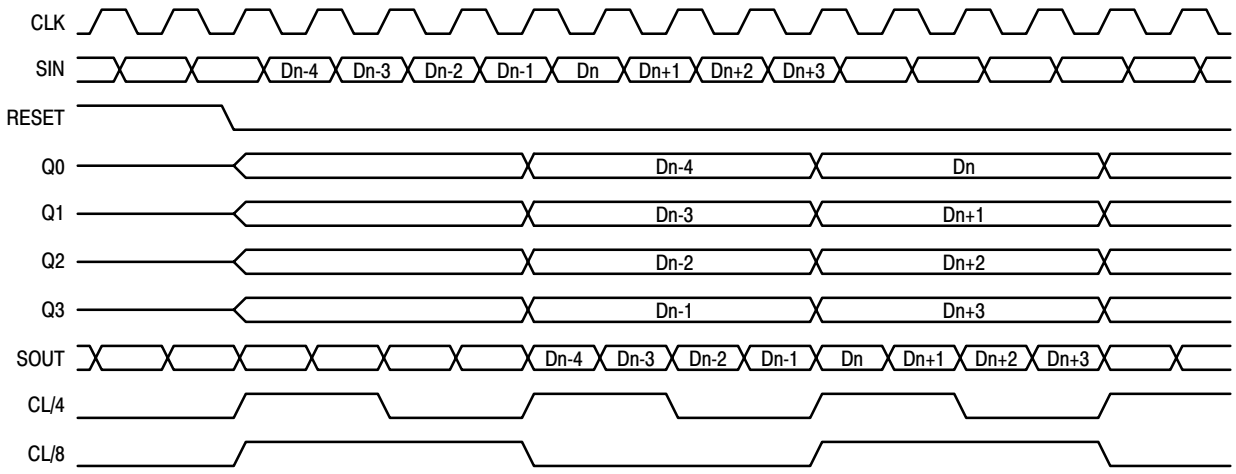
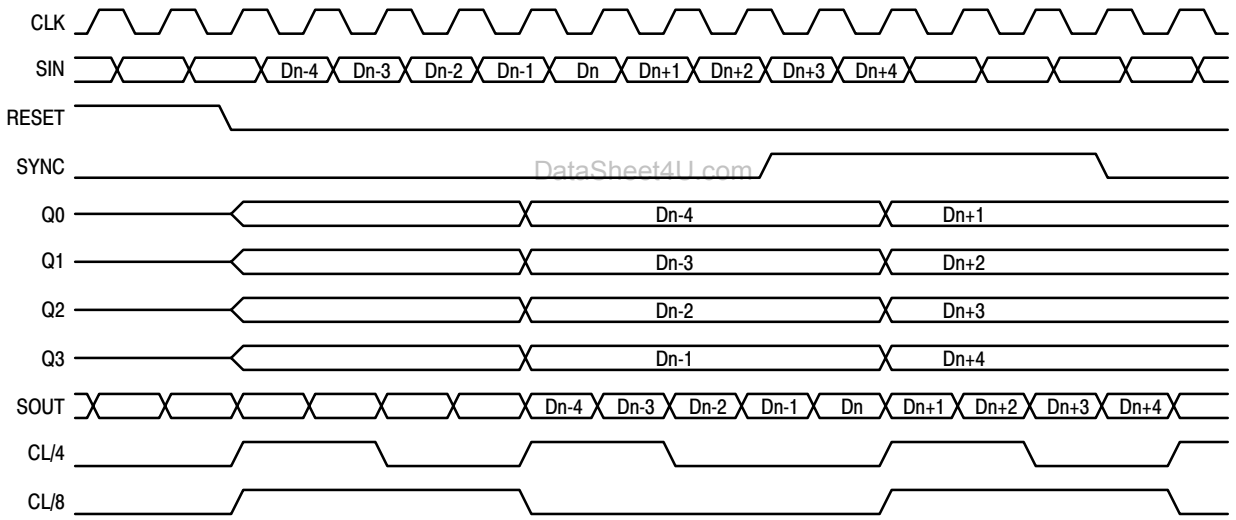


Figure 2.



Timing Diagram A. 1:4 Serial to Parallel Conversion



Timing Diagram B. 1:4 Serial to Parallel Conversion With SYNC Pulse

Figure 3. Timing Diagrams

APPLICATIONS INFORMATION

The MC10E/100E445 is an integrated 1:4 serial to parallel converter. The chip is designed to work with the E446 device to provide both transmission and receiving of a high speed serial data path. The E445, can convert up to a 2.0Gb/s NRZ data stream into 4-bit parallel data. The device also provides a divide by four clock output to be used to synchronize the parallel data with the rest of the system.

The E445 features multiplexed dual serial inputs to provide test loop capability when used in conjunction with the E446. Figure 4 illustrates the loop test architecture. The architecture allows for the electrical testing of the link without requiring actual transmission over the serial data path medium. The SINA serial input of the E445 has an extra buffer delay and thus should be used as the loop back serial input.

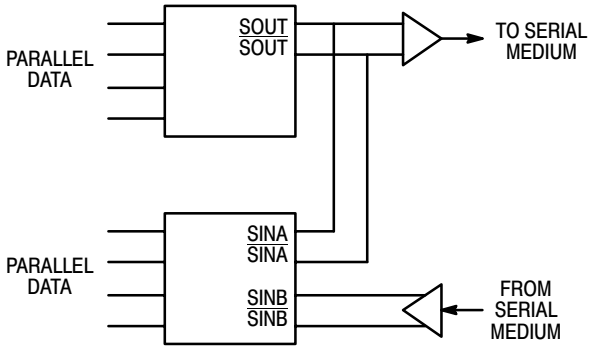
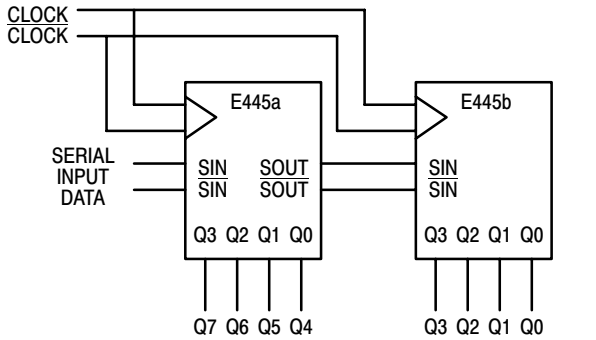


Figure 4. Loopback Test Architecture

The E445 features a differential serial output and a divide by 8 clock output to facilitate the cascading of two devices to build a 1:8 demultiplexer. Figure 5 illustrates the architecture for a 1:8 demultiplexer using two E445's; the timing diagram for this configuration can be found on the following page. Notice the serial outputs (SOUT) of the lower order converter feed the serial inputs of the the higher order device. This feed through of the serial inputs bounds the upper end of the frequency of operation. The clock to serial output propagation delay plus the setup time of the serial input pins must fit into a single clock period for the cascade architecture to function properly. Using the worst case values for these two parameters from the data sheet, TPD CLK to SOUT = 1150ps and tS for SIN = –100ps, yields a minimum period of 1050ps or a clock frequency of 950MHz.

The clock frequency is significantly lower than that of a single converter, to increase this frequency some games can be played with the clock input of the higher order E445. By delaying the clock feeding the second E445 relative to the clock of the first E445 the frequency of operation can be increased. The delay between the two clocks can be increased until the minimum delay of clock to serial out would potentially cause a serial bit to be swallowed (Figure 6).



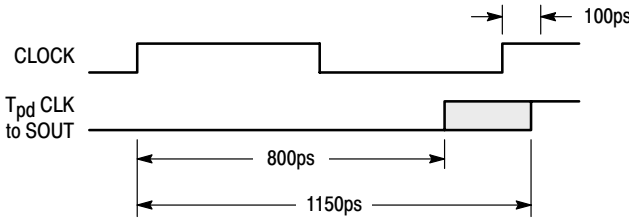


Figure 5. Cascaded 1:8 Converter Architecture

With a minimum delay of 800ps on this output the clock for the lower order E445 cannot be delayed more than 800ps relative to the clock of the first E445 without potentially missing a bit of information. Because the setup time on the serial input pin is negative coincident excursions on the data and clock inputs of the E445 will result in correct operation.

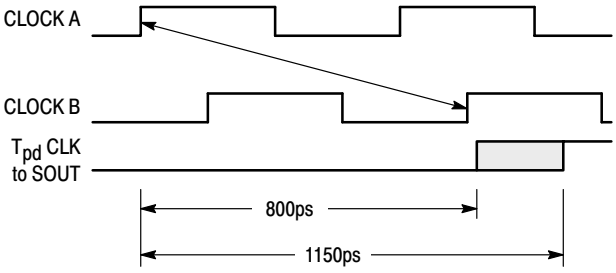


Figure 6. Cascade Frequency Limitation

Perhaps the easiest way to delay the second clock relative to the first is to take advantage of the differential clock inputs of the E445. By connecting the clock for the second E445 to the complimentary clock input pin the device will clock a half a clock period after the first E445 (Figure 7). Utilizing this simple technique will raise the potential conversion frequency up to 1.4GHz. The divide by eight clock of the second E445 should be used to synchronize the parallel data to the rest of the system as the parallel data of the two E445's will no longer be synchronized. This skew problem between the outputs can be worked around as the parallel information will be static for eight more clock pulses.

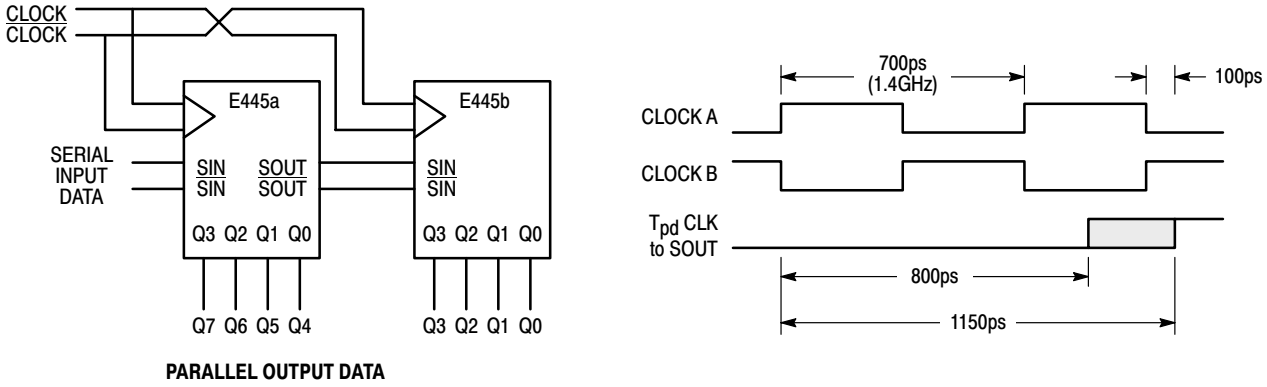


Figure 7. Extended Frequency 1:8 Demultiplexer

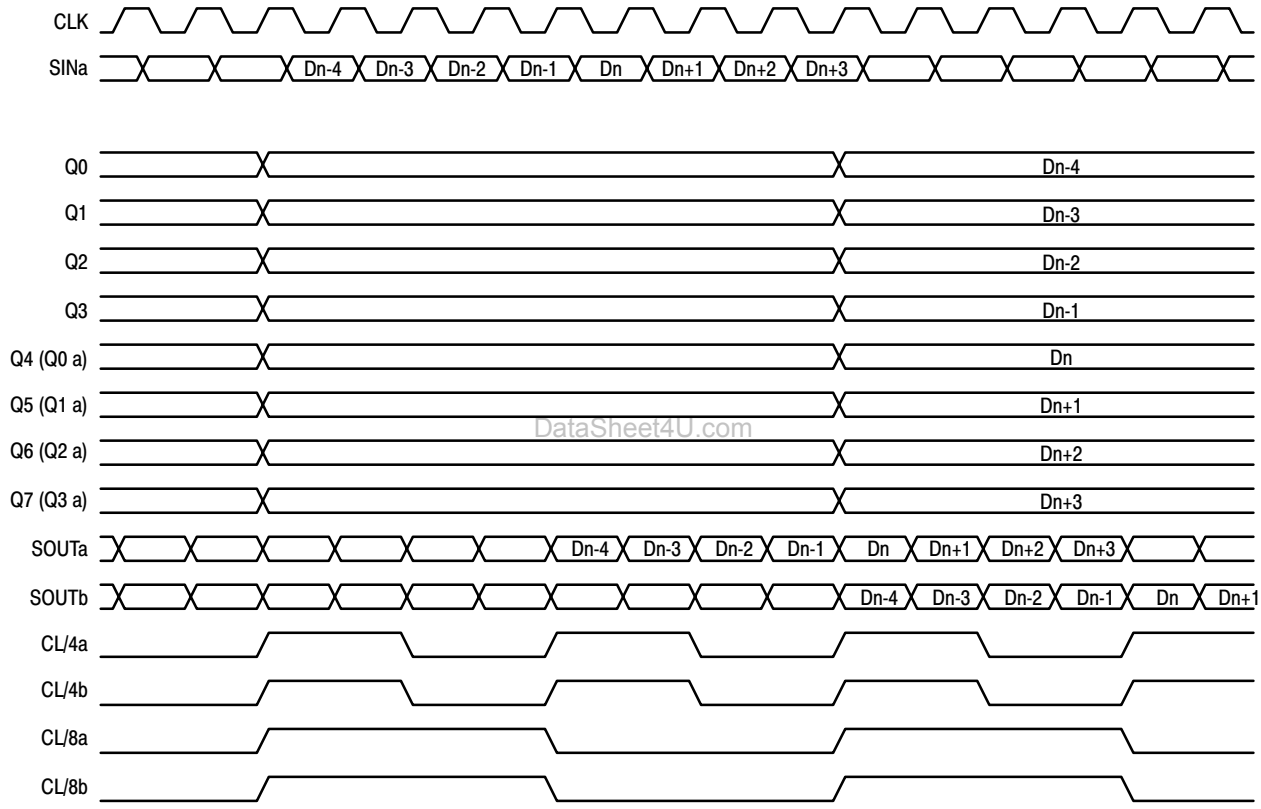


Figure 8. Timing Diagram A. 1:8 Serial to Parallel Conversion

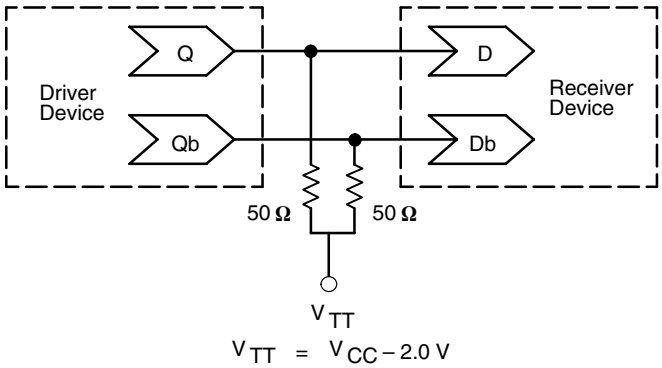


Figure 9. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E446, MC100E446

5V ECL 4-Bit Parallel/Serial Converter

The MC10E/100E446 is an integrated 4-bit parallel to serial data converter. The device is designed to operate for NRZ data rates of up to 1.3 Gb/s. The chip generates a divide by 4 and a divide by 8 clock for both 4-bit conversion and a two chip 8-bit conversion function. The conversion sequence was chosen to convert the parallel data into a serial stream from bit D0 to D3. A serial input is provided to cascade two E446 devices for 8 bit conversion applications. Note that the serial output data clocks off of the negative input clock transition.

The SYNC input will asynchronously reset the internal clock circuitry. This pin allows the user to reset the internal clock conversion unit and thus select the start of the conversion process.

The MODE input is used to select the conversion mode of the device. With the MODE input LOW, or open, the device will function as a 4-bit converter. When the mode input is driven HIGH the internal load clock will change on every eighth clock cycle thus allowing for an 8-bit conversion scheme using two E446's. When cascaded in an 8-bit conversion scheme the devices will not operate at the 1.3 Gb/s data rate of a single device. Refer to the applications section of this data sheet for more information on cascading the E446.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

- On Chip Clock ÷4 and ÷8
- 1.5 Gb/s Typical Data Rate Capability
- Differential Clock and Serial Inputs
- V_{BB} Output for Single-ended Input Applications
- Asynchronous Data Synchronization
- Mode Select to Expand to 8 Bits
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 100 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8",
  Oxygen Index 28 to 34
- Transistor Count = 525 devices

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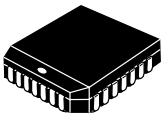
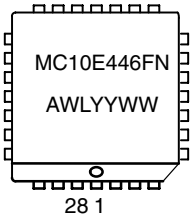
MARKING DIAGRAMS



PLCC–28
FN SUFFIX
CASE 776

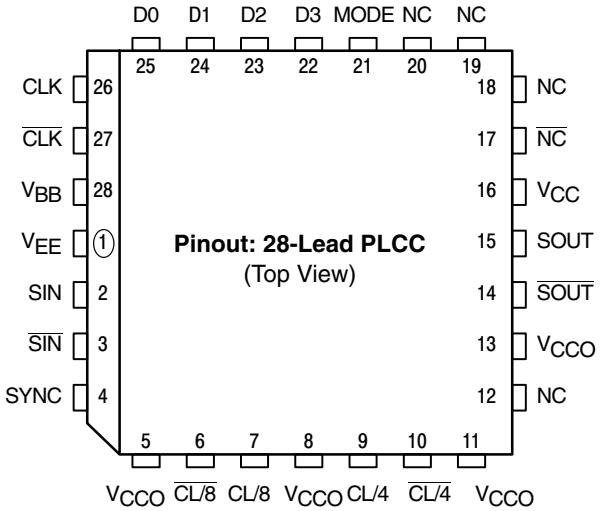


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E446FN	PLCC–28	37 Units/Rail
MC10E446FNR2	PLCC–28	500 Units/Reel
MC100E446FN	PLCC–28	37 Units/Rail
MC100E446FNR2	PLCC–28	500 Units/Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

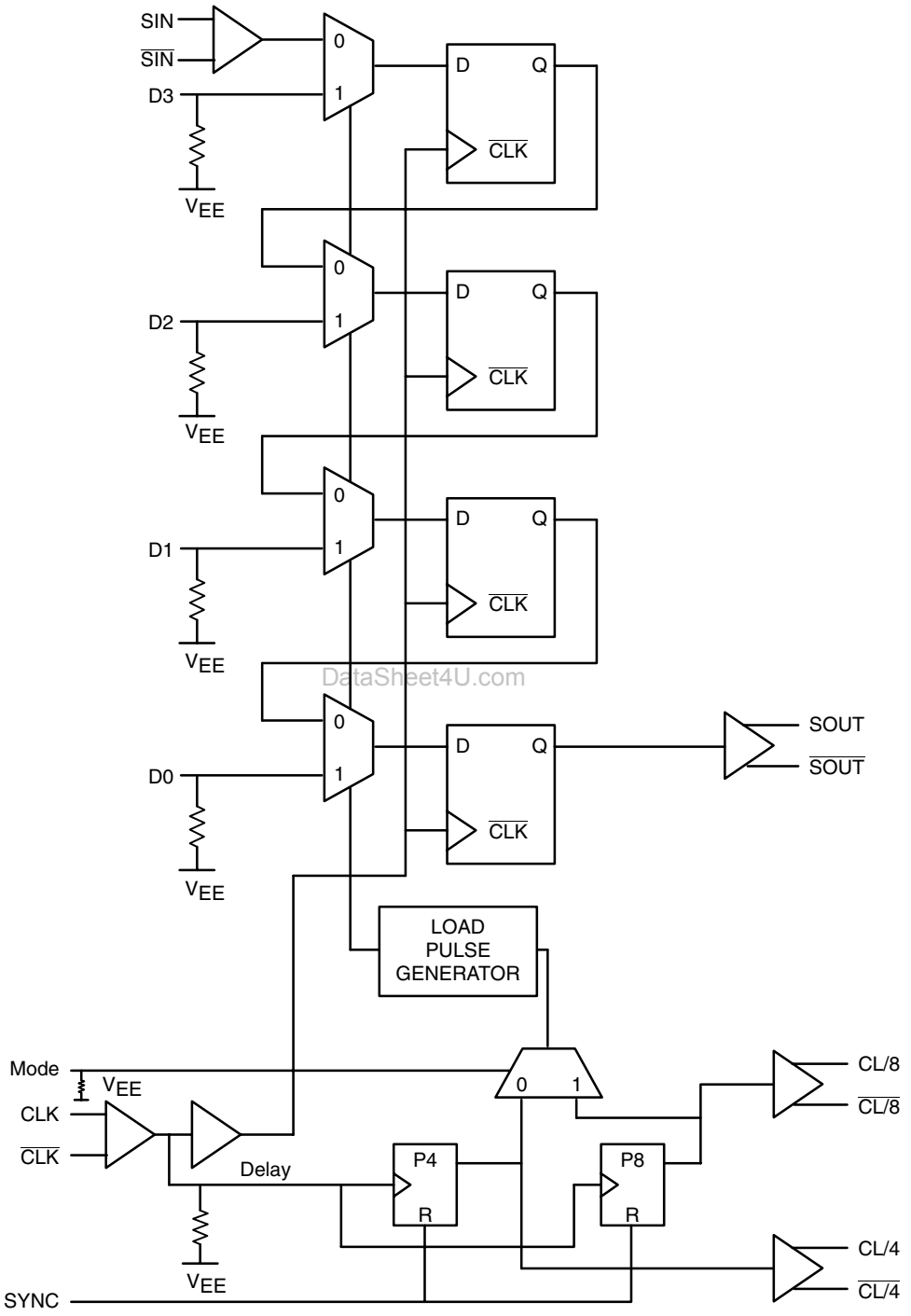
PIN DESCRIPTION

PIN	FUNCTION
SIN	ECL Differential Serial Data Input
D0 – D3	ECL Parallel Data Inputs
SOUT, $\overline{SOUT}$	ECL Differential Serial Data Output
CLK, $\overline{CLK}$	ECL Differential Clock Inputs
CL/4, $\overline{CL/4}$	ECL Differential ÷4 Clock Output
CL/8, $\overline{CL/8}$	ECL Differential ÷8 Clock Output
MODE	Conversion Mode 4-Bit/8-Bit
SYNC	ECL Conversion Synchronizing Input
V_{BB}	Reference Voltage Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

FUNCTION TABLES

Mode	Conversion
L	4-Bit
H	8-Bit

LOGIC DIAGRAM



MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		126	151		126	151		126	151	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
VOH_{sout}	Output HIGH Voltage sout/$\overline{sout}$	3975		4170	3975		4170	3975		4170	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
V_{BB}	Output Voltage Reference	3.62		3.63	3.65		3.75	3.69		3.81	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		126	151		126	151		126	151	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
VOH_{sout}	Output HIGH Voltage sout/$\overline{sout}$	–1025		–830	–1025		–830	–1025		–830	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
V_{BB}	Output Voltage Reference	–1.38		–1.37	–1.35		–1.25	–1.31		–1.19	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		126	151		126	151		145	174	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
VOH_{sout}	Output HIGH Voltage sout/$\overline{sout}$	3980		4210	4020		4240	4090		4330	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
V_{BB}	Output Voltage Reference	3.62		3.73	3.62		3.74	3.62		3.74	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		126	151		126	151		145	174	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
VOH_{sout}	Output HIGH Voltage sout/$\overline{sout}$	–1020		–790	–980		–760	–910		–670	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.27	–1.38		–1.26	–1.38		–1.26	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic		0°C Min	0°C Typ	0°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Typ	85°C Max	Unit
F_{MAX}	Max Conversion Frequency		1.3	1.6		1.3	1.6		1.3	1.6		Gb/s NRZ
t_{PLH} t_{PHL}	Propagation Delay to Output											ps
	CLK to SOUT (Note 2.)		1020	1200	1480	1020	1200	1480	1020	1200	1480	
	CLK to CL/4		650	850	1050	650	850	1050	650	850	1050	
	CLK to CL/8		800	1050	1300	800	1050	1300	800	1050	1300	
	SYNC to CL/4, CL/8		650	850	1100	650	850	1100	650	850	1100	
t_s	Setup Time (Note 3.)	SIN, Dn	-200	-450		-200	–450		–200	–450		ps
t_h	Hold Time (Note 3.)	SIN, Dn	900	650		900	650		900	650		ps
t_{RR}	Reset Recovery Time	SYNC	500	300		500	300		500	300		ps
t_{PW}	Min Pulse Width	CLK, MR	300			300			300			ps
t_{JITTER}	Cycle–to–Cycle Jitter			TBD			TBD			TBD		ps
t_r t_f	Rise/Fall Times (20% - 80%)	SOUT	100	225	350	100	225	350	100	225	350	ps
		Other	200	425	650	200	425	650	200	425	650	

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Propagation delays measured from negative going clock edge.
3. Relative to negative clock edge.

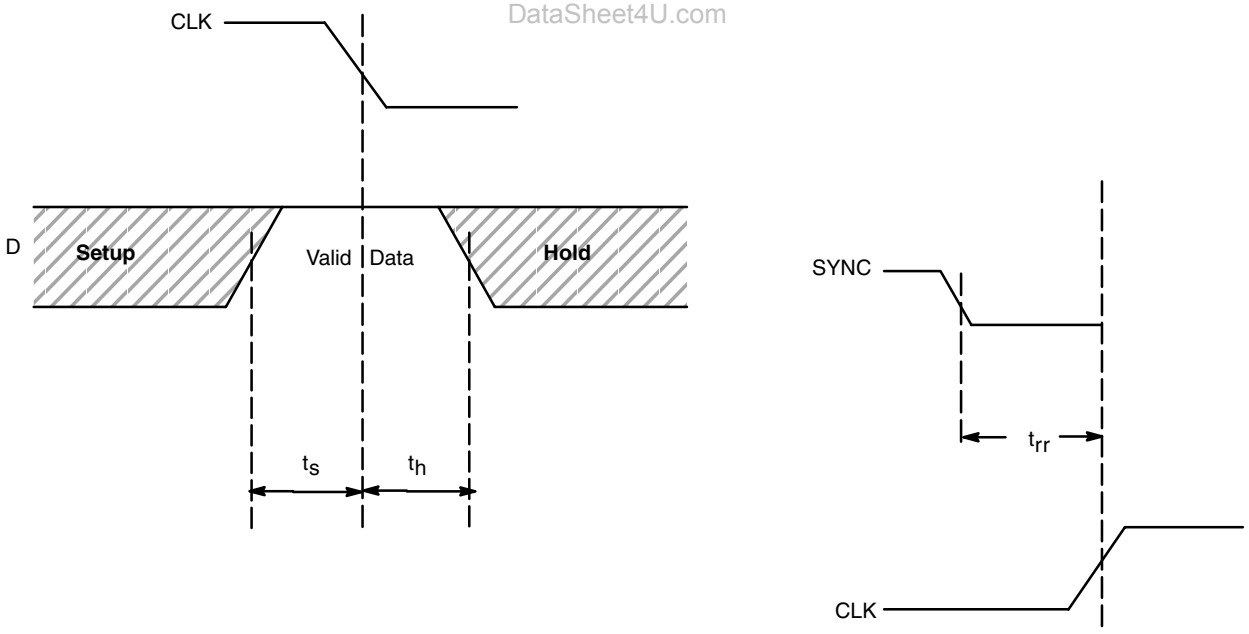
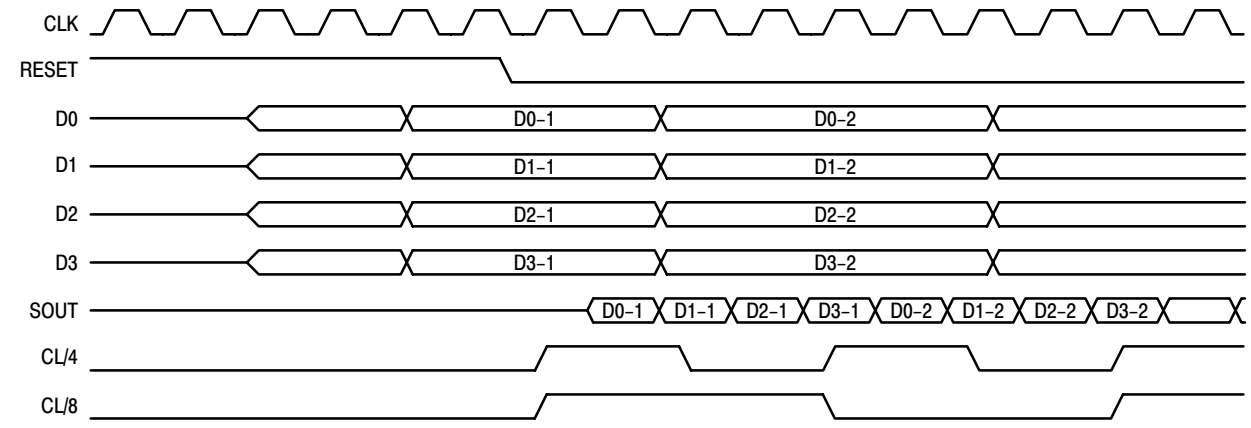
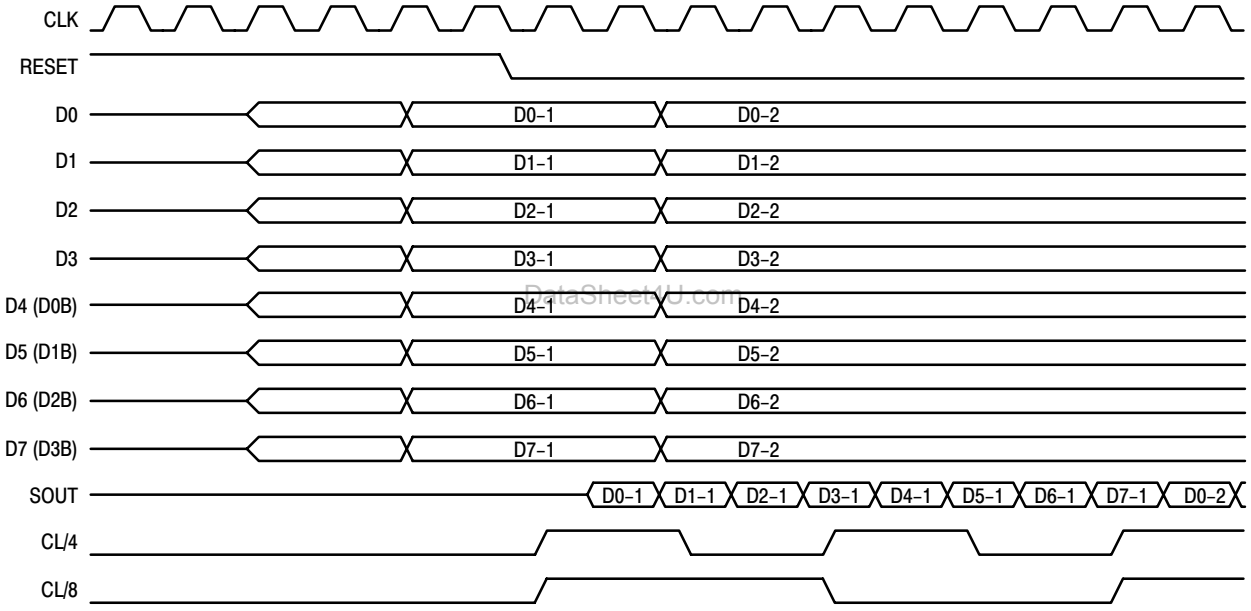


Figure 1.



Timing Diagram A. 4:1 Parallel to Serial Conversion



Timing Diagram B. 8:1 Parallel to Serial Conversion

Figure 2. Timing Diagrams

Applications Information

The MC10E/100E446 is an integrated 4:1 parallel to serial converter. The chip is designed to work with the E445 device to provide both transmission and receiving of a high speed serial data path. The E446 can convert 4 bits of data into a 1.3Gb/s NRZ data stream. The device features a SYNC input which allows the user to reset the internal clock circuitry and restart the conversion sequence (see timing diagram A).

The E446 features a differential serial input and internal divide by 8 circuitry to facilitate the cascading of two devices to build a 8:1 multiplexer. Figure 1 illustrates the architecture for a 8:1 multiplexer using two E446's; the timing diagram for this configuration can be found on the following page. Notice the serial outputs (SOUT) of the higher order converter feed the serial inputs of the the lower order device. This feed through of the serial inputs bounds the upper end of the frequency of operation. The clock to serial output propagation delay plus the setup time of the serial input pins must fit into a single clock period for the cascade architecture to function properly. Using the worst case values for these two parameters from the data sheet, TPD CLK to SOUT = 1480ps and tS for SIN = –200ps, yields a minimum period of 1280ps or a clock frequency of 780MHz.

The clock frequency is somewhat lower than that of a single converter, to increase this frequency some games can be played with the clock input of the higher order E446. By delaying the clock feeding E446A relative to the clock of E446B the frequency of operation can be increased.

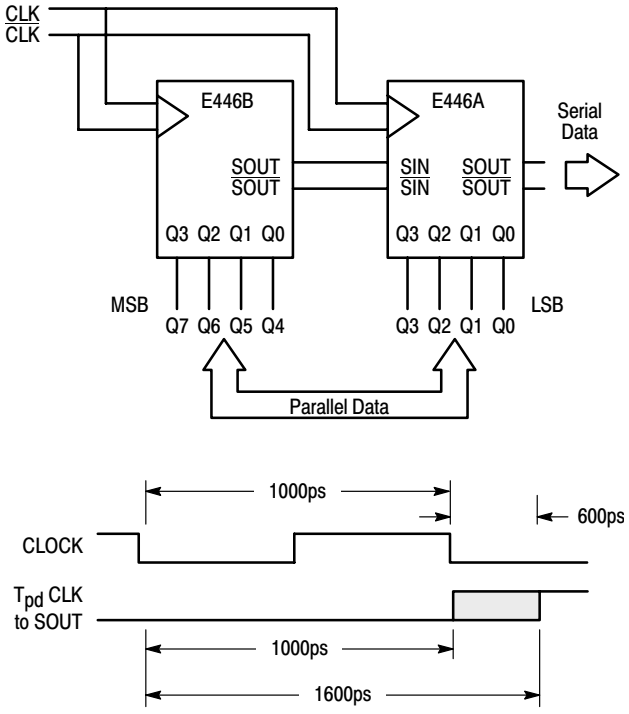


Figure 3. Cascaded 8:1 Converter Architecture

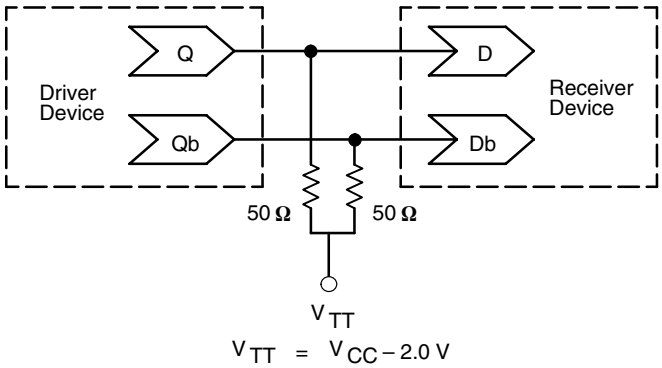


Figure 4. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E451, MC100E451

5V ECL 6-Bit D Register Differential Data and Clock

The MC10E/100E451 contains six D-type flip-flops with single-ended outputs and differential data inputs. The common clock input is also differential. The registers are triggered by a positive transition of the positive clock (CLK) input.

A HIGH on the Master Reset (MR) input resets all Q outputs to LOW.

The differential input structures are clamped so that the inputs of unused registers can be left open without upsetting the bias network of the device. The clamping action will assert the $\overline{D}$ and the $\overline{CLK}$ sides of the inputs. Because of the edge triggered flip-flop nature of the device simultaneously opening both the clock and data inputs will result in an output which reaches an unidentified but valid state. Note that the input clamps only operate when both inputs fall to 2.5 V below V_{CC}.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

- Differential Inputs: Data and Clock
- V_{BB} Output
- 1100 MHz Min. Toggle Frequency
- Asynchronous Master Reset
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 200 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 348 devices

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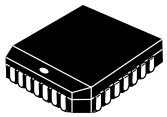
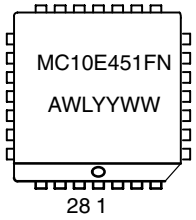


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAMS

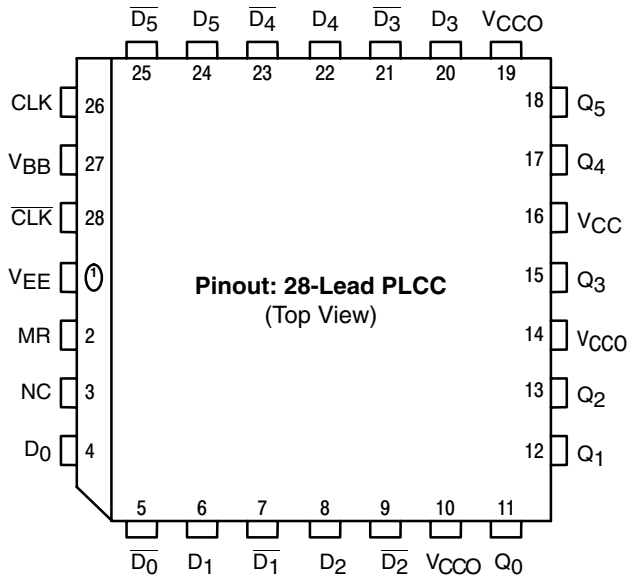


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E451FN	PLCC–28	37 Units/Rail
MC10E451FNR2	PLCC–28	500 Units/Reel
MC100E451FN	PLCC–28	37 Units/Rail
MC100E451FNR2	PLCC–28	500 Units/Reel

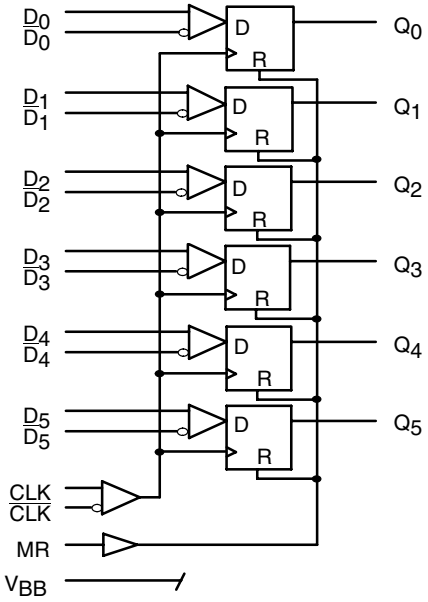
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN	FUNCTION
$D_0 - D_5$, $\overline{D_0} - \overline{D_5}$	ECL Differential Data Input
CLK, $\overline{CLK}$	ECL Differential Clock Input
MR	ECL Master Reset Input
$Q_0 - Q_5$	ECL Data Outputs
V_{BB}	Reference Voltage Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		84	101		84	101		84	101	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage (Single Ended)	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
V_{BB}	Output Voltage Reference	3.62		3.63	3.65		3.75	3.69		3.81	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.2		4.6	2.2		4.6	2.2		4.6	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		84	101		84	101		84	101	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
V_{BB}	Output Voltage Reference	–1.38		–1.37	–1.35		–1.25	–1.31		–1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.8		–0.4	–2.8		–0.4	–2.8		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		84	101		84	101		97	116	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.2		4.6	2.2		4.6	2.2		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		84	101		84	101		97	116	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.8		–0.4	–2.8		–0.4	–2.8		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency		TBD			1.1			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output										ps
	CLK (Diff)	475	650	800	475	650	800	475	650	800	
	CLK (SE)	425	650	850	425	650	850	425	650	850	
	MR	425	600	850	425	600	850	425	600	850	
t_s	Setup Time D	150	–100		150	–100		150	–100		ps
t_h	Hold Time D	250	100		250	100		250	100		ps
t_{RR}	Reset Recovery Time	750	600		750	600		750	600		ps
t_{PW}	Minimum Pulse Width										ps
	CLK, MR	400			400			400			
t_{SKEW}	Within-Device Skew (Note 3.)		100			100			100		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}(AC)	Minimum Input Swing (Note 2.)	150		1000	150		1000	150		1000	mV
t_r t_f	Rise/Fall Times										ps
	(20 - 80%)	275	450	800	275	450	800	275	450	800	

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Minimum input voltage for which AC parameters are guaranteed.
3. Within-device skew is defined as identical transitions on similar paths through a device.

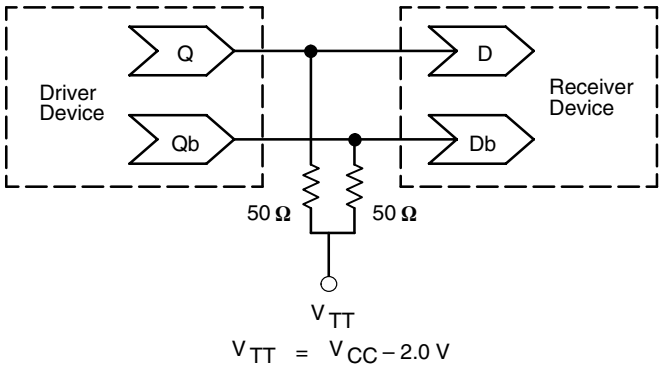


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E452, MC100E452

5V ECL 5-Bit Differential Register

The MC10E/100E452 is a 5-bit differential register with differential data (inputs and outputs) and clock. The registers are triggered by a positive transition of the positive clock (CLK) input. A high on the Master Reset (MR) asynchronously resets all registers so that the Q outputs go LOW.

The differential input structures are clamped so that the inputs of unused registers can be left open without upsetting the bias network of the device. The clamping action will assert the $\overline{D}$ and the $\overline{CLK}$ sides of the inputs. Because of the edge triggered flip-flop nature of the device simultaneously opening both the clock and data inputs will result in an output which reaches an unidentified but valid state. Note that the input clamps only operate when both inputs fall to 2.5 V below V_{CC}.

The fully differential design of the device makes it ideal for very high frequency applications where a registered data path is necessary.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

- Differential D, CLK and Q; V_{BB} Reference Available
- 1100 MHz Min. Toggle Frequency
- Asynchronous Master Reset
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors, Output $\overline{Q}_3$ will Default to Low State When Inputs Are Left Open
- ESD Protection: > 1 KV HBM, > 75 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 315 devices

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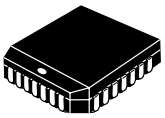
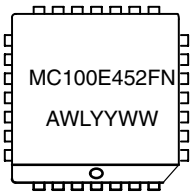


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAMS

28 1



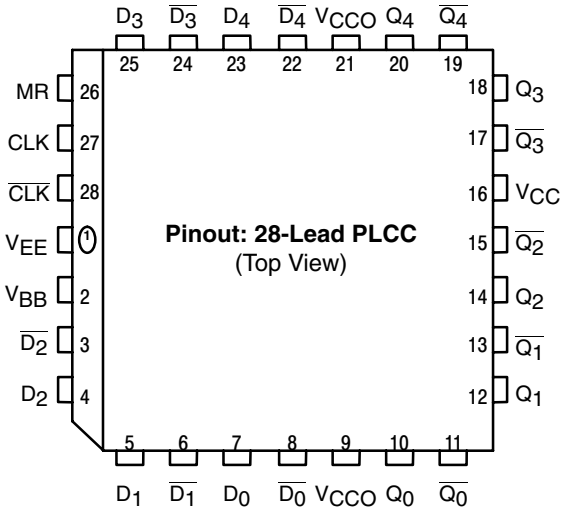
28 1

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E452FN	PLCC–28	37 Units/Rail
MC10E452FNR2	PLCC–28	500 Units/Reel
MC100E452FN	PLCC–28	37 Units/Rail
MC100E452FNR2	PLCC–28	500 Units/Reel

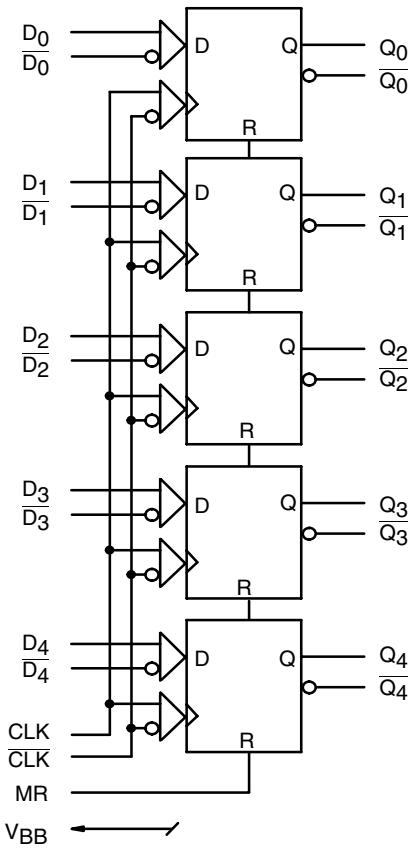
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN	FUNCTION
D[0:4], $\overline{D}$[0:4]	ECL Differential Data Inputs
MR	ECL Master Reset Input
CLK, $\overline{CLK}$	ECL Differential Clock Input
Q[0:4], $\overline{Q}$[0:4]	ECL Differential Data Outputs
V_{BB}	Reference Voltage Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		74	89		74	89		74	89	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage (Single Ended)	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
V_{BB}	Output Voltage Reference	3.62		3.63	3.65		3.75	3.69		3.81	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.2		4.6	2.2		4.6	2.2		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		74	89		74	89		74	89	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
V_{BB}	Output Voltage Reference	–1.38		–1.37	–1.35		–1.25	–1.31		–1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.8		–0.4	–2.8		–0.4	–2.8		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		74	89		74	89		85	102	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.2		4.6	2.2		4.6	2.2		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		74	89		74	89		85	102	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.8		–0.4	–2.8		–0.4	–2.8		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency		TBD			1.1			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK (Diff) CLK (SE) MR	425 375 375	600 600 625	850 900 900				475 425 425	600 600 625	800 850 850	ps
t_S	Setup Time D	175	–50					150	–50		ps
t_H	Hold Time D	225	50					200	50		ps
t_{RR}	Reset Recovery Time	750	450					700	450		
t_{PW}	Minimum Pulse Width CLK MR	400 400						400 400			ps
t_{skew}	Within-Device Skew (Note 2.)		50						50		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Minimum Input Swing (Note 3.)	150		1000	150		1000	150		1000	mV
t_r/t_f	Rise/Fall Times 20–80%	250	475	725				275	475	675	ps

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.
3. Minimum input swing for which AC parameters are guaranteed.

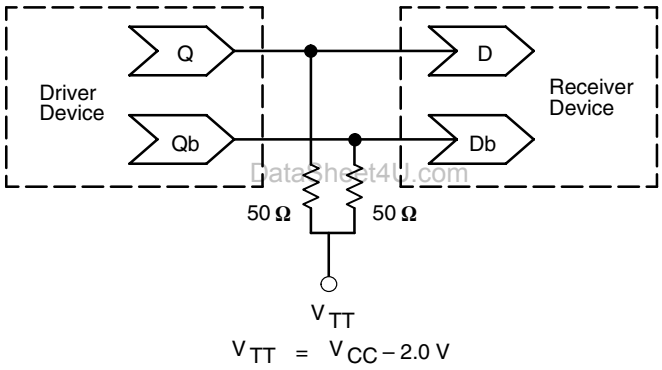


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels

AN1405 – ECL Clock Distribution Techniques

AN1406 – Designing with PECL (ECL at +5.0 V)

AN1503 – ECLinPS I/O SPICE Modeling Kit

AN1504 – Metastability and the ECLinPS Family

AN1568 – Interfacing Between LVDS and ECL

AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit

AN1650 – Using Wire–OR Ties in ECLinPS Designs

AN1672 – The ECL Translator Guide

AND8001 – Odd Number Counters Design

AND8002 – Marking and Date Codes

AND8020 – Termination of ECL Logic Devices

MC10E457, MC100E457

5V ECL Triple Differential 2:1 Multiplexer

The MC10E457/100E457 is a 3-bit differential 2:1 multiplexer. The fully differential data path makes the device ideal for multiplexing low skew clock or other skew sensitive signals.

The higher frequency outputs provide the device with a >1.0 GHz bandwidth to meet the needs of the most demanding system clock.

Both, separate selects and a common select, are provided to make the device well suited for both data path and random logic applications.

The differential inputs have internal clamp structures which will force the Q output of a gate in an open input condition to go to a LOW state. Thus, inputs of unused gates can be left open and will not affect the operation of the rest of the device. Note that the input clamp will take affect only if both inputs fall 2.5 V below V_{CC}.

The 100 Series contains temperature compensation.

Multiple V_{BB} pins are provided to ease AC coupling input signals. The V_{BB} pins, internally generated voltage supply pins, are available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- Differential D and Q; V_{BB} available
- 700 ps Max. Propagation Delay
- High Frequency Outputs
- Separate and Common Select
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 200 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 218 devices

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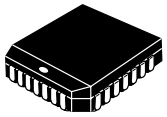
MARKING DIAGRAMS



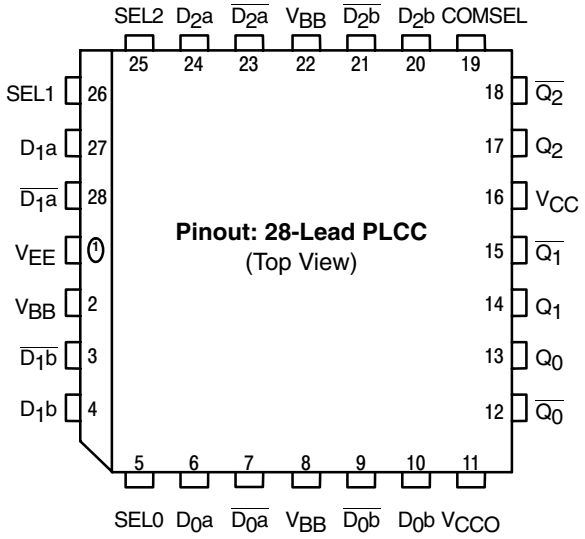
PLCC–28
FN SUFFIX
CASE 776

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E457FN	PLCC–28	37 Units/Rail
MC10E457FNR2	PLCC–28	500 Units/Reel
MC100E457FN	PLCC–28	37 Units/Rail
MC100E457FNR2	PLCC–28	500 Units/Reel

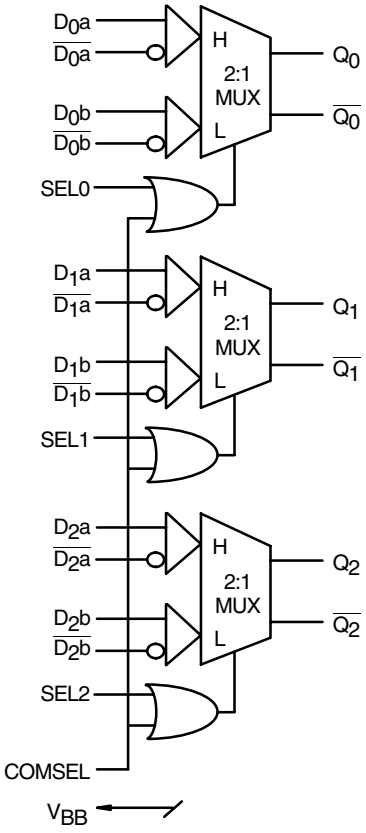
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN	FUNCTION
Dn[0:2]; $\overline{Dn}$[0:2]	ECL Differential Data Inputs
SEL	ECL Individual Select Input
COMSEL	ECL Common Select Input
Q[0:2], $\overline{Q}$[0:2]	ECL Differential Data Outputs
V_{BB}	Reference Voltage Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply

FUNCTION TABLE

SEL	Data
H	a
L	b

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		92	110		92	110		92	110	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3980	4070	4160	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3210	3370	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3830	3995	4160	3870	4030	4190	3940	4110	4280	mV
V_{IL}	Input LOW Voltage (Single Ended)	3050	3285	3520	3050	3285	3520	3050	3302	3555	mV
V_{BB}	Output Voltage Reference	3.62		3.73	3.65		3.75	3.69		3.81	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	2.7		5.0	2.7		5.0	2.7		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

10E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		92	110		92	110		92	110	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1020	–930	–840	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1790	–1630	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1170	–1005	–840	–1130	–970	–810	–1060	–890	–720	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1950	–1715	–1480	–1950	–1715	–1480	–1950	–1698	–1445	mV
V_{BB}	Output Voltage Reference	–1.38		–1.27	–1.35		–1.25	–1.31		–1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	–2.3		0.0	–2.3		0.0	–2.3		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.065		0.3	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.06 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES PECL DC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		92	110		92	110		106	127	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3975	4050	4120	3975	4050	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3190	3295	3380	3190	3255	3380	3190	3260	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	2.7		5.0	2.7		5.0	2.7		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES NECL DC CHARACTERISTICS V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		92	110		92	110		106	127	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1025	–950	–880	–1025	–950	–880	–1025	–950	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1745	–1620	–1810	–1740	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165	–950	–880	–1165	–880	–880	–1165	–880	–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810	–1700	–1475	–1810	–1475	–1475	–1810	–1475	–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.)	–2.3		0.0	–2.3		0.0	–2.3		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / –0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

AC CHARACTERISTICS V_{CCx}= 5.0 V; V_{EE}= 0.0 V or V_{CCx}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output										ps
	D (Differential)	325	475	700				375	475	650	
	D (Single-Ended)	275	475	750				325	475	700	
	SEL	300	500	775				350	500	725	
	COMSEL	325	525	800				375	525	750	
t_{skew}	Within-Device Skew (Note 2.)		40						40		ps
t_{skew}	Duty Cycle Skew (Note 3.) $t_{PLH} - t_{PHL}$		±10						±10		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}(AC)	Minimum Input Swing (Note 4.)	150						150			mV
t_r/t_f	Rise/Fall Time 20–80%	125	275	500				150	275	450	ps

1. 10 Series: V_{EE} can vary +0.46 V / –0.06 V.
   100 Series: V_{EE} can vary +0.46 V / –0.8 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.
3. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.
4. Minimum input swing for which AC parameters are guaranteed.

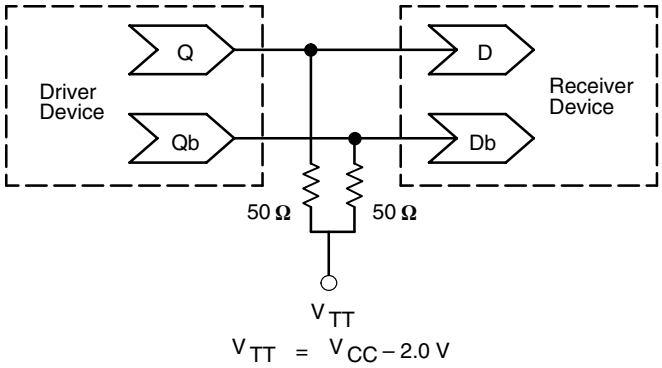


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E1651

5V, -5V ECL Dual ECL Output Comparator With Latch

The MC10E1651 is fabricated using ON Semiconductor's advanced MOSAIC III™ process. The MC10E1651 incorporates a fixed level of input hysteresis as well as output compatibility with 10 KH logic devices. In addition, a latch is available allowing a sample and hold function to be performed. The device is available in both a 16-pin DIP and a 20-pin surface mount package.

The latch enable ($\overline{LEN}_a$ and $\overline{LEN}_b$) input pins operate from standard ECL 10 KH logic levels. When the latch enable is at a logic high level, the MC10E1651 acts as a comparator; hence, Q will be at a logic high level if V1 > V2 (V1 is more positive than V2). $\overline{Q}$ is the complement of Q. When the latch enable input goes to a low logic level, the outputs are latched in their present state providing the latch enable setup and hold time constraints are met.

The 100 series contains temperature compensation.

- Typical 3.0 dB Bandwidth > 1.0 GHz
- Typical V to Q Propagation Delay of 775 ps
- Typical Output Rise/Fall of 350 ps
- Common Mode Range –2.0 V to +3.0 V
- Individual Latch Enables
- Differential Outputs
- 28mV Input Hysteresis
- Operating Mode: V_{CC}= 5.0 V, V_{EE}= –5.2 V
- No Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 100 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8",
  Oxygen Index 28 to 34
- Transistor Count = 85 devices

ON Semiconductor™

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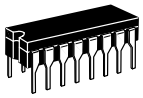
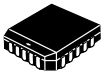
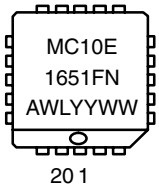
MARKING DIAGRAMS



CDIP–16
L SUFFIX
CASE 620



PLCC–20
FN SUFFIX
CASE 775



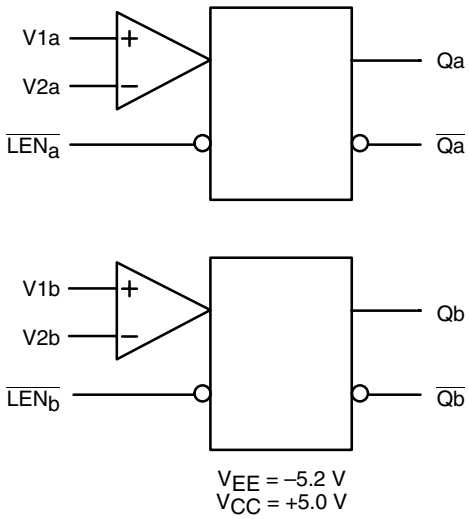
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E1651L	CDIP–16	25 Units/Rail
MC10E1651FN	PLCC–20	46 Units/Rail
MC10E1651FNR2	PLCC–20	500 Units/Reel

MC10E1651

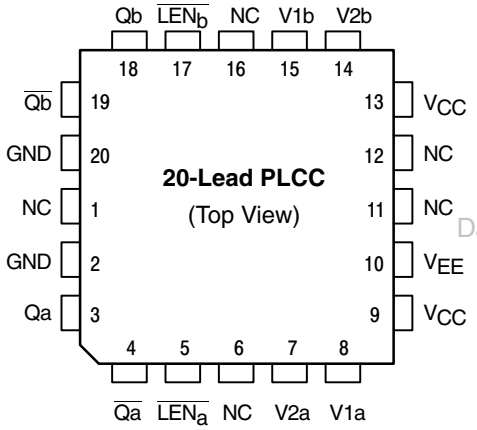
LOGIC DIAGRAM

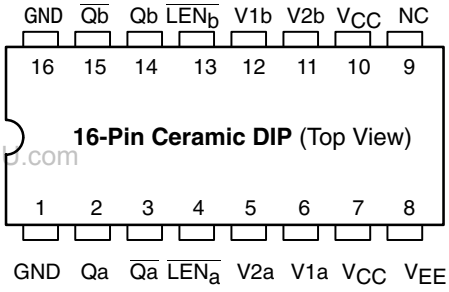


FUNCTION TABLE

$\overline{LEN}$	V1, V2	FUNCTION
H	V1 > V2	H
H	V1 < V2	L
L	X	Latched

LOGIC DIAGRAMS AND PINOUT ASSIGNMENTS





Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

PIN	FUNCTION
Qa, $\overline{Qa}$	ECL Differential Outputs (a)
Qb, $\overline{Qb}$	ECL Differential Outputs (b)
$\overline{LENa}$, $\overline{LENb}$	ECL Latch Enable
V1a, V1b	ECL Input Comparator 1
V2a, V2b	ECL Input Comparator 2
V_{CC}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect
GND	Ground

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
VSUP	Total Supply Voltage	$\|V_{EE}\| + \|V_{CC}\|$		12.0	V
VPP	Differential Input Voltage	|V1 – V2|		3.7	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

DC CHARACTERISTICS V_{CC} = +5.0 V ±5%; V_{EE} = –5.2 V ±5% (Note 1.)

		0°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage (Note 2.)	–1020		–840	–980		–810	–920		–735	mV
V_{OL}	Output Low Voltage (Note 2.)	–1950		–1630	–1950		–1630	–1950		–1600	mV
II I_{IH}	Input Current (V1, V2) Input HIGH Current ($\overline{LEN}$)			65 150			65 150			65 150	µA
I_{CC} I_{EE}	Positive Supply Current Negative Supply Current			50 –55			50 –55			50 –55	mA
VCMR	Common Mode Range (Note 3.)	–2.0		3.0	–2.0		3.0	–2.0		3.0	V
Hys	Hysteresis		27			27			30		mV
V_{skew}	Hysteresis Skew (Note 4.)		–1.0			–1.0			0		mV
C_{in}	Input Capacitance DIP PLCC			 3 2			 3 2			 3 2	pF

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. VCMR Min varies 1:1 with V_{EE}; Max varies 1:1 with V_{CC}.
4. Hysteresis skew (V_{skew}) is provided to indicate the offset of the hysteresis window. For example, at 25°C the nominal hysteresis value is 27mV and the V_{skew} value indicates that the hysteresis was skewed from the reference level by 1mV in the negative direction. Hence the hysteresis window ranged from 14mV below the reference level to 13mV above the reference level. All hysteresis measurements were determined using a reference voltage of 0mV.

AC CHARACTERISTICS V_{CC} = +5.0 V ±5%; V_{EE} = –5.2 V ±5% (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency		TBD			> 1.0			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output (Note 2.) V to Q $\overline{LEN}$ to Q	 600 400	 750 575	 900 750	 625 400	 775 575	 925 750	 700 500	 850 650	 1050 850	ps
t_s	Setup Time V	450	300		450	300		550	350		ps
t_h	Enable Hold Time V	–50	–250		–50	–250		–100	–250		ps
t_{pw}	Minimum Pulse Width $\overline{LEN}$	400			400			400			ps
t_{skew}	Within Device Skew (Note 3.)		15			15			15		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
T_{DE}	Delay Dispersion (ECL Levels) (Notes 4., 5.) (Notes 4., 6.)					 100 60					ps
T_{DL}	Delay Dispersion (TTL Levels) (Notes 7., 8.) (Notes 6., 7.)					 350 100					ps
t_r t_f	Rise/Fall Times (20-80%)	 225	 325	 475	 225	 325	 475	 250	 375	 500	ps

1. Input and output parameters vary 1:1 with V_{CC}.
2. The propagation delay is measured from the crosspoint of the input signal and the threshold value to the crosspoint of the Q and $\overline{Q}$ output signals. For propagation delay measurements the threshold level (V_{THR}) is centered about an 850mV input logic swing with a slew rate of 0.75 V/NS. There is an insignificant change in the propagation delay over the input common mode range.
3. t_{skew} is the propagation delay skew between comparator A and comparator B for a particular part under identical input conditions.
4. Refer to figure 4 and note that the input is at 850mV ECL levels with the input threshold range between the 20% and 80% points. The delay is measured from the crosspoint of the input signal and the threshold value to the crosspoint of the Q and $\overline{Q}$ output signals.
5. The slew rate is 0.25 V/NS for input rising edges.
6. The slew rate is 0.75 V/NS for input rising edges.
7. Refer to Figure 5 and note that the input is at 2.5 V TTL levels with the input threshold range between the 20% and 80% points. The delay is measured from the crosspoint of the input signal and the threshold value to the crosspoint of the Q and $\overline{Q}$ output signals.
8. The slew rate is 0.3 V/NS for input rising edges.

APPLICATIONS INFORMATION

The timing diagram (Figure 1.) is presented to illustrate the MC10E1651's compare and latch features. When the signal on the $\overline{LEN}$ pin is at a logic high level, the device is operating in the "compare mode," and the signal on the input arrives at the output after a nominal propagation delay (t_{PHL}, t_{PLH}). The input signal must be asserted for a time, t_s, prior to the negative going transition on $\overline{LEN}$ and held for a time, t_h, after the LEN transition. After time t_h, the latch is operating in the "latch mode," thus transitions on the input do not appear at the output. The device continues to operate in the "latch mode" until the latch is asserted once again. Moreover, the $\overline{LEN}$ pulse must meet the minimum pulse width (t_{pw}) requirement to effect the correct input-output relationship. Note that the $\overline{LEN}$ waveform in Figure 1. shows the $\overline{LEN}$ signal swinging around a reference labeled VBB_{INT}; this waveform emphasizes the requirement that $\overline{LEN}$ follow typical ECL 10KH logic levels because VBB_{INT} is the internally generated reference level, hence is nominally at the ECL VBB level.

Finally, V_{OD} is the input voltage overdrive and represents the voltage level beyond the threshold level (V_{THR}) to which the input is driven. As an example, if the threshold level is set on one of the comparator inputs as 80 mV and the input signal swing on the complementary input is from zero to 100mV, the positive going overdrive would be 20 mV and the negative going overdrive would be 80mV. The result of differing overdrive levels is that the devices have shorter propagation delays with greater overdrive because the threshold level is crossed sooner than the case of lower overdrive levels. Typically, semiconductor manufactures refer to the threshold voltage as the input offset voltage (VOS) since the threshold voltage is the sum of the externally supplied reference voltage and inherent device offset voltage.

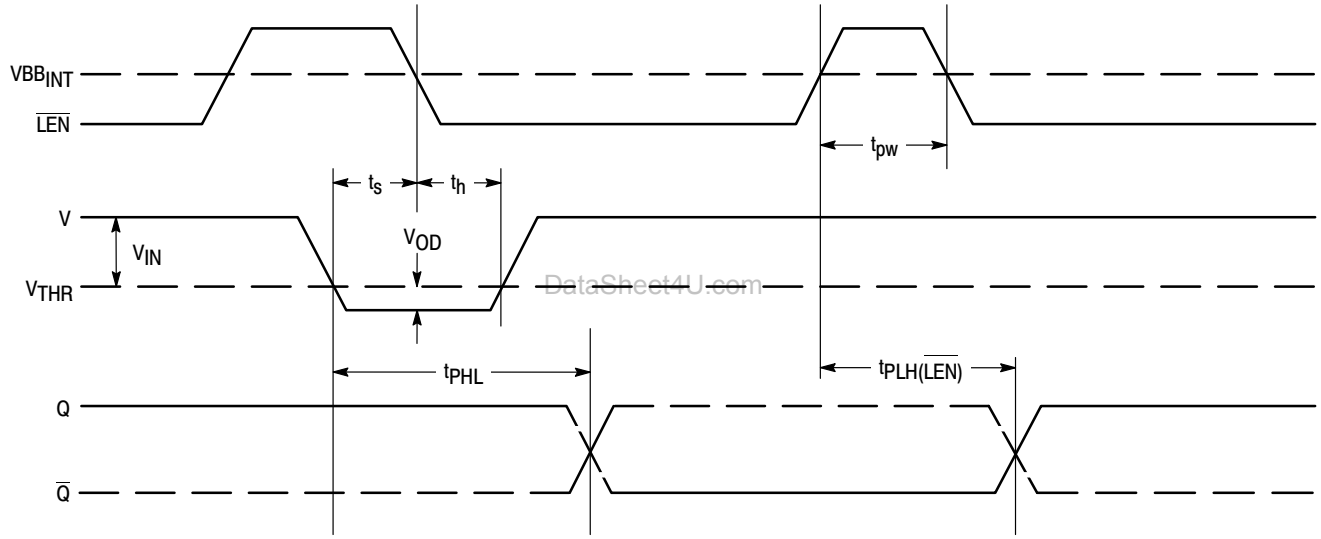


Figure 1. Input/Output Timing Diagram

DELAY DISPERSION

Under a constant set of input conditions comparators have a specified nominal propagation delay. However, since propagation delay is a function of input slew rate and input voltage overdrive the delay dispersion parameters, T_{DE} and T_{DT}, are provided to allow the user to adjust for these variables (where T_{DE} and T_{DT} apply to inputs with standard ECL and TTL levels, respectively).

Figure 2. and Figure 3. define a range of input conditions which incorporate varying input slew rates and input voltage overdrive. For input parameters that adhere to these constraints the propagation delay can be described as:

$$T_{NOM} \pm T_{DE} \text{ (or } T_{DT})$$

where T_{NOM} is the nominal propagation delay. T_{NOM} accounts for nonuniformity introduced by temperature and voltage variability, whereas the delay dispersion parameter takes into consideration input slew rate and input voltage overdrive variability. Thus a modified propagation delay can be approximated to account for the effects of input conditions that differ from those under which the parts where tested. For example, an application may specify an ECL input with a slew rate of 0.25 V/NS, an overdrive of 17 mV and a temperature of 25°C, the delay dispersion parameter would be 100 ps. The modified propagation delay would be

$$775 \text{ ps} \pm 100 \text{ ps}$$

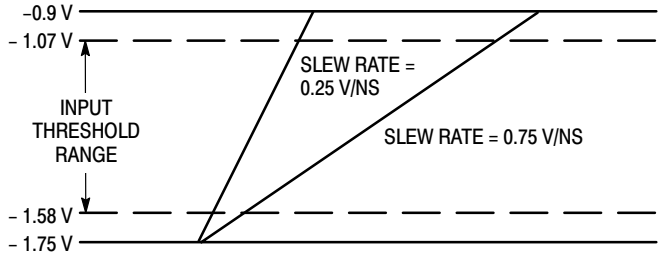


Figure 2. ECL Dispersion Test Input Conditions

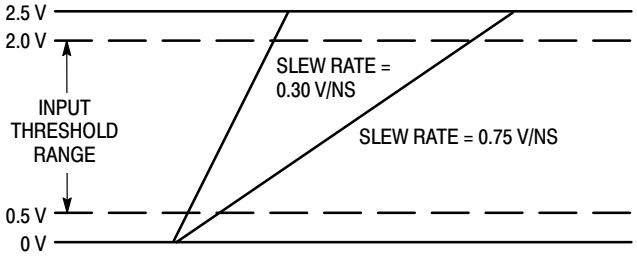


Figure 3. TTL Dispersion Test Input Conditions

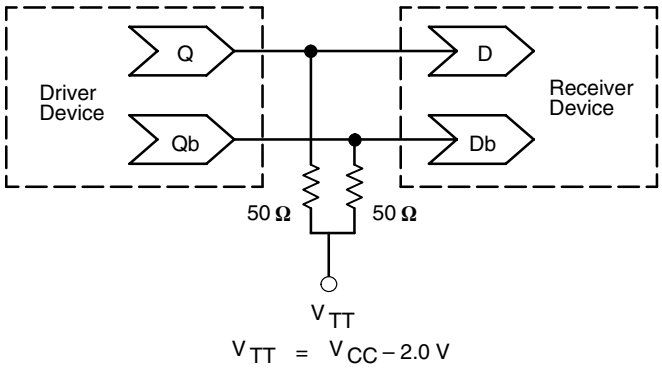


Figure 4. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10E1652

5V ECL Dual ECL Output Comparator With Latch

The MC10E1652 is fabricated using ON Semiconductor's advanced MOSAIC III™ process and is output compatible with 10H logic devices. In addition, the device is available in both a 16-pin DIP and a 20-pin surface mount package. However, the MC10E1652 provides user programmable hysteresis.

The latch enable ($\overline{LEN}_a$ and $\overline{LEN}_b$) input pins operate from standard ECL 10H logic levels. When the latch enable is at a logic high level, the MC10E1652 acts as a comparator; hence, Q will be at a logic high level if V1 > V2 (V1 is more positive than V2). $\overline{Q}$ is the complement of Q. When the latch enable input goes to a low logic level, the outputs are latched in their present state, providing the latch enable setup and hold time constraints are met. The level of input hysteresis is controlled by applying a bias voltage to the HYS pin.

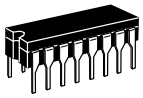
The 100 Series contains temperature compensation.

- Typical 3.0 dB Bandwidth > 1.0 GHz
- Typical V to Q Propagation Delay of 775 ps
- Typical Output Rise/Fall of 350 ps
- Common Mode Range –2.0 V to +3.0 V
- Individual Latch Enables
- Differential Outputs
- Operating Mode: V_{CC}= 5.0 V, V_{EE}= –5.2 V
- Programmable Input Hysteresis
- No Internal Input Pulldown Resistors
- ESD Protection: > 2 KV HBM, > 100 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8",
  Oxygen Index 28 to 34
- Transistor Count = 85 devices

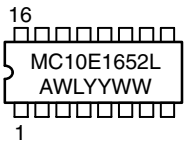
ON Semiconductor™

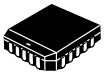
http://onsemi.com

MARKING DIAGRAMS

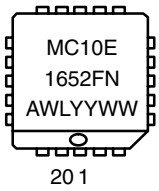


CDIP–16
L SUFFIX
CASE 620





PLCC–20
FN SUFFIX
CASE 775

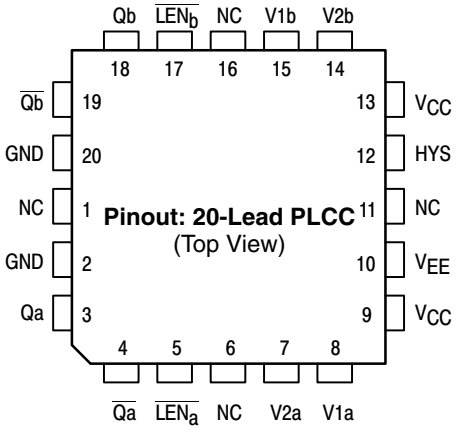


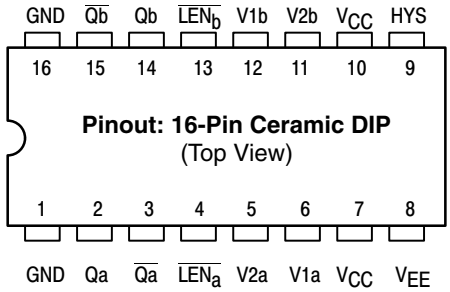
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC10E1652L	CDIP–16	25 Units/Rail
MC10E1652FN	PLCC–20	46 Units/Rail
MC10E1652FNR2	PLCC–20	500 Units/Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT





* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

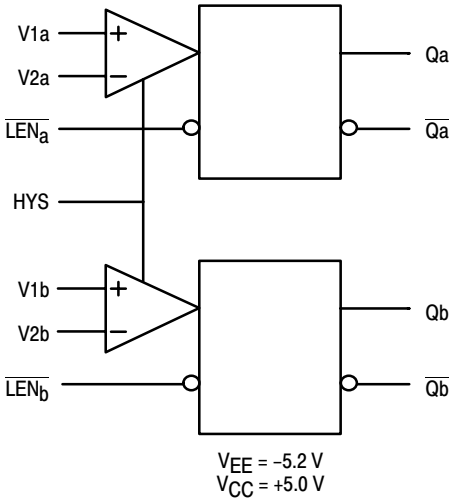
PIN DESCRIPTION

PIN	FUNCTION
Qa, $\overline{Qa}$	ECL Differential Outputs (a)
Qb, $\overline{Qb}$	ECL Differential Outputs (b)
$\overline{LENa}$, $\overline{LENb}$	ECL Latch Enable
V1a, V1b	ECL Input Comparator 1
V2a, V2b	ECL Input Comparator 2
HYS	ECL Hysteresis Control
V_{CC}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect
GND	Ground

FUNCTION TABLE

$\overline{LEN}$	V1, V2	Function
H	V1 > V2	H
H	V1 < V2	L
L	X	Latched

LOGIC DIAGRAM



MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
VSUP	Total Supply Voltage	$\|V_{EE}\| + \|V_{CC}\|$		12.0	V
VPP	Differential Input Voltage	|V1 – V2|		3.7	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	12 –12	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V_{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 –5.7 to –4.2	V V
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

DC CHARACTERISTICS V_{CC} = +5.0 V ±5%; V_{EE} = –5.2 V ±5% (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage (Note 2.)	–1020		–840	–980		–810	–920		–735	mV
V_{OL}	Output Low Voltage (Note 2.)	–1950		–1630	–1950		–1630	–1950		–1600	mV
II I_{IH}	Input Current (V1, V2) Input HIGH Current ($\overline{LEN}$)			65 150			65 150			65 150	μA
I_{CC} I_{EE}	Positive Supply Current Negative Supply Current			50 –55			50 –55			50 –55	mA
VCMR	Common Mode Range (Note 3.)	–2.0		3.0	–2.0		3.0	–2.0		3.0	V
Hys	Hysteresis (Note 4.)		27			27			30		mV
V_{skew}	Hysteresis Skew (Note 5.)		–1.0			–1.0			0		mV
C_{in}	Input Capacitance DIP PLCC			 3 2			 3 2			 3 2	pF

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. VCMR Min varies 1:1 with V_{EE}; Max varies 1:1 with V_{CC}.
4. The HYS pin programming characterization information is shown in Figure 2, The hysteresis values indicated in the data sheet are for the condition in which the voltage on the HYS pin is set to V_{EE}.
5. Hysteresis skew (V_{skew}) is provided to indicate the offset of the hysteresis window. For example, at 25°C the nominal hysteresis value is 27 mV and the V_{skew} value indicates that the hysteresis was skewed from the reference level by 1 mV in the negative direction. Hence the hysteresis window ranged from 14 mV below the reference level to 13 mV above the reference level. All hysteresis measurements were determined using a reference voltage of 0 mV. The hysteresis skew values apply over the programming range shown in Figure 2.

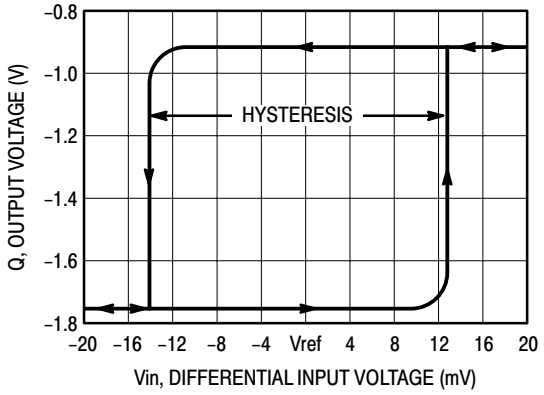


Figure 1. Typical Hysteresis Curve

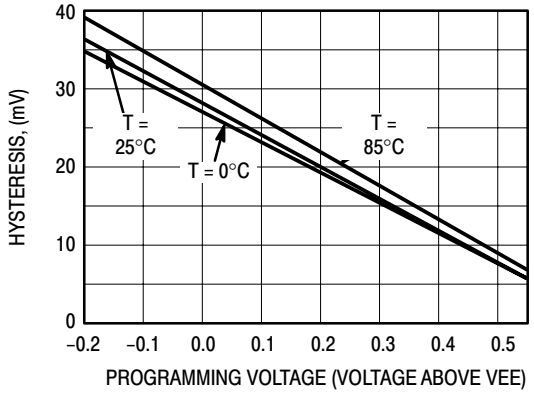


Figure 2. Hysteresis Programming Voltage

AC CHARACTERISTICS V_{CC} = +5.0 V ±5%; V_{EE} = –5.2 V ±5% (Note 1.)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency		TBD			> 1.0			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output (Note 2.) V to Q $\overline{LEN}$ to Q	 600 400	 750 575	 900 750	 625 400	 775 575	 925 750	 700 500	 850 650	 1050 850	ps
t_s	Setup Time V	 450	 300		 450	 300		 550	 350		ps
t_h	Enable Hold Time V	 –50	 –250		 –50	 –250		 –100	 –250		ps
t_{pw}	Minimum Pulse Width $\overline{LEN}$	 400			 400			 400			ps
t_{skew}	Within Device Skew (Note 3.)		15			15			15		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
T_{DE}	Delay Dispersion (ECL Levels) (Notes 4. 5.) (Notes 4., 6.)					 100 60					ps
T_{DL}	Delay Dispersion (TTL Levels) (Notes 7., 8.) (Notes 6., 7.)					 350 100					ps
VPP	Differential Input Voltage |V1 – V2|			3.7			3.7			3.7	V
t_r t_f	Rise/Fall Times (20-80%)	 225	 325	 475	 225	 325	 475	 250	 375	 500	ps

1. Input and output parameters vary 1:1 with V_{CC}.
2. The propagation delay is measured from the crosspoint of the input signal and the threshold value to the crosspoint of the Q and $\overline{Q}$ output signals. For propagation delay measurements the threshold level (V_{THR}) is centered about an 850 mV input logic swing with a slew rate of 0.75 V/NS. There is an insignificant change in the propagation delay over the input common mode range.
3. t_{skew} is the propagation delay skew between comparator A and comparator B for a particular part under identical input conditions.
4. Refer to Figure 4 and note that the input is at 850 mV ECL levels with the input threshold range between the 20% and 80% points. The delay is measured from the crosspoint of the input signal and the threshold value to the crosspoint of the Q and $\overline{Q}$ output signals.
5. The slew rate is 0.25 V/NS for input rising edges.
6. The slew rate is 0.75 V/NS for input rising edges.
7. Refer to Figure 5 and note that the input is at 2.5 V TTL levels with the input threshold range between the 20% and 80% points. The delay is measured from the crosspoint of the input signal and the threshold value to the crosspoint of the Q and $\overline{Q}$ output signals.
8. The slew rate is 0.3 V/NS for input rising edges.

APPLICATIONS INFORMATION

The timing diagram (Figure 3.) is presented to illustrate the MC10E1652's compare and latch features. When the signal on the $\overline{LEN}$ pin is at a logic high level, the device is operating in the "compare mode," and the signal on the input arrives at the output after a nominal propagation delay (t_{PHL}, t_{PLH}). The input signal must be asserted for a time, t_s, prior to the negative going transition on $\overline{LEN}$ and held for a time, t_h, after the LEN transition. After time t_h, the latch is operating in the "latch mode," thus transitions on the input do not appear at the output. The device continues to operate in the "latch mode" until the latch is asserted once again. Moreover, the $\overline{LEN}$ pulse must meet the minimum pulse width (t_{pw}) requirement to effect the correct input-output relationship. Note that the $\overline{LEN}$ waveform in Figure 3. shows the $\overline{LEN}$ signal swinging around a reference labeled VBB_{INT}; this waveform emphasizes the requirement that $\overline{LEN}$ follow typical ECL 10KH logic levels because VBB_{INT} is the internally generated reference level, hence is nominally at the ECL VBB level.

Finally, V_{OD} is the input voltage overdrive and represents the voltage level beyond the threshold level (V_{THR}) to which the input is driven. As an example, if the threshold level is set on one of the comparator inputs as 80 mV and the input signal swing on the complementary input is from zero to 100 mV, the positive going overdrive would be 20 mV and the negative going overdrive would be 80 mV. The result of differing overdrive levels is that the devices have shorter propagation delays with greater overdrive because the threshold level is crossed sooner than the case of lower overdrive levels. Typically, semiconductor manufactures refer to the threshold voltage as the input offset voltage (VOS) since the threshold voltage is the sum of the externally supplied reference voltage and inherent device offset voltage.

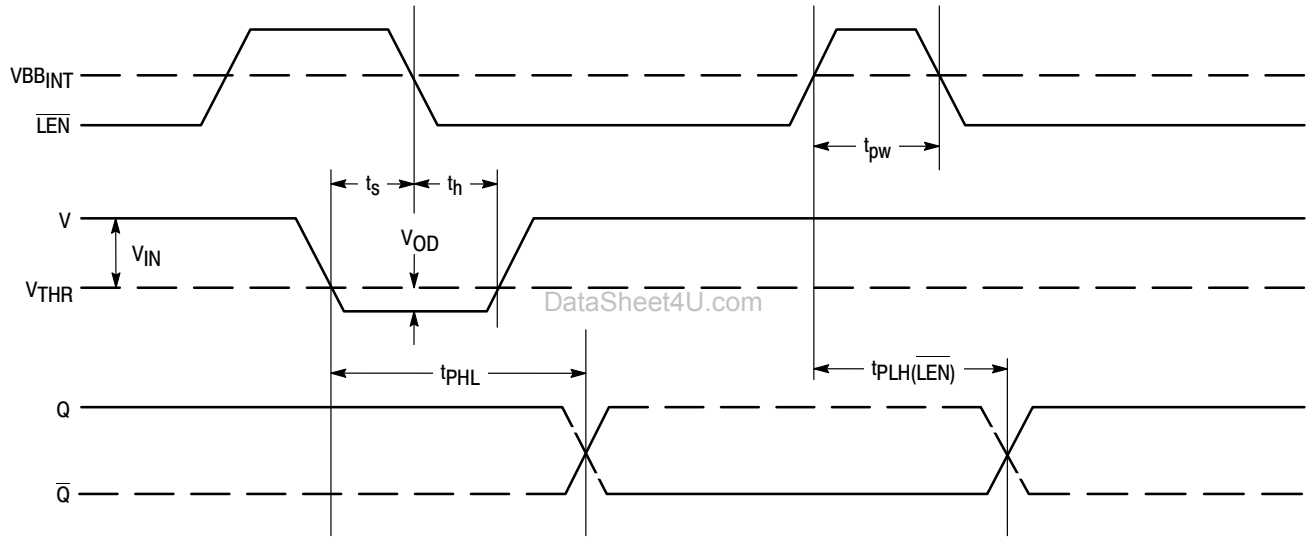


Figure 3. Input/Output Timing Diagram

DELAY DISPERSION

Under a constant set of input conditions comparators have a specified nominal propagation delay. However, since propagation delay is a function of input slew rate and input voltage overdrive the delay dispersion parameters, T_{DE} and T_{DT}, are provided to allow the user to adjust for these variables (where T_{DE} and T_{DT} apply to inputs with standard ECL and TTL levels, respectively).

Figure 4. and Figure 5. define a range of input conditions which incorporate varying input slew rates and input voltage overdrive. For input parameters that adhere to these constraints the propagation delay can be described as:

$$T_{NOM} \pm T_{DE} \text{ (or } T_{DT})$$

where T_{NOM} is the nominal propagation delay. T_{NOM} accounts for nonuniformity introduced by temperature and voltage variability, whereas the delay dispersion parameter takes into consideration input slew rate and input voltage overdrive variability. Thus a modified propagation delay can be approximated to account for the effects of input conditions that differ from those under which the parts where tested. For example, an application may specify an ECL input with a slew rate of 0.25 V/NS, an overdrive of 17 mV and a temperature of 25°C, the delay dispersion parameter would be 100 ps. The modified propagation delay would be

$$775 \text{ ps} \pm 100 \text{ ps}$$

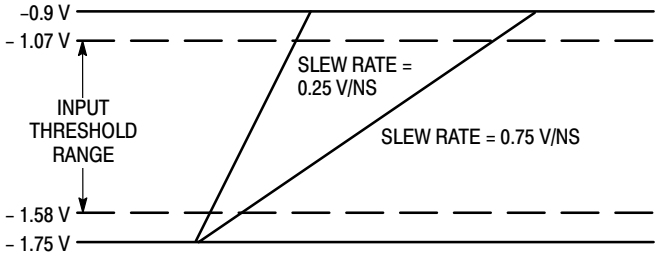


Figure 4. ECL Dispersion Test Input Conditions

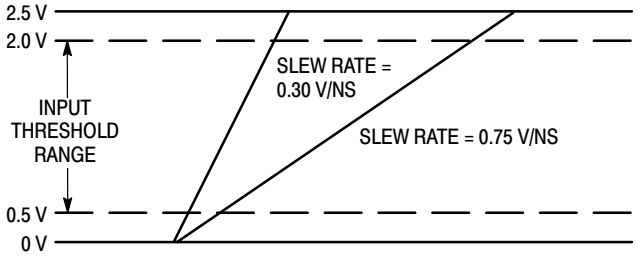


Figure 5. TTL Dispersion Test Input Conditions

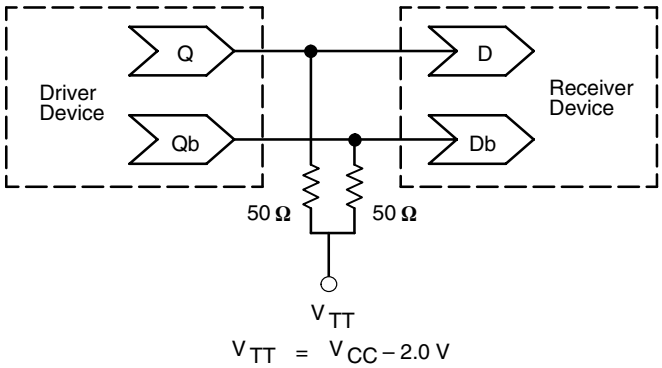


Figure 6. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

CHAPTER 2
ECLinPS Lite Data Sheets

MC10EL01, MC100EL01

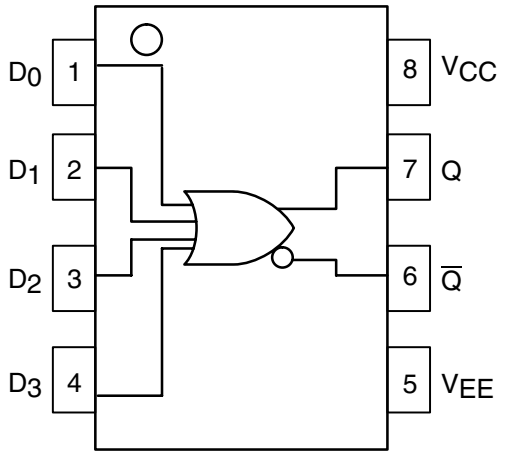
5V ECL 4-Input OR/NOR

The MC10EL/100EL01 is a 4-input OR/NOR gate. The device is functionally equivalent to the E101 device with higher performance capabilities. With propagation delays and output transition times significantly faster than the E101, the EL01 is ideally suited for those applications which require the ultimate in AC performance.

The 100 series contains temperature compensation.

- 230 ps Propagation Delay
- ESD Protection: > 1 KV HBM, > 100 V MM
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 46 devices

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
D0–D3	ECL Data Inputs
Q, $\overline{Q}$	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

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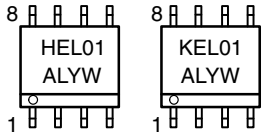
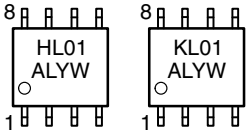
MARKING DIAGRAMS*

SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10EL01D	SO–8	98 Units/Rail
MC10EL01DR2	SO–8	2500 Tape & Reel
MC100EL01D	SO–8	98 Units/Rail
MC100EL01DR2	SO–8	2500 Tape & Reel
MC10EL01DT	TSSOP–8	98 Units/Rail
MC10EL01DTR2	TSSOP–8	2500 Tape & Reel
MC100EL01DT	TSSOP–8	98 Units/Rail
MC100EL01DTR2	TSSOP–8	2500 Tape & Reel

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		14	17		14	17		14	17	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3770		4110	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage	3050		3500	3050		3520	3050		3555	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.25 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		14	17		14	17		14	17	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1080	–990	–890	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1800	–1650	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1230		–890	–1130		–810	–1060		–720	mV
V_{IL}	Input LOW Voltage	–1950		–1500	–1950		–1480	–1950		–1445	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.25 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		14	17		14	17		16	20	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage	3190		3525	3190		3525	3190		3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		14	17		14	17		16	20	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage	–1810		–1475	–1810		–1475	–1810		–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output	70	220	370	130	230	330	150	250	350	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	100	225	350	100	225	350	100	225	350	ps

1. 10 Series: V_{EE} can vary +0.25 V / –0.5 V.
   100 Series: V_{EE} can vary +0.8 V / –0.5 V.

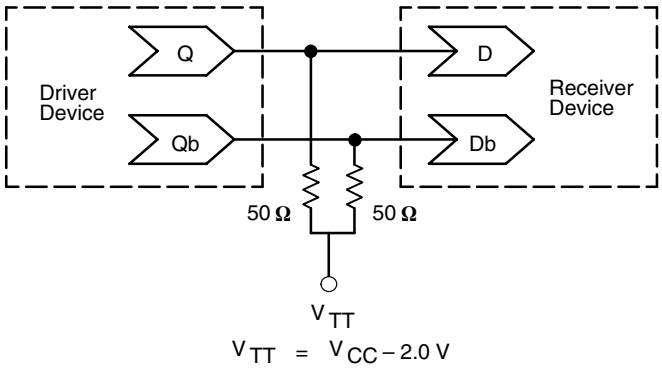


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10EL04, MC100EL04

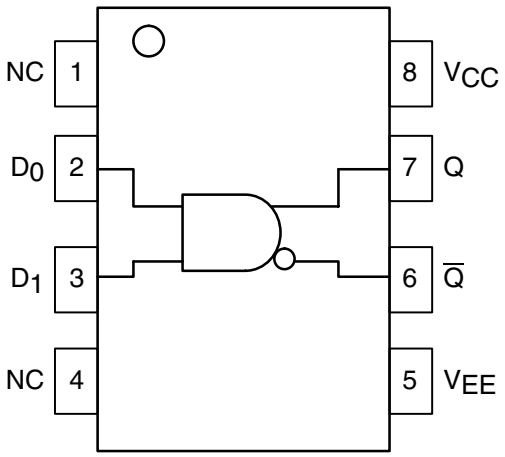
5V ECL 2-Input AND/NAND

The MC10EL/100EL04 is a 2-input AND/NAND gate. The device is functionally equivalent to the E104 device with higher performance capabilities. With propagation delays and output transition times significantly faster than the E104, the EL04 is ideally suited for those applications which require the ultimate in AC performance.

The 100 Series contains temperature compensation.

- 240 ps Propagation Delay
- ESD Protection: > 1 KV HBM, > 100 V MM
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 45 devices

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
D0, D1	ECL Data Inputs
Q, $\overline{Q}$	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

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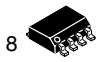
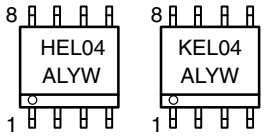
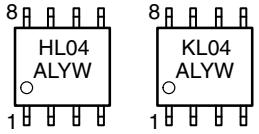
MARKING DIAGRAMS*



SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10EL04D	SO–8	98 Units/Rail
MC10EL04DR2	SO–8	2500 Tape & Reel
MC100EL04D	SO–8	98 Units/Rail
MC100EL04DR2	SO–8	2500 Tape & Reel
MC10EL04DT	TSSOP–8	98 Units/Rail
MC10EL04DTR2	TSSOP–8	2500 Tape & Reel
MC100EL04DT	TSSOP–8	98 Units/Rail
MC100EL04DTR2	TSSOP–8	2500 Tape & Reel

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		14	17		14	17		14	17	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3770		4110	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage	3050		3500	3050		3520	3050		3555	mV
I_{IH}	Input HIGH Current D0 D1			 250 150			 250 150			 250 150	µA
I_{IL}	Input LOW Current	0.5			0.5			0.3			µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}.
   V_{EE} can vary +0.25 V / –0.5 V for +25°C and +85°C. or V_{EE} can vary +0.06 V / –0.5 V for –40°C.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		14	17		14	17		14	17	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1080	–990	–890	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1800	–1650	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1230		–890	–1130		–810	–1060		–720	mV
V_{IL}	Input LOW Voltage	–1950		–1500	–1950		–1480	–1950		–1445	mV
I_{IH}	Input HIGH Current D0 D1			 250 150			 250 150			 250 150	µA
I_{IL}	Input LOW Current	0.5			0.5			0.3			µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}.
   V_{EE} can vary +0.25 V / –0.5 V for +25°C and +85°C. or V_{EE} can vary +0.06 V / –0.5 V for –40°C.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		14	17		14	17		16	20	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage	3190		3525	3190		3525	3190		3525	mV
I_{IH}	Input HIGH Current D0 D1			 250 150			 250 150			 250 150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		14	17		14	17		16	20	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage	–1810		–1475	–1810		–1475	–1810		–1475	mV
I_{IH}	Input HIGH Current D0 D1			 250 150			 250 150			 250 150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output	70	235	410	130	240	370	155	265	395	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	100	225	350	100	225	350	100	225	350	ps

1. 10 Series: V_{EE} can vary +0.25 V / –0.5 V for +25°C and +85°C. or V_{EE} can vary +0.06 V / –0.5 V for –40°C.
   100 Series: V_{EE} can vary +0.8 V / –0.5 V.

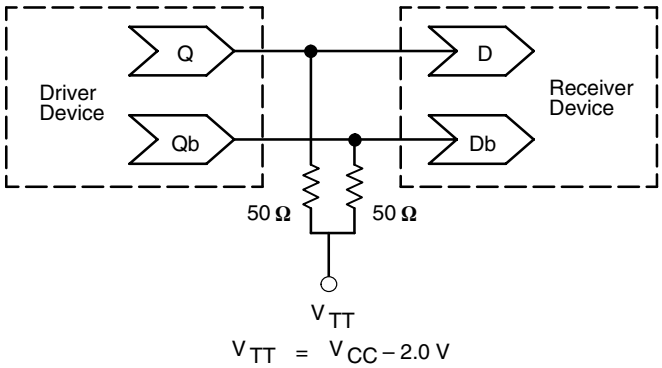


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10EL05, MC100EL05

5V ECL 2-Input Differential AND/NAND

The MC10EL/100EL05 is a 2-input differential AND/NAND gate. The device is functionally equivalent to the E404 device with higher performance capabilities. With propagation delays and output transition times significantly faster than the E404, the EL05 is ideally suited for those applications which require the ultimate in AC performance.

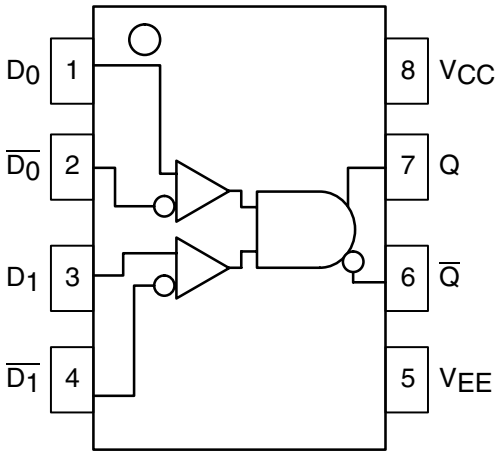
Because a negative 2-input NAND is equivalent to a 2-input OR function, the differential inputs and outputs of the device allows the EL05 to also be used as a 2-input differential OR/NOR gate.

The differential inputs employ clamp circuitry so that under open input conditions (pulled down to V_{EE}) the input to the AND gate will be HIGH. In this way, if one set of inputs is open, the gate will remain active to the other input.

The 100 Series contains temperature compensation.

- 275 ps Propagation Delay
- ESD Protection: > 1 KV HBM, > 100 V MM
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 44 devices

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
D0, $\overline{D0}$; D1, $\overline{D1}$	ECL Data Inputs
Q, $\overline{Q}$	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

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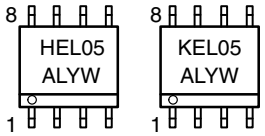
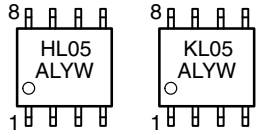
MARKING DIAGRAMS*

SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

TRUTH TABLE

D0	D1	$\overline{D0}$	$\overline{D1}$	Q	$\overline{Q}$
L	L	H	H	L	H
L	H	H	L	L	H
H	L	L	H	L	H
H	H	L	L	H	L

ORDERING INFORMATION

Device	Package	Shipping
MC10EL05D	SO–8	98 Units/Rail
MC10EL05DR2	SO–8	2500 Tape & Reel
MC100EL05D	SO–8	98 Units/Rail
MC100EL05DR2	SO–8	2500 Tape & Reel
MC10EL05DT	TSSOP–8	98 Units/Rail
MC10EL05DTR2	TSSOP–8	2500 Tape & Reel
MC100EL05DT	TSSOP–8	98 Units/Rail
MC100EL05DTR2	TSSOP–8	2500 Tape & Reel

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		18	22		18	22		18	22	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3770		4110	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage (Single Ended)	3050		3500	3050		3520	3050		3555	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	3.0		4.6	3.0		4.6	3.0		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.25 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

10EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		18	22		18	22		18	22	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1080	–990	–890	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1800	–1650	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1230		–890	–1130		–810	–1060		–720	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1950		–1500	–1950		–1480	–1950		–1445	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.0		–0.4	–2.0		–0.4	–2.0		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.25 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

100EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		18	22		18	22		21	25	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	3.0		4.6	3.0		4.6	3.0		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

100EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		18	22		18	22		21	25	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.0		–0.4	–2.0		–0.4	–2.0		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output	135	260	440	185	275	390	215	305	420	ps
V_{PP}	Input Swing (Note 2.)	150		1000	150		1000	150		1000	mV
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	100	225	350	100	225	350	100	225	350	ps

1. 10 Series: V_{EE} can vary +0.25 V / –0.5 V.
   100 Series: V_{EE} can vary +0.8 V / –0.5 V.
2. $V_{PP(}$min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

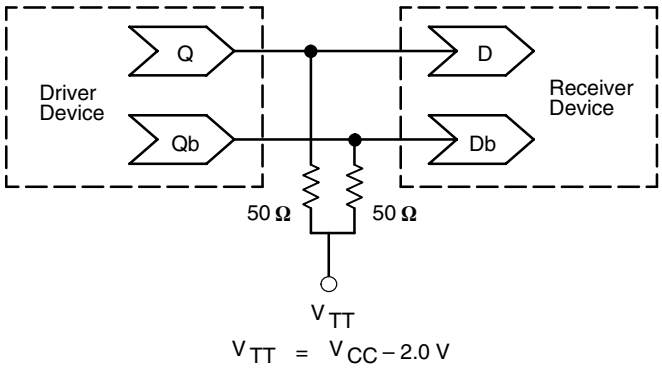


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10EL07, MC100EL07

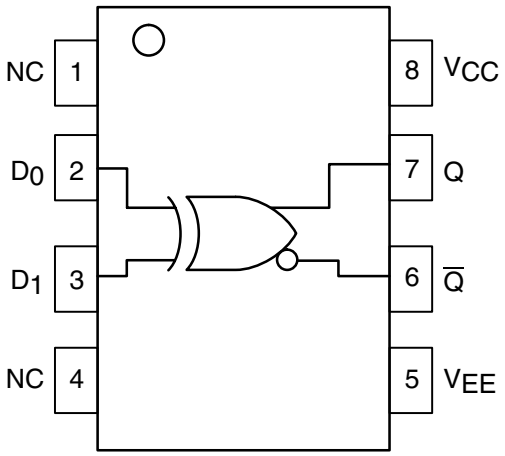
5V ECL 2-Input XOR/XNOR

The MC10EL/100EL07 is a 2-input XOR/XNOR gate. The device is functionally equivalent to the E107 device with higher performance capabilities. With propagation delays and output transition times significantly faster than the E107, the EL07 is ideally suited for those applications which require the ultimate in AC performance.

The 100 Series contains temperature compensation.

- 260 ps Propagation Delay
- ESD Protection: > 1 KV HBM, > 100 V MM
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 47 devices

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
D0, D1	ECL Data Inputs
Q, $\overline{Q}$	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

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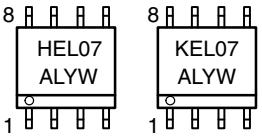
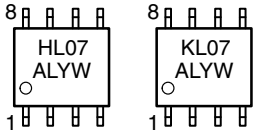
MARKING DIAGRAMS*

SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10EL07D	SO–8	98 Units/Rail
MC10EL07DR2	SO–8	2500 Tape & Reel
MC100EL07D	SO–8	98 Units/Rail
MC100EL07DR2	SO–8	2500 Tape & Reel
MC10EL07DT	TSSOP–8	98 Units/Rail
MC10EL07DTR2	TSSOP–8	2500 Tape & Reel
MC100EL07DT	TSSOP–8	98 Units/Rail
MC100EL07DTR2	TSSOP–8	2500 Tape & Reel

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		14	17		14	17		14	17	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3770		4110	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage	3050		3500	3050		3520	3050		3555	mV
I_{IH}	Input HIGH Current D0 D1			 250 150			 250 150			 250 150	µA
I_{IL}	Input LOW Current	0.5			0.5			0.3			µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}.
   V_{EE} can vary +0.25 V / –0.5 V for +25°C and +85°C. or V_{EE} can vary +0.06 V / –0.5 V for –40°C.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		14	17		14	17		14	17	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1080	–990	–890	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1800	–1650	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1230		–890	–1130		–810	–1060		–720	mV
V_{IL}	Input LOW Voltage	–1950		–1500	–1950		–1480	–1950		–1445	mV
I_{IH}	Input HIGH Current D0 D1			 250 150			 250 150			 250 150	µA
I_{IL}	Input LOW Current	0.5			0.5			0.3			µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}.
   V_{EE} can vary +0.25 V / –0.5 V for +25°C and +85°C. or V_{EE} can vary +0.06 V / –0.5 V for –40°C.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		14	17		14	17		16	20	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage	3190		3525	3190		3525	3190		3525	mV
I_{IH}	Input HIGH Current D0 D1			 250 150			 250 150			 250 150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		14	17		14	17		16	20	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage	–1810		–1475	–1810		–1475	–1810		–1475	mV
I_{IH}	Input HIGH Current D0 D1			 250 150			 250 150			 250 150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output	90	250	435	150	260	395	170	280	415	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	100	225	350	100	225	350	100	225	350	ps

1. 10 Series: V_{EE} can vary +0.25 V / –0.5 V for +25°C and +85°C. or V_{EE} can vary +0.06 V / –0.5 V for –40°C.
   100 Series: V_{EE} can vary +0.8 V / –0.5 V.

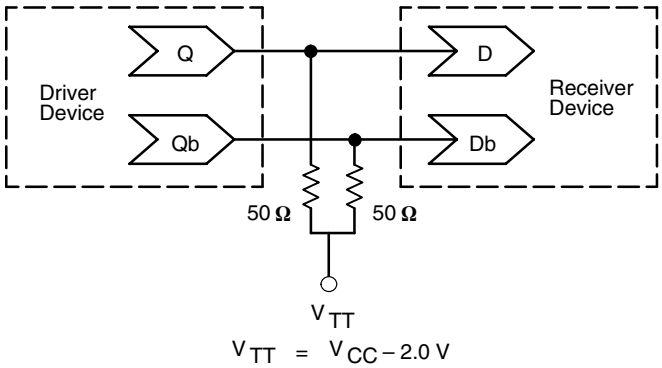


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10EL11, MC100EL11

5V ECL 1:2 Differential Fanout Buffer

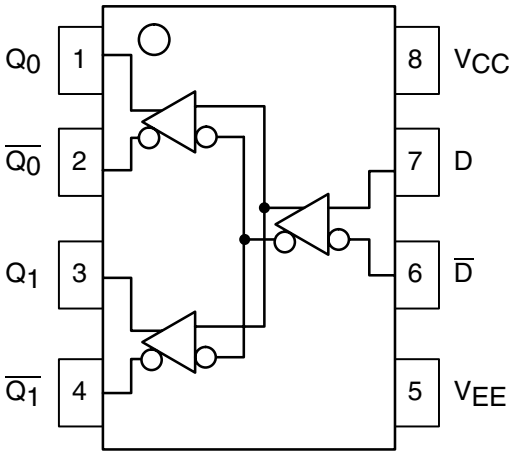
The MC10EL/100EL11 is a differential 1:2 fanout buffer. The device is functionally similar to the E111 device but with higher performance capabilities. Having within-device skews and output transition times significantly improved over the E111, the EL11 is ideally suited for those applications which require the ultimate in AC performance.

The differential inputs of the EL11 employ clamping circuitry to maintain stability under open input conditions. If the inputs are left open (pulled to V_{EE}) the Q outputs will go LOW.

The 100 Series contains temperature compensation.

- 265 ps Propagation Delay
- 5 ps Skew Between Outputs
- ESD Protection: > 1 KV HBM, > 100 V MM
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 44 devices

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
D, $\overline{D}$	ECL Data Inputs
Q0, $\overline{Q0}$; Q1, $\overline{Q1}$	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

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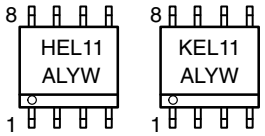
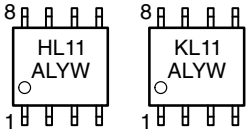
MARKING DIAGRAMS*

SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10EL11D	SO–8	98 Units/Rail
MC10EL11DR2	SO–8	2500 Tape & Reel
MC100EL11D	SO–8	98 Units/Rail
MC100EL11DR2	SO–8	2500 Tape & Reel
MC10EL11DT	TSSOP–8	98 Units/Rail
MC10EL11DTR2	TSSOP–8	2500 Tape & Reel
MC100EL11DT	TSSOP–8	98 Units/Rail
MC100EL11DTR2	TSSOP–8	2500 Tape & Reel

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		26	31		26	31		26	31	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3770		4110	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage (Single Ended)	3050		3500	3050		3520	3050		3555	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.5		4.6	2.5		4.6	2.5		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.25 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

10EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		26	31		26	31		26	31	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1080	–990	–890	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1800	–1650	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1230		–890	–1130		–810	–1060		–720	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1950		–1500	–1950		–1480	–1950		–1445	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.5		–0.4	–2.5		–0.4	–2.5		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.25 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

100EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		26	31		26	31		30	36	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.5		4.6	2.5		4.6	2.5		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

100EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		26	31		26	31		30	36	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.5		–0.4	–2.5		–0.4	–2.5		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output	135	260	385	190	265	340	215	290	365	ps
t_{SKEW}	Within-Device Skew (Note 2.) Duty Cycle Skew (Note 3.)		5 5			5 5	20 20		5 5	20 20	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 4.)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	100	225	350	100	225	350	100	225	350	ps

1. 10 Series: V_{EE} can vary +0.25 V / –0.5 V.
   100 Series: V_{EE} can vary +0.8 V / –0.5 V.
2. Within-device skew defined as identical transitions on similar paths through a device.
3. Duty cycle skew is the difference between a TPLH and TPHL propagation delay through a device.
4. $V_{PP(}$min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

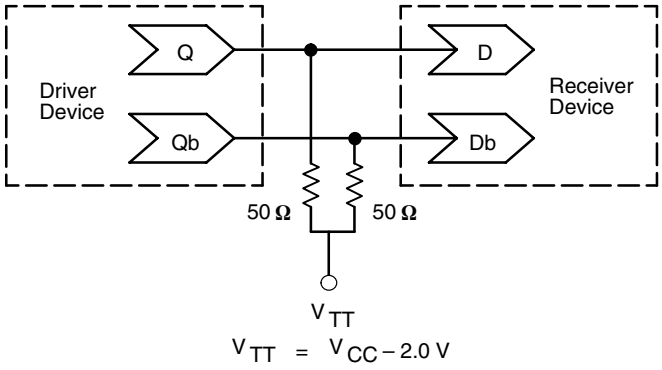


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10EL12, MC100EL12

5V ECL Low Impedance Driver

The MC10EL/100EL12 is a low impedance drive buffer. With two pairs of OR/NOR outputs the device is ideally suited for high drive applications such as memory addressing. The device is a function equivalent to the E112 device with higher performance capabilities. With propagation delays significantly faster than the E112, the EL12 is ideally suited for those applications which require the ultimate in AC performance.

The 100 Series contains temperature compensation.

- 290 ps Propagation Delay
- Dual Outputs for 25 Ω Drive Applications
- ESD Protection: > 1 KV HBM, > 100 V MM
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 44 devices

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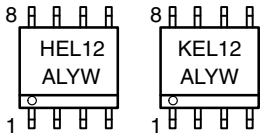
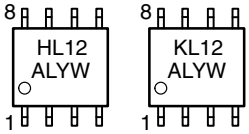
MARKING DIAGRAMS*

SO–8
D SUFFIX
CASE 751



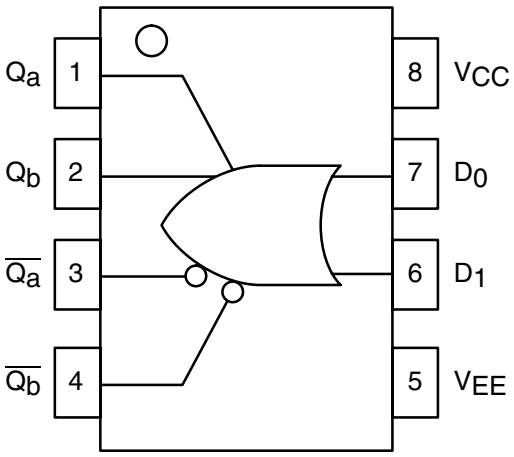
TSSOP–8
DT SUFFIX
CASE 948R



H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
D0, D1	ECL Data Inputs
Qa,$\overline{Qa}$; Qb, $\overline{Qb}$	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

ORDERING INFORMATION

Device	Package	Shipping
MC10EL12D	SO–8	98 Units/Rail
MC10EL12DR2	SO–8	2500 Tape & Reel
MC100EL12D	SO–8	98 Units/Rail
MC100EL12DR2	SO–8	2500 Tape & Reel
MC10EL12DT	TSSOP–8	98 Units/Rail
MC10EL12DTR2	TSSOP–8	2500 Tape & Reel
MC100EL12DT	TSSOP–8	98 Units/Rail
MC100EL12DTR2	TSSOP–8	2500 Tape & Reel

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		14	17		14	17		14	17	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3770		4110	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage	3050		3500	3050		3520	3050		3555	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.06 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		14	17		14	17		14	17	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1080	–990	–890	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1800	–1650	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1230		–890	–1130		–810	–1060		–720	mV
V_{IL}	Input LOW Voltage	–1950		–1500	–1950		–1480	–1950		–1445	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.06 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		14	17		14	17		16	20	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage	3190		3525	3190		3525	3190		3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		14	17		14	17		16	20	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage	–1810		–1475	–1810		–1475	–1810		–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output	120	280	500	180	290	450	210	320	480	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	150	350	550	150	350	550	150	350	550	ps

1. 10 Series: V_{EE} can vary +0.06 V / –0.5 V.
   100 Series: V_{EE} can vary +0.8 V / –0.5 V.

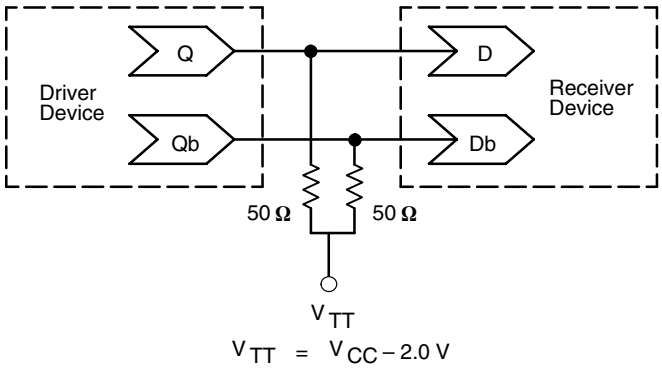


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC100EL13

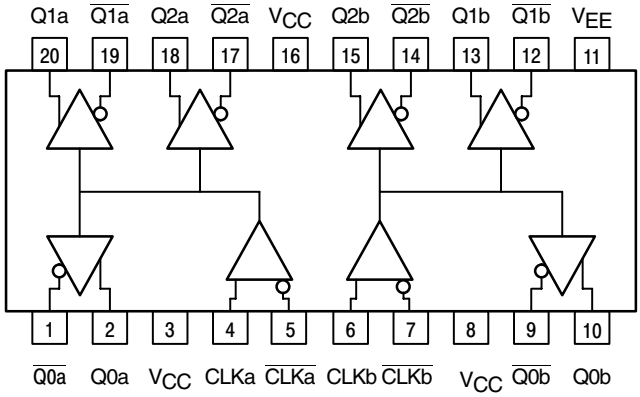
5V ECL Dual 1:3 Fanout Buffer

The MC100EL13 is a dual, fully differential 1:3 fanout buffer. The Low Output–Output Skew of the device makes it ideal for distributing two different frequency synchronous signals.

The differential inputs have special circuitry which ensures device stability under open input conditions. When both differential inputs are left open the D input will pull down to V_{EE}, The $\overline{D}$ input will bias around $V_{CC}/2$ and the Q output will go LOW.

- 500 ps Typical Propagation Delays
- 50 ps Output–Output Skews
- ESD Protection: > 2 KV HBM, > 100 V MM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 143 devices

Logic Diagram and Pinout: 20–Lead SOIC (Top View)



* All V_{CC} pins are tied together on the die.

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

PIN	FUNCTION
Qna, $\overline{Qna}$	ECL Differential Clock Outputs
Qnb, $\overline{Qnb}$	ECL Differential Clock Outputs
CLKn, $\overline{CLKn}$	ECL Differential Clock Inputs
V_{CC}	Positive Supply
VEE	Negative Supply

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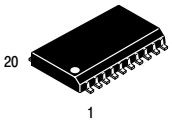
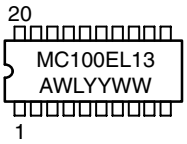
MARKING DIAGRAM



SO–20
DW SUFFIX
CASE 751D



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC100EL13DW	SO–20	38 Units/Rail
MC100EL13DWR2	SO–20	1000 Units/Reel

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

100EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		30	38		30	38		32	40	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Common Mode Range (Differential) (Note 3.) V_{PP} < 500 mV $V_{PP} \geq$ 500 mV	 1.3 1.5		 4.6 4.6	 1.2 1.4		 4.6 4.6	 1.2 1.4		 4.6 4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

100EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		30	38		30	38		32	40	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Common Mode Range (Differential) (Note 3.) V_{PP} < 500 mV $V_{PP} \geq$ 500 mV	 –3.7 –3.5		 –0.4 –0.4	 –3.8 –3.6		 –0.4 –0.4	 –3.8 –3.6		 –0.4 –0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay CLK→Q/$\overline{Q}$	410		600	430		620	450		640	ps
$t_{sk(O)}$	Output–Output Skew Any Qa→Qa, Any Qb→Qb Any Qa→Any Qb			 50 75			 50 75			 50 75	ps
$t_{sk(DC)}$	Duty Cycle Skew $\lvert t_{PLH} - t_{PHL} \rvert$			50			50			50	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 2.)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	230		500	230		500	230		500	ps

1. V_{EE} can vary +0.8 V / –0.5 V.
2. $V_{PP(}$min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

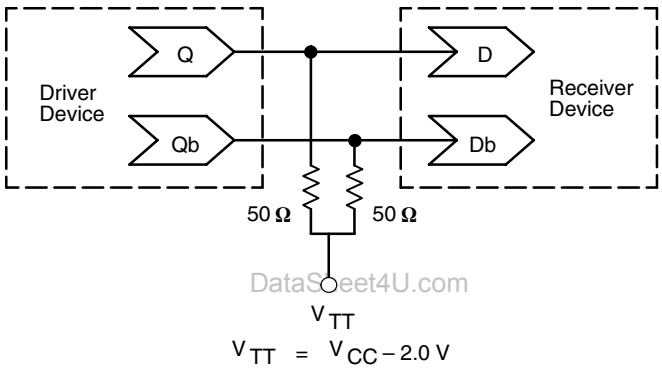


Figure 1. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405 – ECL Clock Distribution Techniques
AN1406 – Designing with PECL (ECL at +5.0 V)
AN1503 – ECLinPS I/O SPICE Modeling Kit
AN1504 – Metastability and the ECLinPS Family
AN1560 – Low Voltage ECLinPS SPICE Modeling Kit
AN1568 – Interfacing Between LVDS and ECL
AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650 – Using Wire–OR Ties in ECLinPS Designs
AN1672 – The ECL Translator Guide
AND8001 – Odd Number Counters Design
AND8002 – Marking and Date Codes
AND8020 – Termination of ECL Logic Devices

MC100EL14

5V ECL 1:5 Clock Distribution Chip

The MC100EL14 is a low skew 1:5 clock distribution chip designed explicitly for low skew clock distribution applications. The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The EL14 features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open and pulled LOW by the input pulldown resistor) the SEL pin will select the differential clock input.

The common enable ($\overline{EN}$) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock, therefore all associated specification limits are referenced to the negative edge of the clock input.

- 50 ps Output-to-Output Skew
- Synchronous Enable/Disable
- Multiplexed Clock Input
- ESD Protection: > 2 KV HBM, > 200 V MM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors on CLK, SCLK, SEL, and $\overline{EN}$.
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 303 devices

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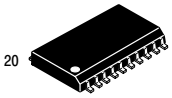
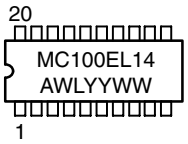


SO–20
DW SUFFIX
CASE 751D

MARKING DIAGRAM

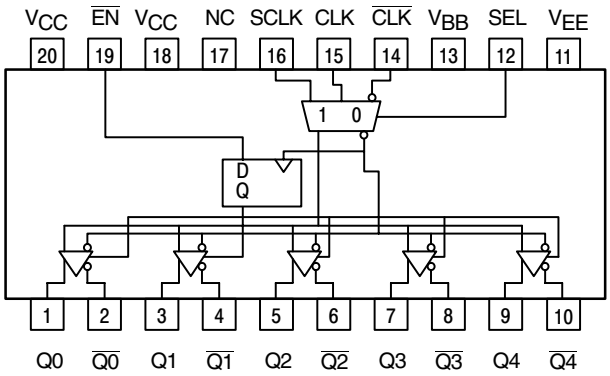


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC100EL14DW	SO–20	38 Units/Rail
MC100EL14DWR2	SO–20	1000 Units/Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} pins are tied together on the die.

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

PIN	FUNCTION
CLK, $\overline{CLK}$	ECL Diff Clock Inputs
SCLK	ECL Scan Clock Input
$\overline{EN}$	ECL Sync Enable
SEL	ECL Clock Select Input
$Q_{0–4}$, $\overline{Q_{0–4}}$	ECL Diff Clock Outputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

FUNCTION TABLE

CLK*	SCLK*	SEL*	$\overline{EN}$*	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L (1)

1. On next negative transition of CLK or SCLK

* Pins will default low when left open.

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

100EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		32	40		32	40		34	42	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Common Mode Range (Differential) (Note 3.) V_{PP} < 500 mV $V_{PP} \geq$ 500 mV	1.3 1.5		4.6 4.6	1.2 1.4		4.6 4.6	1.2 1.4		4.6 4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak–to–peak voltage lies between V_{PP}min and 1 V.

100EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		32	40		32	40		34	42	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Common Mode Range (Differential) (Note 3.) V_{PP} < 500 mV $V_{PP} \geq$ 500 mV	–3.7 –3.5		–0.4 –0.4	–3.8 –3.6		–0.4 –0.4	–3.8 –3.6		–0.4 –0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak–to–peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Prop CLK to Q (Diff) Delay CLK to Q (SE) SCLK to Q	520 470 470		720 770 770	580 530 530	680 680 680	780 830 830	630 580 580		830 880 880	ps
t_{SKEW}	Part-to-Part Skew Within-Device Skew (Note 9.)			200 50			200 50			200 50	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_S	Setup Time $\overline{EN}$	0			0			0			ps
t_H	Hold Time $\overline{EN}$	0			0			0			ps
V_{PP}	Input Swing (Note 10.)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	230		500	230		500	230		500	ps

1. V_{EE} can vary +0.8 V / –0.5 V.
9. Skews are specified for identical LOW-to-HIGH or HIGH-to-LOW transitions.
10. $V_{PP(min)}$ is the minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

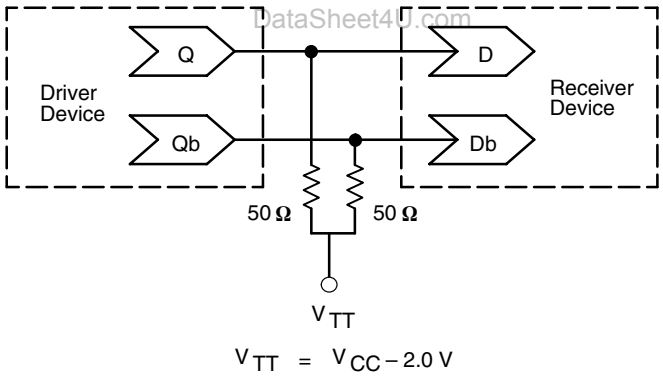


Figure 1. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10EL15, MC100EL15

5V ECL 1:4 Clock Distribution Chip

The MC10EL/100EL15 is a low skew 1:4 clock distribution chip designed explicitly for low skew clock distribution applications. The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The EL15 features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open and pulled LOW by the input pulldown resistor) the SEL pin will select the differential clock input.

The common enable ($\overline{EN}$) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock, therefore all associated specification limits are referenced to the negative edge of the clock input.

The 100 series contains temperature compensation.

- 50 ps Output-to-Output Skew
- Synchronous Enable/Disable
- Multiplexed Clock Input
- ESD Protection: > 1 KV HBM, > 100 V MM
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors on CLKs, SCLK, SEL, and $\overline{EN}$.
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 103 devices

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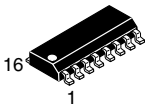
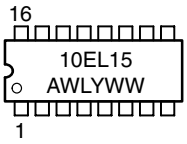
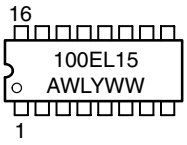
MARKING DIAGRAMS



SO–16
D SUFFIX
CASE 751B



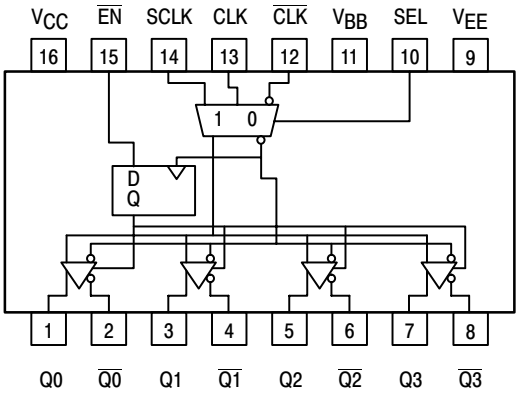
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week



ORDERING INFORMATION

Device	Package	Shipping
MC10EL15D	SO–16	48 Units / Rail
MC10EL15DR2	SO–16	2500 Units / Reel
MC100EL15D	SO–16	48 Units / Rail
MC100EL15DR2	SO–16	2500 Units / Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
CLK, $\overline{CLK}$	ECL Diff Clock Inputs
SCLK	ECL Scan Clock Input
$\overline{EN}$	ECL Sync Enable
SEL	ECL Clock Select Input
$Q_{0–3}$, $\overline{Q_{0–3}}$	ECL Diff Clock Outputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

FUNCTION TABLE

CLK*	SCLK*	SEL*	$\overline{EN}$*	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L(1)

1. On next negative transition of CLK or SCLK

* Pins will default low when left open.

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	16 SOIC 16 SOIC	130 75	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	16 SOIC	33 to 36	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		25	35		25	35		25	35	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3770		4110	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage (Single Ended)	3050		3500	3050		3520	3050		3555	mV
V_{BB}	Output Voltage Reference	3.57		3.7	3.65		3.75	3.69		3.81	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.5		4.6	2.5		4.6	2.5		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.06 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

10EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		25	35		25	35		25	35	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1080	–990	–890	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1800	–1650	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1230		–890	–1130		–810	–1060		–720	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1950		–1500	–1950		–1480	–1950		–1445	mV
V_{BB}	Output Voltage Reference	–1.43		–1.30	–1.35		–1.25	–1.31		–1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.5		–0.4	–2.5		–0.4	–2.5		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.06 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

100EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		25	35		25	35		25	38	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.5		4.6	2.5		4.6	2.5		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

100EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		25	35		25	35		25	38	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.5		–0.4	–2.5		–0.4	–2.5		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay CLK to Q (Diff) CLK to Q (SE) SCLK to Q	 460 410 410		 660 710 710	 470 420 420		 670 720 720	 500 450 470		 700 750 750	ps
t_{SKEW}	Part-to-Part Skew Within-Device Skew (Note 2.)			200 50			200 50			200 50	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_S	Setup Time $\overline{EN}$	150			150			150			ps
t_H	Hold Time $\overline{EN}$	400			400			400			ps
V_{PP}	Input Swing (Note 3.)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	325		575	325		575	325		575	ps

1. 10 Series: V_{EE} can vary +0.06 V / –0.5 V.
   100 Series: V_{EE} can vary +0.8 V / –0.5 V.
2. Skews are specified for identical LOW–to–HIGH or HIGH–to–LOW transitions.
3. $V_{PP(}$min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

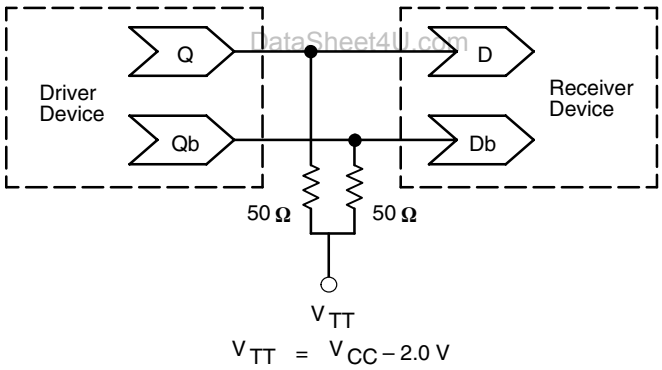


Figure 1. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10EL16, MC100EL16

5V ECL Differential Receiver

The MC10EL/100EL16 is a differential receiver. The device is functionally equivalent to the E116 device with higher performance capabilities. With output transition times significantly faster than the E116, the EL16 is ideally suited for interfacing with high frequency sources.

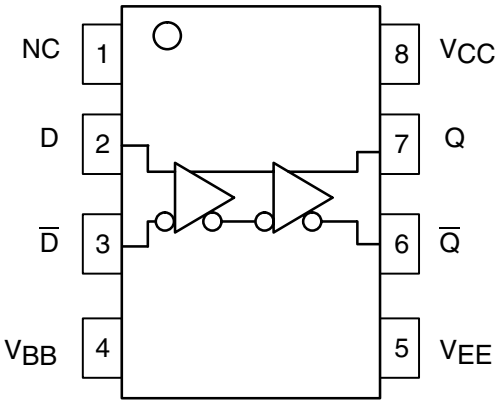
The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

Under open input conditions (pulled to V_{EE}) internal input clamps will force the Q output LOW.

The 100 Series contains temperature compensation.

- 190 ps Propagation Delay
- ESD Protection: > 1 KV HBM, > 100 V MM
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 47 devices

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
D, $\overline{D}$	ECL Data Inputs
Q, $\overline{Q}$	ECL Data Outputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

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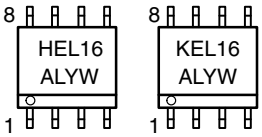
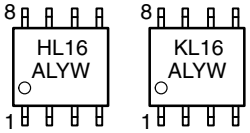
MARKING DIAGRAMS*

SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10EL16D	SO–8	98 Units/Rail
MC10EL16DR2	SO–8	2500 Tape & Reel
MC100EL16D	SO–8	98 Units/Rail
MC100EL16DR2	SO–8	2500 Tape & Reel
MC10EL16DT	TSSOP–8	98 Units/Rail
MC10EL16DTR2	TSSOP–8	2500 Tape & Reel
MC100EL16DT	TSSOP–8	98 Units/Rail
MC100EL16DTR2	TSSOP–8	2500 Tape & Reel

October, 2000 – Rev. 3
Publication Order Number:
MC10EL16/D

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		18	22		18	22		18	22	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3770		4110	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage (Single Ended)	3050		3500	3050		3520	3050		3555	mV
V_{BB}	Output Voltage Reference	3.57		3.7	3.65		3.75	3.69		3.81	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.5		4.6	2.5		4.6	2.5		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.25 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

10EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		18	22		18	22		18	22	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1080	–990	–890	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1800	–1650	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1230		–890	–1130		–810	–1060		–720	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1950		–1500	–1950		–1480	–1950		–1445	mV
V_{BB}	Output Voltage Reference	–1.43		–1.30	–1.35		–1.25	–1.31		–1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.5		–0.4	–2.5		–0.4	–2.5		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.25 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

100EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		18	22		18	22		21	26	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.5		4.6	2.5		4.6	2.5		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

100EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		18	22		18	22		21	26	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.5		–0.4	–2.5		–0.4	–2.5		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output (Diff) (SE)	 125 75	 250 250	 375 425	 175 125	 250 250	 325 375	 205 155	 280 280	 355 405	ps
t_{SKEW}	Duty Cycle Skew (Diff) (Note 2.)		5	20		5	20		5	20	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 3.)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	100	190	350	100	190	350	100	190	350	ps

1. 10 Series: V_{EE} can vary +0.25 V / –0.5 V.
   100 Series: V_{EE} can vary +0.8 V / –0.5 V.
2. Duty cycle skew is the difference between a TPLH and TPHL propagation delay through a device.
3. $V_{PP(}$min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

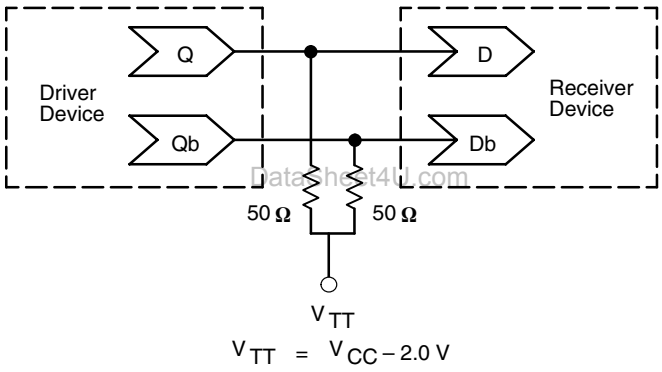


Figure 1. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC100EL17

5V ECL Quad Differential Receiver

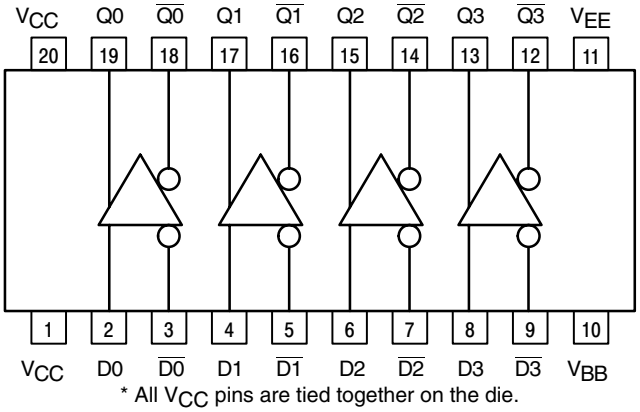
The MC100EL17 is a low-voltage, quad differential receiver. The device is functionally equivalent to the E116 device

Under open input conditions, the $\overline{D}$ input will be biased at $V_{CC}/2$ and the D input will be pulled down to V_{EE}. This operation will force the Q output LOW and ensure stability.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- 325 ps Propagation Delay
- ESD Protection: > 2 KV HBM, > 100 V MM
- The 100 series contains temperature compensation
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 141 devices

LOGIC DIAGRAM AND PINOUT: 20-LEAD SOIC (Top View)



* All V_{CC} pins are tied together on the die.

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

Pins	Function
Dn, $\overline{D}$n	ECL Differential Data Inputs
Qn, $\overline{Q}$n	ECL Differential Data Outputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

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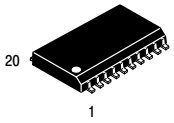
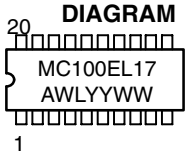


SO–20
DW SUFFIX
CASE 751D

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC100EL17DW	SO–20	38 Units/Rail
MC100EL17DWR2	SO–20	1000 Units/Reel

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

100EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		26	31		26	31		27	33	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Common Mode Range (Differential) (Note 3.) V_{PP} < 500 mV $V_{PP} \geq$ 500 mV	 1.3 1.5		 4.6 4.6	 1.2 1.4		 4.6 4.6	 1.2 1.4		 4.6 4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

100EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		26	31		26	31		27	33	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Common Mode Range (Differential) (Note 3.) V_{PP} < 500 mV $V_{PP} \geq$ 500 mV	 –3.7 –3.5		 –0.4 –0.4	 –3.8 –3.6		 –0.4 –0.4	 –3.8 –3.6		 –0.4 –0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay Diff D to Q S.E.	330 280		530 580	350 300		550 600	360 310		560 610	ps
t_{SKEW}	Skew Output–to–Output (Note 2.) Part–to–Part (Diff) (Note 2.) Duty Cycle (Diff) (Note 3.)			75 200 25			75 200 25			75 200 25	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 4.)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	280		550	280		550	280		550	ps

1. V_{EE} can vary +0.8 V / –0.5 V.
2. Skews are valid across specified voltage range, part–to–part skew is for a given temperature.
3. Duty cycle skew is the difference between a TPLH and TPHL propagation delay through a device.
4. $V_{PP(min)}$ is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

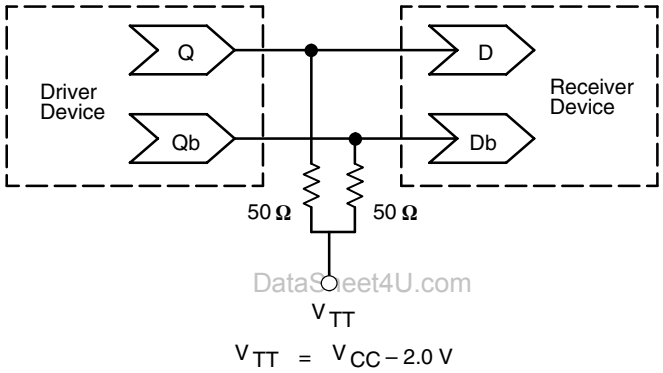


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels

AN1405 – ECL Clock Distribution Techniques

AN1406 – Designing with PECL (ECL at +5.0 V)

AN1503 – ECLinPS I/O SPICE Modeling Kit

AN1504 – Metastability and the ECLinPS Family

AN1560 – Low Voltage ECLinPS SPICE Modeling Kit

AN1568 – Interfacing Between LVDS and ECL

AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit

AN1650 – Using Wire–OR Ties in ECLinPS Designs

AN1672 – The ECL Translator Guide

AND8001 – Odd Number Counters Design

AND8002 – Marking and Date Codes

AND8020 – Termination of ECL Logic Devices

MC100EL29

5V ECL Dual Differential Data and Clock D Flip-Flop With Set and Reset

The MC100EL29 is a dual master–slave flip flop. The device features fully differential Data and Clock inputs as well as outputs. Data enters the master latch when the clock is LOW and transfers to the slave upon a positive transition on the clock input.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The differential inputs have special circuitry which ensures device stability under open input conditions. When both differential inputs are left open the D input will pull down to V_{EE} and the $\overline{D}$ input will bias around $V_{CC}/2$. The outputs will go to a defined state, however the state will be random based on how the flip flop powers up.

Both flip flops feature asynchronous, overriding Set and Reset inputs. Note that the Set and Reset inputs cannot both be HIGH simultaneously.

- 1100 MHz Flip–Flop Toggle Frequency
- 580 ps Propagation Delays
- ESD Protection: > 2 KV HBM, > 100 V MM
- Q Output will Default LOW with Inputs Open or at V_{EE}
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors on D(s), CLK(s), S(s), and R(s).
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 313 devices

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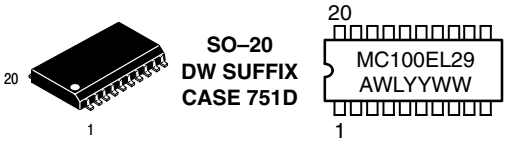
MARKING DIAGRAM



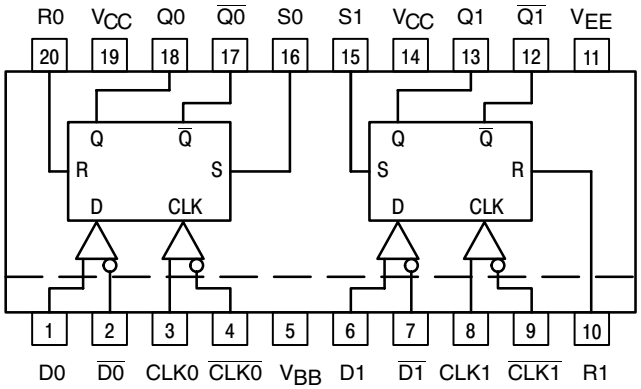
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC100EL29DW	SO–20	38 Units/Rail
MC100EL29DWR2	SO–20	1000 Units/Reel

January, 2001 – Rev. 1
Publication Order Number:
MC100EL29/D

LOGIC DIAGRAM AND PINOUT: 20-LEAD SOIC (Top View)



* All V_{CC} pins are tied together on the die.

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

PIN	FUNCTION
D0, $\overline{D0}$; D1, $\overline{D1}$	ECL Differential Data Inputs
R0–R1	ECL Reset Inputs
CLK0, $\overline{CLK0}$; CLK1, $\overline{CLK1}$	ECL Differential Clock Inputs
S0–S1	ECL Set Inputs
Q0, $\overline{Q0}$; Q1, $\overline{Q1}$	ECL Differential Data Outputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

TRUTH TABLE

R*	S*	D*	CLK*	Q	$\overline{Q}$
L	L	L	Z	L	H
L	L	H	Z	H	L
H	L	X	X	L	H
L	H	X	X	H	L
H	H	X	X	Undef	Undef

Z = LOW to HIGH Transition

* Pins will default low when left open.

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

100EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		35	50		35	50		35	50	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Common Mode Range (Differential) (Note 3.) V_{PP} < 500 mV $V_{PP} \geq$ 500 mV	1.3 1.5		4.6 4.6	1.2 1.4		4.6 4.6	1.2 1.4		4.6 4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

100EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current		35	50		35	50		35	50	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Common Mode Range (Differential) (Note 3.) V_{PP} < 500 mV $V_{PP} \geq$ 500 mV	–3.7 –3.5		–0.4 –0.4	–3.8 –3.6		–0.4 –0.4	–3.8 –3.6		–0.4 –0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay CLK to Output S, R	480 480		680 700	500 500		700 720	520 520		720 740	ps
t_S t_H	Setup Time Hold Time	0 100			0 100			0 100			ps
t_{RR}	Set/Reset Recovery	100			100			100			ps
t_{PW}	Minimum Pulse Width CLK, Set, Reset	400			400			400			ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 2.)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	280		550	280		550	280		550	ps

1. V_{EE} can vary vary +0.8 V / –0.5 V.
2. $V_{PP(}$min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

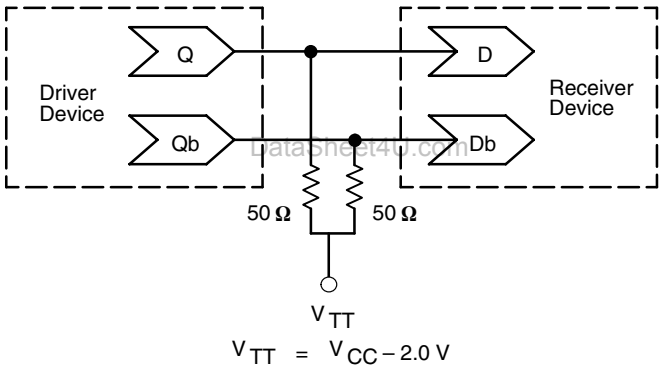


Figure 1. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC100EL30

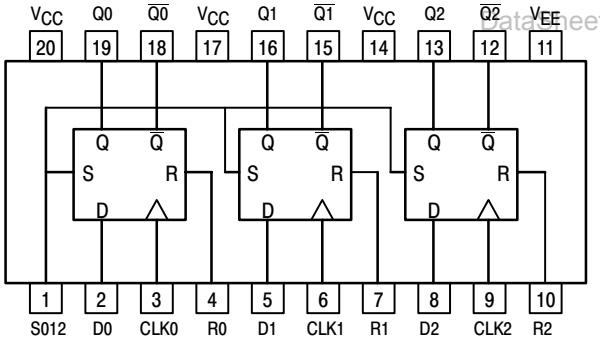
5V ECL Triple D Flip-Flop with Set and Reset

The MC100EL30 is a triple master–slave D flip flop with differential outputs. Data enters the master latch when the clock input is LOW and transfers to the slave upon a positive transition on the clock input.

In addition to a common Set input individual Reset inputs are provided for each flip flop. Both the Set and Reset inputs function asynchronous and overriding with respect to the clock inputs.

- 1200 MHz Minimum Toggle Frequency
- 450 ps Typical Propagation Delays
- ESD Protection: >2 KV HBM
- The 100 Series Contains Temperature Compensation.
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 347 devices

Logic Diagram and Pinout: 20-Lead SOIC (Top View)



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

PIN	FUNCTION
D0–D2	ECL Data Inputs
R0–R2	ECL Reset Inputs
CLK0–CLK2	ECL Clock Inputs
S012	ECL Common Set Input
Q0–Q2; $\overline{Q0}$–$\overline{Q2}$	ECL Differential Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

TRUTH TABLE

R*	S*	D*	CLK*	Q	$\overline{Q}$
L	L	L	Z	L	H
L	L	H	Z	H	L
H	L	X	X	L	H
L	H	X	X	H	L
H	H	X	X	Undef	Undef

Z = LOW to HIGH Transition
X = Don’t Care

* Pins will default low when left open.

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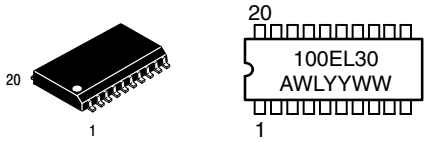
MARKING DIAGRAM*



SO–20
DW SUFFIX
CASE 751D

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100EL30DW	SO–20	38 Units/Rail
MC100EL30DWR2	SO–20	1000 Units/Reel

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		55	62		55	62		55	64	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage	3190		3525	3190		3525	3190		3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		55	62		55	62		55	64	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage	–1810		–1475	–1810		–1475	–1810		–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency	1.0			1.2			1.2			GHz
t_{PLH} t_{PHL}	Propagation Delay CLK to Output S, R	460 470		690 710	480 490		710 730	500 515		730 755	ps
t_S t_H	Setup Time Hold Time	150 200	0 100		150 200	0 100		150 200	0 100		ps
t_{RR}	Set/Reset Recovery	400	200		400	200		400	200		ps
t_{PW}	Minimum Pulse Width CLK Set, Reset	400 650			400 650			400 650			ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	280		550	280	450	550	280		550	ps

1. V_{EE} can vary +0.8 V / –0.5 V.

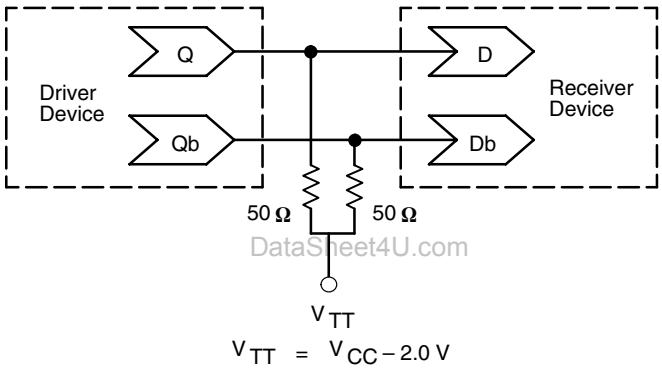


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405 – ECL Clock Distribution Techniques
AN1406 – Designing with PECL (ECL at +5.0 V)
AN1503 – ECLinPS I/O SPICE Modeling Kit
AN1504 – Metastability and the ECLinPS Family
AN1560 – Low Voltage ECLinPS SPICE Modeling Kit
AN1568 – Interfacing Between LVDS and ECL
AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650 – Using Wire–OR Ties in ECLinPS Designs
AN1672 – The ECL Translator Guide
AND8001 – Odd Number Counters Design
AND8002 – Marking and Date Codes
AND8020 – Termination of ECL Logic Devices

MC10EL31, MC100EL31

5V ECL D Flip-Flop With Set and Reset

The MC10EL/100EL31 is a D flip-flop with set and reset. The device is functionally equivalent to the E131 device with higher performance capabilities. With propagation delays and output transition times significantly faster than the E131, the EL31 is ideally suited for those applications which require the ultimate in AC performance.

Both set and reset inputs are asynchronous, level triggered signals. Data enters the master portion of the flip-flop when clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock.

The 100 Series contains temperature compensation.

- 475 ps Propagation Delay
- 2.8 GHz Toggle Frequency
- ESD Protection: > 1 KV HBM, > 100 V MM
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors on D, CLK, S, and R
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Metastability 125 ps (see Application Note AN1504)
- Transistor Count = 79 devices

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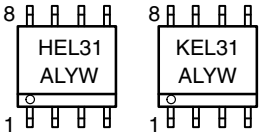
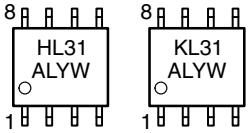
MARKING DIAGRAMS*

SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



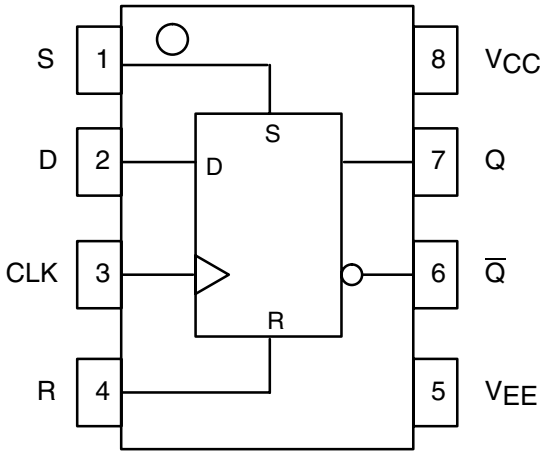
H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10EL31D	SO–8	98 Units/Rail
MC10EL31DR2	SO–8	2500 Tape & Reel
MC100EL31D	SO–8	98 Units/Rail
MC100EL31DR2	SO–8	2500 Tape & Reel
MC10EL31DT	TSSOP–8	98 Units/Rail
MC10EL31DTR2	TSSOP–8	2500 Tape & Reel
MC100EL31DT	TSSOP–8	98 Units/Rail
MC100EL31DTR2	TSSOP–8	2500 Tape & Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



TRUTH TABLE

D	S*	R*	CLK	Q
L	L	L	Z	L
H	L	L	Z	H
X	H	L	X	H
X	L	H	X	L
X	H	**H**	X	Undef

Z = LOW to HIGH Transition

* Pins will default low when left open.

PIN DESCRIPTION

PIN	FUNCTION
S	ECL Set Input
D	ECL Data Input
R	ECL Reset Input
CLK	ECL Clock Input
Q, $\overline{Q}$	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		27	32		27	32		27	32	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3770		4110	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage	3050		3500	3050		3520	3050		3555	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.25 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		27	32		27	32		27	32	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1080	–990	–890	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1800	–1650	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1230		–890	–1130		–810	–1060		–720	mV
V_{IL}	Input LOW Voltage	–1950		–1500	–1950		–1480	–1950		–1445	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.25 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		27	32		27	32		31	37	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage	3190		3525	3190		3525	3190		3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		27	32		27	32		31	37	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage	–1810		–1475	–1810		–1475	–1810		–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Toggle Frequency	2.0	2.5		2.2	2.8		2.2	2.8		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK S, R	315 295	465 455	630 630	375 355	475 465	590 590	430 400	530 510	645 645	ps
t_S t_H	Setup Time Hold Time	150 250	0 100		150 250	0 100		150 250	0 100		ps
t_{RR}	Set/Reset Recovery	400	200		400	200		400	200		ps
t_{PW}	Minimum Pulse Width CLK, Set, Reset	400			400			400			ps
tJITTER	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	100	225	350	100	225	350	100	225	350	ps

1. 10 Series: V_{EE} can vary +0.25 V / –0.5 V.
   100 Series: V_{EE} can vary +0.8 V / –0.5 V.

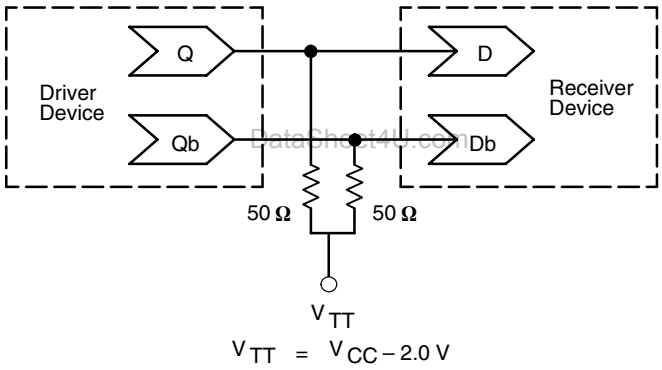


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10EL32, MC100EL32

5V ECL ÷2 Divider

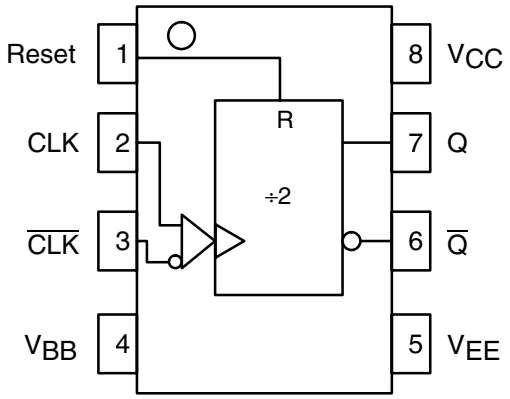
The MC10EL/100EL32 is an integrated ÷2 divider. The differential clock inputs and the V_{BB} allow a differential, single-ended or AC coupled interface to the device. The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flop will attain a random state; the reset allows for the synchronization of multiple EL32's in a system.

The 100 Series contains temperature compensation.

- 510 ps Propagation Delay
- 3.0 GHz Toggle Frequency
- ESD Protection: > 1 KV HBM, > 100 V MM
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors on CLK(s) and R.
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8",
  Oxygen Index 28 to 34
- Transistor Count = 82 devices

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
CLK, $\overline{CLK}$	ECL Clock Inputs*
Reset	ECL Asynch Reset*
Q, $\overline{Q}$	ECL Data Outputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

* Pins will default low when left open.

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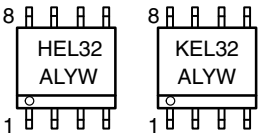
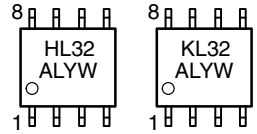
MARKING DIAGRAMS*

SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10EL32D	SO–8	98 Units/Rail
MC10EL32DR2	SO–8	2500 Tape & Reel
MC100EL32D	SO–8	98 Units/Rail
MC100EL32DR2	SO–8	2500 Tape & Reel
MC10EL32DT	TSSOP–8	98 Units/Rail
MC10EL32DTR2	TSSOP–8	2500 Tape & Reel
MC100EL32DT	TSSOP–8	98 Units/Rail
MC100EL32DTR2	TSSOP–8	2500 Tape & Reel

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		25	30		25	30		25	30	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3770		4110	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage (Single Ended)	3050		3500	3050		3520	3050		3555	mV
V_{BB}	Output Voltage Reference	3.57		3.7	3.65		3.75	3.69		3.81	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.5		4.6	2.5		4.6	2.5		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.25 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

10EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		25	30		25	30		25	30	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1080	–990	–890	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1800	–1650	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1230		–890	–1130		–810	–1060		–720	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1950		–1500	–1950		–1480	–1950		–1445	mV
V_{BB}	Output Voltage Reference	–1.43		–1.30	–1.35		–1.25	–1.31		–1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.5		–0.4	–2.5		–0.4	–2.5		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.25 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

100EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		25	30		25	30		29	35	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.5		4.6	2.5		4.6	2.5		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

100EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		25	30		25	30		29	35	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.5		–0.4	–2.5		–0.4	–2.5		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency	2.2	3.0		2.6	3.0		2.6	3.0		GHz
t_{PLH} t_{PHL}	Propagation Delay CLK to Q Reset to Q	 360 390	 500 540	 640 690	 420 440	 510 540	 600 640	 450 450	 540 550	 630 650	 ps
V_{PP}	Input Swing (Note 2.)	150		1000	150		1000	150		1000	mV
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	100	225	350	100	225	350	100	225	350	ps

1. 10 Series: V_{EE} can vary +0.25 V / –0.5 V.
   100 Series: V_{EE} can vary +0.8 V / –0.5 V.
2. V_{PP}(min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

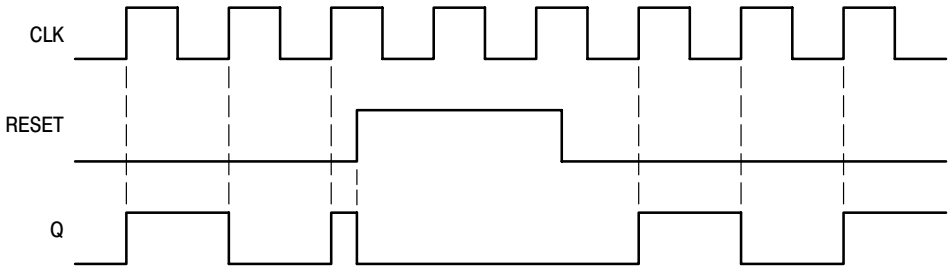


Figure 1. Timing Diagram

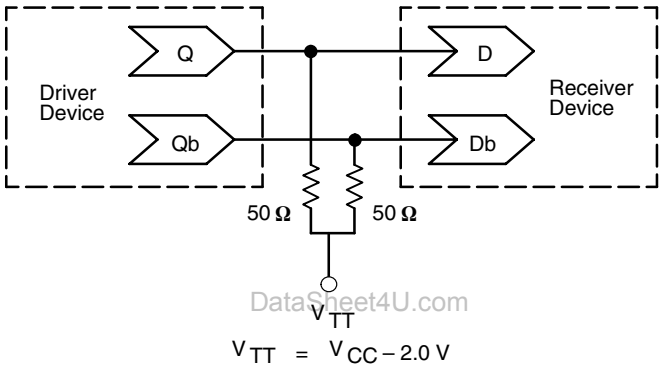


Figure 2. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10EL33, MC100EL33

5V ECL ÷4 Divider

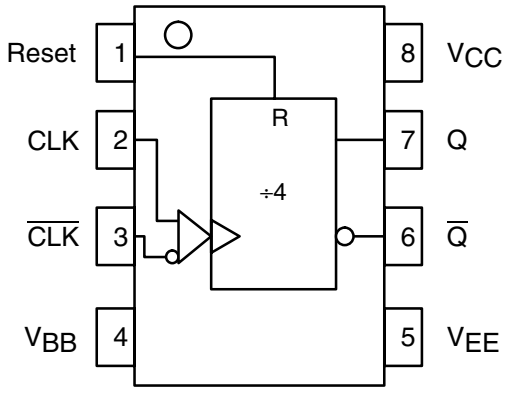
The MC10EL/100EL33 is an integrated ÷4 divider. The differential clock inputs and the V_{BB} allow a differential, single-ended or AC coupled interface to the device. The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flops will attain a random state; the reset allows for the synchronization of multiple EL33's in a system.

The 100 Series contains temperature compensation.

- 650 ps Propagation Delay
- 4.0 GHz Toggle Frequency
- ESD Protection: > 1 KV HBM, > 100 V MM
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors on CLK(s) and R.
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8",
  Oxygen Index 28 to 34
- Transistor Count = 95 devices

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
CLK, $\overline{CLK}$	ECL Clock Inputs*
Reset	ECL Asynch Reset*
Q, $\overline{Q}$	ECL Data Outputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

* Pins will default low when left open.

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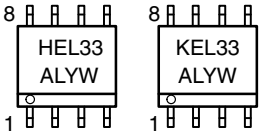
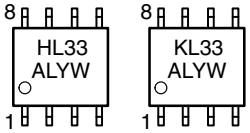
MARKING DIAGRAMS*

SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10EL33D	SO–8	98 Units/Rail
MC10EL33DR2	SO–8	2500 Tape & Reel
MC100EL33D	SO–8	98 Units/Rail
MC100EL33DR2	SO–8	2500 Tape & Reel
MC10EL33DT	TSSOP–8	98 Units/Rail
MC10EL33DTR2	TSSOP–8	2500 Tape & Reel
MC100EL33DT	TSSOP–8	98 Units/Rail
MC100EL33DTR2	TSSOP–8	2500 Tape & Reel

October, 2000 – Rev. 4
Publication Order Number:
MC10EL33/D

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		27	33		27	33		27	33	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3770		4110	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage (Single Ended)	3050		3500	3050		3520	3050		3555	mV
V_{BB}	Output Voltage Reference	3.57		3.7	3.65		3.75	3.69		3.81	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (DIfferential) (Note 3.)	2.5		4.6	2.5		4.6	2.5		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.25 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

10EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		27	33		27	33		27	33	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1080	–990	–890	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1800	–1650	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1230		–890	–1130		–810	–1060		–720	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1950		–1500	–1950		–1480	–1950		–1445	mV
V_{BB}	Output Voltage Reference	–1.43		–1.30	–1.35		–1.25	–1.31		–1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (DIfferential) (Note 3.)	–2.5		–0.4	–2.5		–0.4	–2.5		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.25 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

100EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		27	33		27	33		31	37	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (DIfferential) (Note 3.)	2.5		4.6	2.5		4.6	2.5		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

100EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		27	33		27	33		31	37	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (DIfferential) (Note 3.)	–2.5		–0.4	–2.5		–0.4	–2.5		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay CLK to Q Reset to Q	 490 310	 630 460	 770 610	 550 360	 640 460	 730 560	 590 380	 670 480	 760 580	 ps
t_{RR}	Set/Reset Recovery	400	200		400	200		400	200		ps
V_{PP}	Input Swing (Note 2.)	150		1000	150		1000	150		1000	mV
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	100	225	350	100	225	350	100	225	350	ps

1. 10 Series: V_{EE} can vary +0.25 V / –0.5 V.
   100 Series: V_{EE} can vary +0.8 V / –0.5 V.
2. V_{PP}(min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

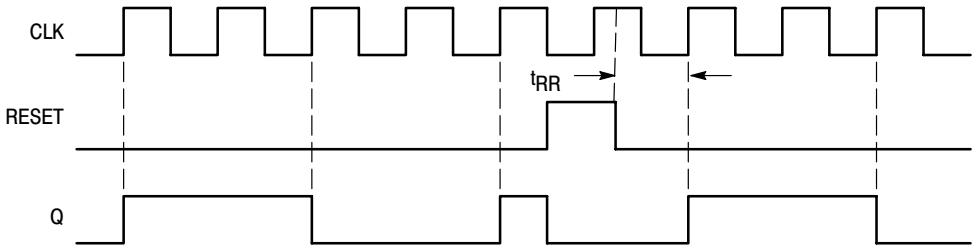


Figure 1. Timing Diagram

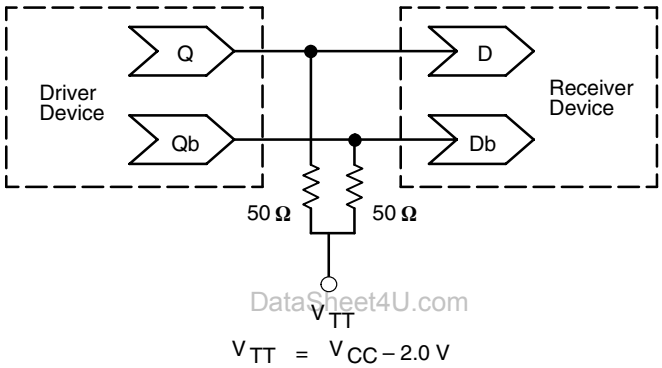


Figure 2. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
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AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10EL34, MC100EL34

5V ECL ÷2, ÷4, ÷8 Clock Generation Chip

The MC10/100EL34 is a low skew ÷2, ÷4, ÷8 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The common enable ($\overline{EN}$) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon startup, the internal flip-flops will attain a random state; the master reset (MR) input allows for the synchronization of the internal dividers, as well as multiple EL34s in a system.

The 100 Series contains temperature compensation.

- 50 ps Output-to-Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- ESD Protection: > 1 KV HBM, > 100 V MM
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors on CLK(s), $\overline{EN}$, and MR
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 191 devices

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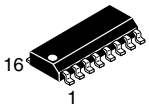
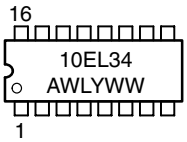
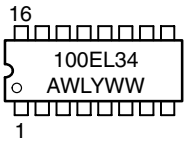
MARKING DIAGRAMS



SO–16
D SUFFIX
CASE 751B



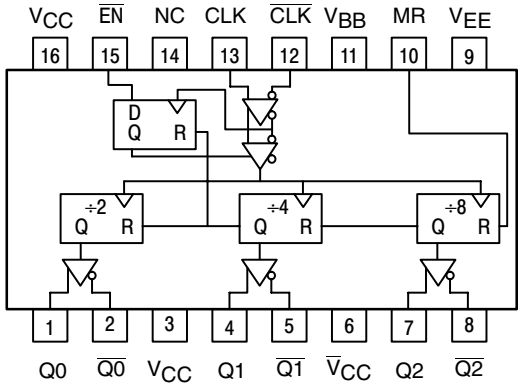
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week



ORDERING INFORMATION

Device	Package	Shipping
MC10EL34D	SO–16	48 Units / Rail
MC10EL34DR2	SO–16	2500 Units / Reel
MC100EL34D	SO–16	48 Units / Rail
MC100EL34DR2	SO–16	2500 Units / Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All V_{CC} pins are tied together on the die.

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

FUNCTION TABLE

CLK*	$\overline{EN}$*	MR*	FUNCTION
Z	L	L	Divide
ZZ	H	L	Hold $Q_{0–3}$
X	X	H	Reset $Q_{0–3}$

Z = Low-to-High Transition
ZZ = High-to-Low Transition

* Pins will default low when left open.

PIN DESCRIPTION

PIN	FUNCTION
CLK, $\overline{CLK}$	ECL Diff Clock Inputs
$\overline{EN}$	ECL Sync Enable
MR	ECL Master Reset
Q0, $\overline{Q0}$	ECL Diff ÷2 Outputs
Q1, $\overline{Q1}$	ECL Diff ÷4 Outputs
Q2, $\overline{Q2}$	ECL Diff ÷8 Outputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	16 SOIC 16 SOIC	130 75	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	16 SOIC	33 to 36	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current			39			39			39	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3770		4110	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage (Single Ended)	3050		3500	3050		3520	3050		3555	mV
V_{BB}	Output Voltage Reference	3.57		3.7	3.65		3.75	3.69		3.81	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	3.0		4.6	3.0		4.6	3.0		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.06 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V.

10EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current			39			39			39	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1080	–990	–890	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1800	–1650	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1230		–890	–1130		–810	–1060		–720	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1950		–1500	–1950		–1480	–1950		–1445	mV
V_{BB}	Output Voltage Reference	–1.43		–1.30	–1.35		–1.25	–1.31		–1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.0		–0.4	–2.0		–0.4	–2.0		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.06 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V.

100EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current			39			39			42	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.2		4.6	2.2		4.6	2.2		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V.

100EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current			39			39			42	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.8		–0.4	–2.8		–0.4	–2.8		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

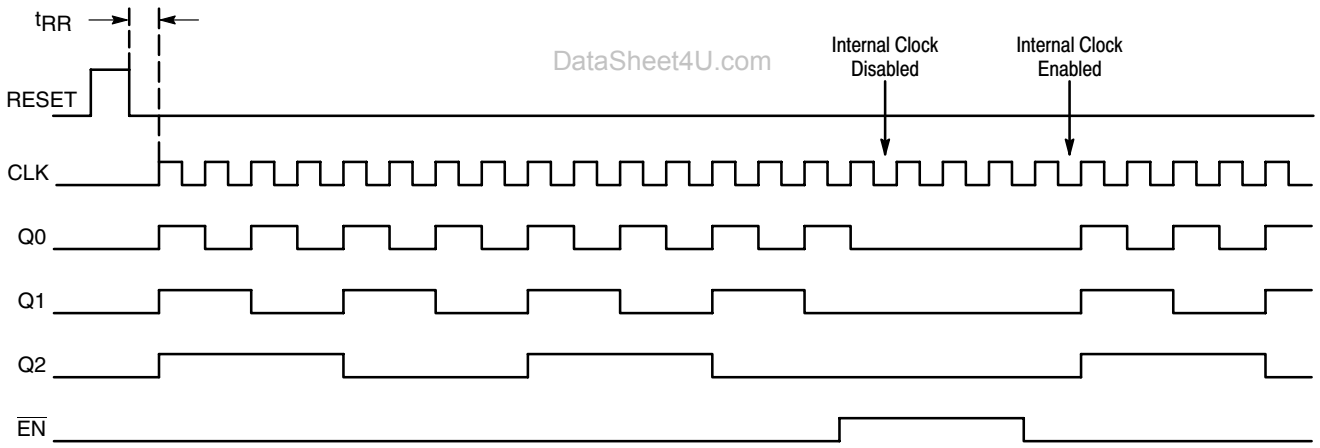
NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V.

AC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK to Q0 CLK to Q1,2 MR to Q	960 900 750		1200 1140 1060	960 900 750		1200 1140 1060	970 910 790		1210 1150 1090	ps
t_{SKEW}	Within-Device Skew (Note 2.)		100			100			100		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_S	Setup Time $\overline{EN}$	400			400			400			ps
t_H	Hold Time $\overline{EN}$	250			250			250			ps
t_{RR}	Set/Reset Recovery	400	200		400	200		400	200		ps
V_{PP}	Input Swing (Note 3.)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	275		525	275		525	275		525	ps

1. 10 Series: V_{EE} can vary +0.06 V / –0.5 V.
   100 Series: V_{EE} can vary +0.8 V / –0.5 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.
3. $V_{PP(}$min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.



The $\overline{EN}$ signal will freeze the internal clocks to the flip–flops on the first falling edge of CLK after its assertion. The internal dividers will maintain their state during the internal clock freeze and will return to clocking once the internal clocks are unfrozen. The outputs will transition to their next states in the same manner, time and relationship as they would have had the $\overline{EN}$ signal not been asserted.

Figure 1. Timing Diagram

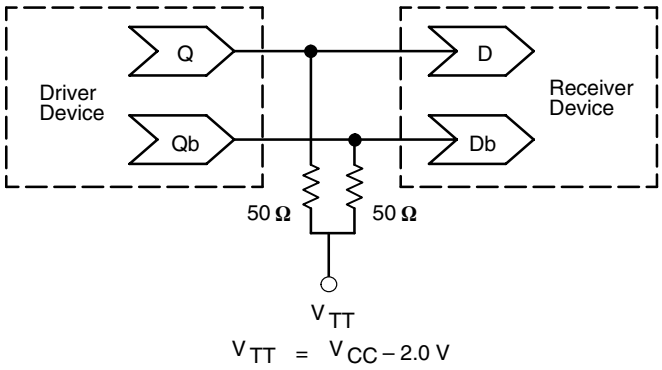


Figure 2. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10EL35, MC100EL35

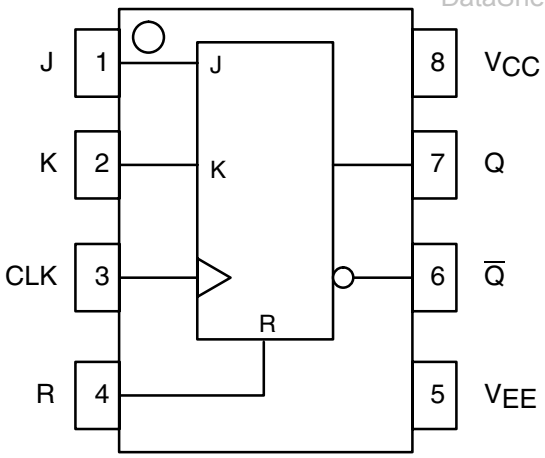
5V ECL JK Flip-Flop

The MC10EL/100EL35 is a high speed JK flip-flop. The J/K data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The reset pin is asynchronous and is activated with a logic HIGH.

The 100 Series contains temperature compensation.

- 525 ps Propagation Delay
- 2.2G Hz Toggle Frequency
- ESD Protection: > 1 KV HBM, > 100 V MM
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors on J, K, CLK, and R
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 81 devices

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
J	ECL Input
K	ECL Input
R	ECL Reset
CLK	ECL Clock Input
Q, $\overline{Q}$	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

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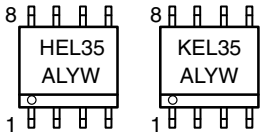
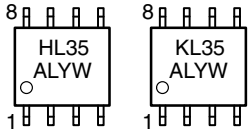
MARKING DIAGRAMS*

SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

TRUTH TABLE

J*	K*	R*	CLK	Qn+1
L	L	L	Z	Qn
L	H	L	Z	L
H	L	L	Z	H
H	H	L	Z	$\overline{Qn}$
X	X	H	X	L

Z = LOW to HIGH Transition
* Pins will default low when left open.

ORDERING INFORMATION

Device	Package	Shipping
MC10EL35D	SO–8	98 Units/Rail
MC10EL35DR2	SO–8	2500 Tape & Reel
MC100EL35D	SO–8	98 Units/Rail
MC100EL35DR2	SO–8	2500 Tape & Reel
MC10EL35DT	TSSOP–8	98 Units/Rail
MC10EL35DTR2	TSSOP–8	2500 Tape & Reel
MC100EL35DT	TSSOP–8	98 Units/Rail
MC100EL35DTR2	TSSOP–8	2500 Tape & Reel

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		27	32		27	32		27	32	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3770		4110	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage	3050		3500	3050		3520	3050		3555	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.25 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		27	32		27	32		27	32	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1080	–990	–890	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1800	–1650	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1230		–890	–1130		–810	–1060		–720	mV
V_{IL}	Input LOW Voltage	–1950		–1500	–1950		–1480	–1950		–1445	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.25 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		27	32		27	32		32	37	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		27	32		27	32		32	37	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

			–40°C			25°C			85°C			
Symbol	Characteristic		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency		1.4	2.0		1.8	2.2		1.8	2.2		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output	CLK MR	290 225	515 450	740 675	350 275	525 450	700 625	395 350	570 525	745 700	ps
t_S	Setup Time	J, K	150	0		150	0		150	0		ps
t_H	Hold Time	J, K	250	100		250	100		250	100		ps
t_{RR}	Reset Recovery		400	200		400	200		400	200		ps
t_{PW}	Minimum Pulse Width	CLK, Reset	400			400			400			ps
t_{JITTER}	Cycle–to–Cycle Jitter			TBD			TBD			TBD		ps
t_r t_f	Output Rise/Fall Times Q (20% – 80%)		100	225	350	100	225	350	100	225	350	ps

1. 10 Series: V_{EE} can vary +0.25 V / –0.5 V.
   100 Series: V_{EE} can vary +0.8 V / –0.5 V.

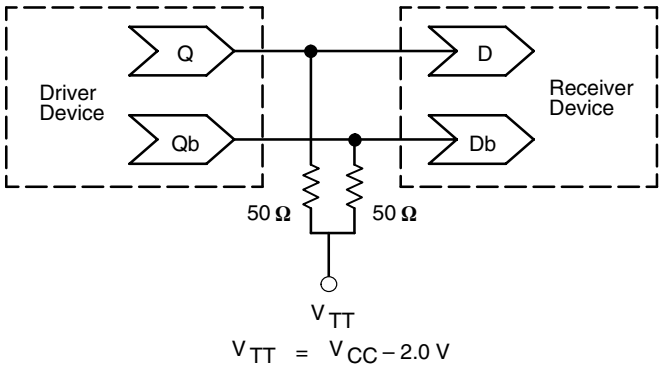


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC100EL38

5V ECL ÷2, ÷4/6 Clock Generation Chip

The MC100EL38 is a low skew ÷2, ÷4/6 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The common enable ($\overline{EN}$) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

The Phase_Out output will go HIGH for one clock cycle whenever the ÷2 and the ÷4/6 outputs are both transitioning from a LOW to a HIGH. This output allows for clock synchronization within the system.

Upon startup, the internal flip-flops will attain a random state; therefore, for systems which utilize multiple EL38s, the master reset (MR) input must be asserted to ensure synchronization. For systems which only use one EL38, the MR pin need not be exercised as the internal divider design ensures synchronization between the ÷2 and the ÷4/6 outputs of a single device.

- 50 ps Output-to-Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- ESD Protection: > 2 KV HBM, > 100 V MM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors on CLK, $\overline{EN}$, MR, and DIVSEL
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 388 devices

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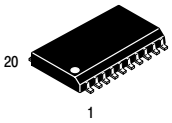
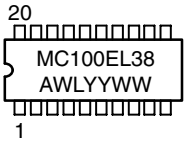
MARKING DIAGRAM



SO–20
DW SUFFIX
CASE 751D

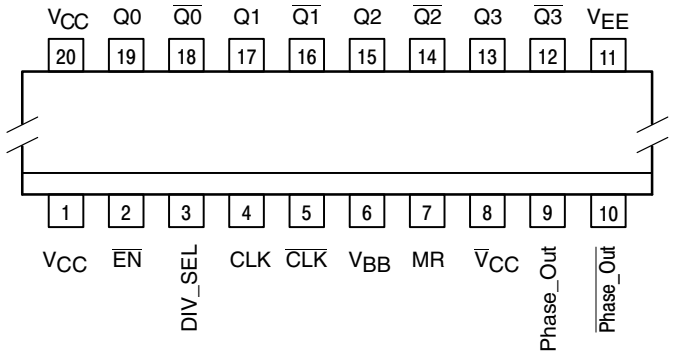


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC100EL38DW	SO–20	38 Units/Rail
MC100EL38DWR2	SO–20	1000 Units/Reel

Pinout: 20-Lead SOIC (Top View)



* All V_{CC} pins are tied together on the die.

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

FUNCTION TABLE

CLK*	$\overline{EN}$*	MR*	FUNCTION
Z	L	L	Divide
ZZ	H	L	Hold Q_{0-3}
X	X	H	Reset Q_{0-3}

Z = Low-to-High Transition
ZZ = High-to-Low Transition
* Pin will default low when left open.

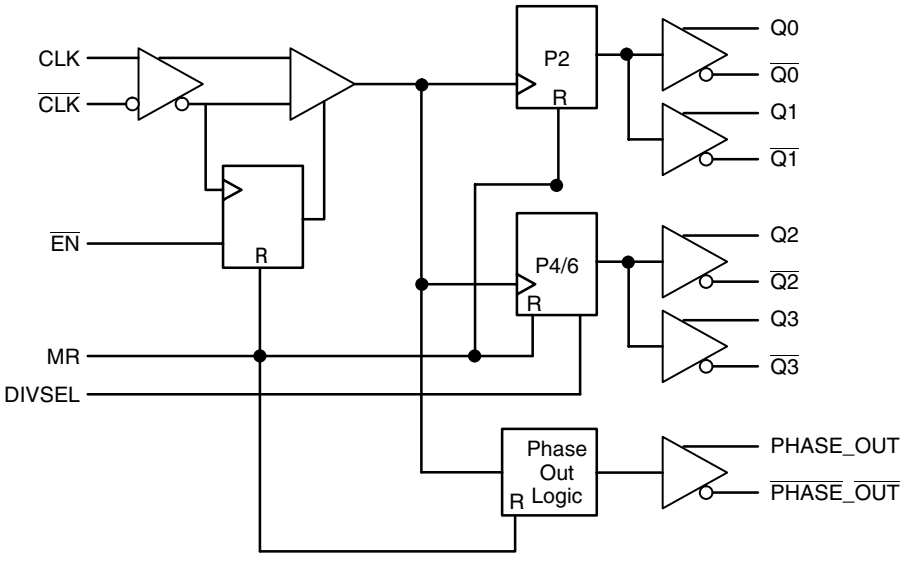
DIVSEL*	Q_2, Q_3 OUTPUTS
0	Divide by 4
1	Divide by 6

* Pin will default low when left open.

PIN DESCRIPTION

PIN	FUNCTION
CLK, $\overline{CLK}$	ECL Diff Clock Inputs
$\overline{EN}$	ECL Sync Enable
MR	ECL Master Reset
Q0, $\overline{Q0}$; Q1,$\overline{Q1}$	ECL Diff ÷2 Outputs
Q2,$\overline{Q2}$; Q3, $\overline{Q3}$	ECL Diff ÷4/6 Outputs
DIV_SEL	ECL Frequency Select Input
Phase_Out, $\overline{Phase\_Out}$	ECL Phase Sync Signal
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

LOGIC DIAGRAM



MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

100EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		50	60		50	60		54	65	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	1.65		4.45	1.65		4.45	1.65		4.45	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

100EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		50	60		50	60		54	65	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–3.35		–0.55	–3.35		–0.55	–3.35		–0.55	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay CLK → Q (Diff) to Output CLK → Q (S.E.) CLK → Phase_Out (Diff) CLK → Phase_Out (S.E.) MR → Q	760 710 800 750 510		960 1010 1000 1050 810	800 750 840 790 540		1000 1050 1040 1090 840	850 800 890 840 570		1050 1100 1090 1140 870	ps
t_{SKEW}	Within-Device Skew (Note 2.) $Q_0 - Q_3$ All			50 75			50 75			50 75	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
	Part-to-Part $Q_0 - Q_3$ (Diff) All			200 240			200 240			200 240	
t_S	Setup Time $\overline{EN} \rightarrow \overline{CLK}$ DIVSEL → CLK		150			150			150		ps
t_H	Hold Time $\overline{CLK} \rightarrow \overline{EN}$ CLK → Div_Sel		150 200			150 200			150 200		ps
V_{PP}	Input Swing (Note 3.)	150		1000	150		1000	150		1000	mV
t_{RR}	Reset Recovery Time			100			100			100	ps
t_{PW}	Minimum Pulse Width CLK MR	800 700			800 700			800 700			ps
t_r, t_f	Output Rise/Fall Times Q (20% – 80%)	280		550	280		550	280		550	ps

1. V_{EE} can vary +0.8 V / –0.5 V.
2. Skew is measured between outputs under identical transitions.
3. $V_{PP(}$min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

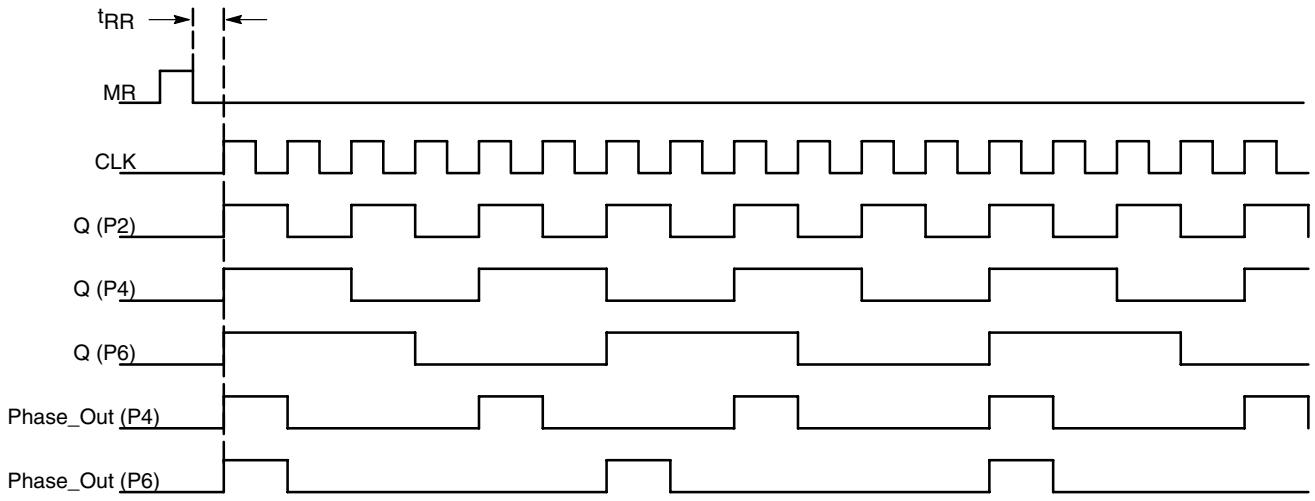


Figure 1. Timing Diagram

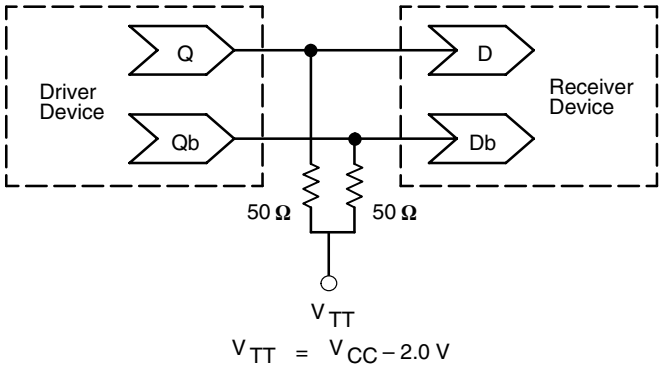


Figure 2. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC100EL39

5V ECL ÷2/4, ÷4/6 Clock Generation Chip

The MC100EL39 is a low skew ÷2/4, ÷4/6 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The common enable ($\overline{EN}$) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon startup, the internal flip-flops will attain a random state; therefore, for systems which utilize multiple EL39s, the master reset (MR) input must be asserted to ensure synchronization. For systems which only use one EL39, the MR pin need not be exercised as the internal divider design ensures synchronization between the ÷2/4 and the ÷4/6 outputs of a single device.

- 50 ps Output-to-Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- ESD Protection: > 2 KV HBM, > 100 V MM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors on $\overline{EN}$, MR, CLK(s), and DIVSEL(s)
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 419 devices

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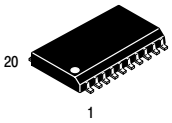
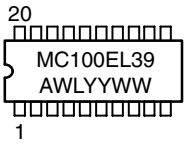
MARKING DIAGRAM



SO–20
DW SUFFIX
CASE 751D

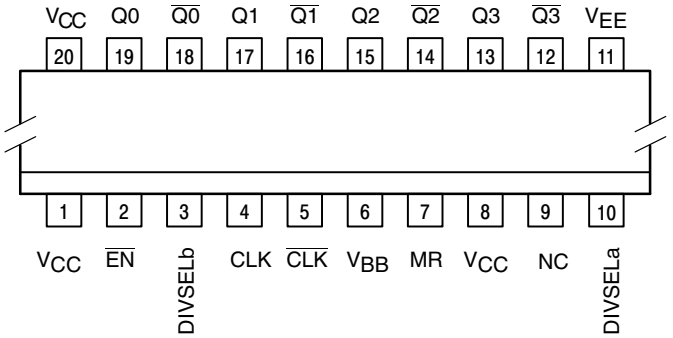


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC100EL39DW	SO–20	38 Units/Rail
MC100EL39DWR2	SO–20	1000 Units/Reel

PINOUT: 20-LEAD SOIC (Top View)



* All V_{CC} pins are tied together on the die.

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

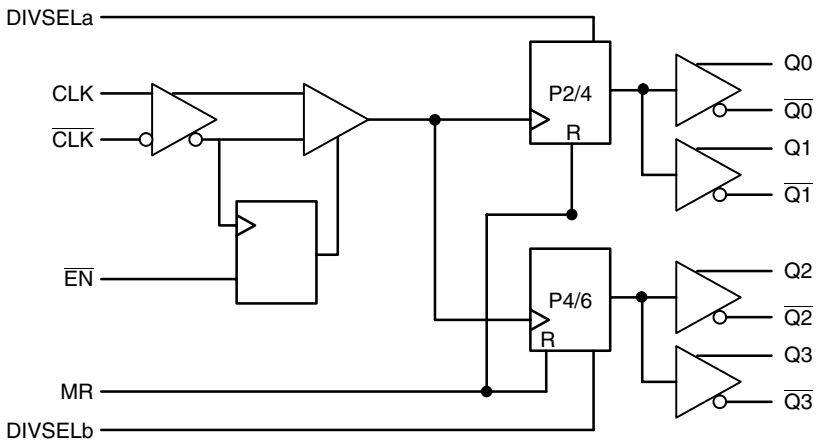
PIN	FUNCTION
CLK, $\overline{CLK}$	ECL Diff Clock Inputs
$\overline{EN}$	ECL Sync Enable
MR	ECL Master Reset
Q0, $\overline{Q0}$; Q1, $\overline{Q1}$	ECL Diff ÷2/4 Outputs
Q2, $\overline{Q2}$; Q3, $\overline{Q3}$	ECL Diff ÷4/6 Outputs
DIVSELa,	ECL Frequency Select Input
DIVSELb	ECL Frequency Select Input
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

FUNCTION TABLE

CLK*	$\overline{EN}$*	MR*	FUNCTION
Z	L	L	Divide
ZZ	H	L	Hold Q_{0-3}
X	X	H	Reset Q_{0-3}

Z = Low-to-High Transition
ZZ = High-to-Low Transition
* Pin will default low when left open.

LOGIC DIAGRAM



DIVSELa*	Q_0, Q_1 OUTPUTS
0	Divide by 2
1	Divide by 4
DIVSELb*	**Q_2, Q_3 OUTPUTS**
0	Divide by 4
1	Divide by 6

* Pin will default low when left open.

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

100EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		50	59		50	59		54	61	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Common Mode Range (Differential) (Note 3.) V_{PP} < 500 mV $V_{PP} \geq$ 500 mV	1.3 1.5		4.6 4.6	1.2 1.4		4.6 4.6	1.2 1.4		4.6 4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

100EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		50	59		50	59		54	61	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Common Mode Range (Differential) (Note 3.) V_{PP} < 500 mV $V_{PP} \geq$ 500 mV	–3.7 –3.5		–0.4 –0.4	–3.8 –3.6		–0.4 –0.4	–3.8 –3.6		–0.4 –0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency	1.0			1.0			1.0			GHz
t_{PLH} t_{PHL}	Propagation Delay CLK → Q (Diff) to Output CLK → Q (S.E.) MR → Q	760 710 600		960 1010 900	800 750 610		1000 1050 910	850 800 630		1050 1100 930	ps
t_{SKEW}	Within-Device Skew (Note 2.) $Q_0 - Q_3$			50			50			50	ps
	Part-to-Part $Q_0 - Q_3$ (Diff)			200			200			200	
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_S	Setup Time $\overline{EN} \rightarrow \overline{CLK}$ DIVSEL → CLK	250 400			250 400			250 400			ps
t_H	Hold Time $\overline{CLK} \rightarrow \overline{EN}$ CLK → Div_Sel	100 150			100 150			100 150			ps
V_{PP}	Input Swing (Note 3.)	150		1000	150		1000	150		1000	mV
t_{RR}	Reset Recovery Time			100			100			100	ps
t_{PW}	Minimum Pulse Width CLK MR	500 700			500 700			500 700			ps
t_r, t_f	Output Rise/Fall Times Q (20% – 80%)	280		550	280		550	280		550	ps

1. V_{EE} can vary +0.8 V / –0.5 V.
2. Skew is measured between outputs under identical transitions.
3. $V_{PP(}$min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

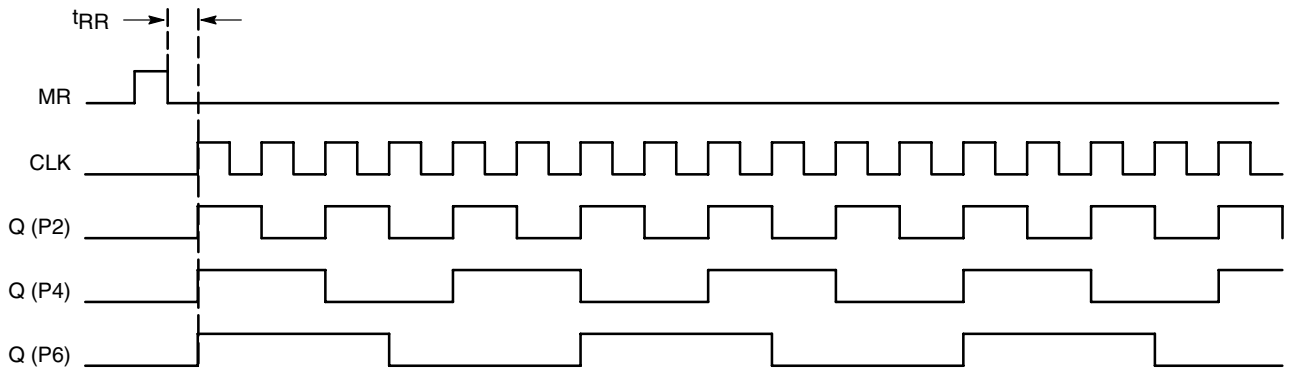


Figure 1. Timing Diagram

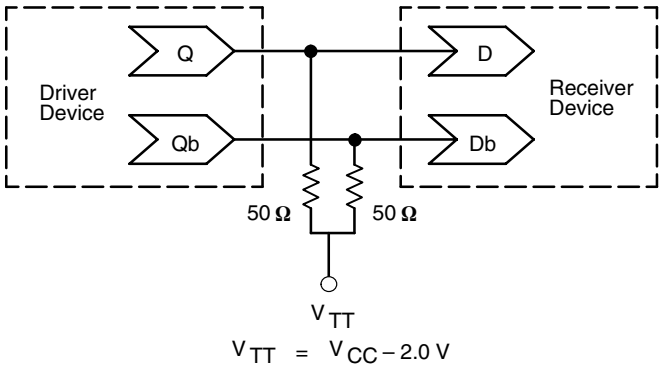


Figure 2. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10EL51, MC100EL51

5V ECL Differential Clock D Flip-Flop

The MC10EL/100EL51 is a differential clock D flip-flop with reset. The device is functionally similar to the E151 device with higher performance capabilities. With propagation delays and output transition times significantly faster than the E151 the EL51 is ideally suited for those applications which require the ultimate in AC performance.

The reset input is an asynchronous, level triggered signal. Data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The differential clock inputs of the EL51 allow the device to be used as a negative edge triggered flip-flop.

The differential input employs clamp circuitry to maintain stability under open input (pulled down to V_{EE}) conditions.

The 100 Series contains temperature compensation.

- 475 ps Propagation Delay
- 2.8 GHz Toggle Frequency
- ESD Protection: > 1 KV HBM, > 100 V MM
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors on D, R, and CLK
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 73 devices

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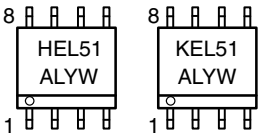
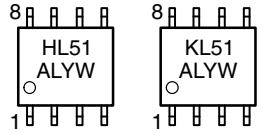
MARKING DIAGRAMS*

SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



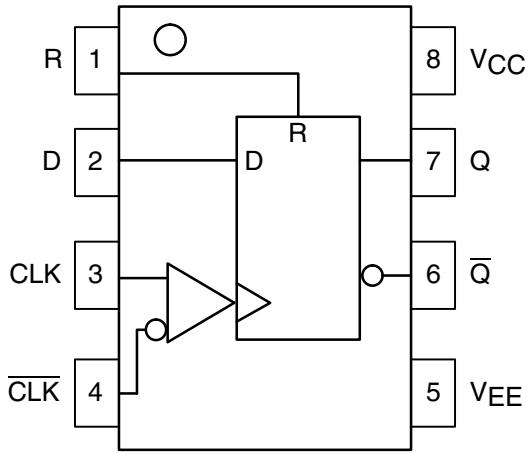
H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10EL51D	SO–8	98 Units/Rail
MC10EL51DR2	SO–8	2500 Tape & Reel
MC100EL51D	SO–8	98 Units/Rail
MC100EL51DR2	SO–8	2500 Tape & Reel
MC10EL51DT	TSSOP–8	98 Units/Rail
MC10EL51DTR2	TSSOP–8	2500 Tape & Reel
MC100EL51DT	TSSOP–8	98 Units/Rail
MC100EL51DTR2	TSSOP–8	2500 Tape & Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



TRUTH TABLE

D*	R*	CLK*	Q**
L	L	Z	L
H	L	Z	H
X	H	X	L

Z = LOW to HIGH Transition
* Pin will default low when left open.
**Pin will default low when inputs are left open.

PIN DESCRIPTION

PIN	FUNCTION
R	ECL Reset Input
D	ECL Data Input
CLK, $\overline{CLK}$	ECL Clock Inputs
Q, $\overline{Q}$	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		24	29		24	29		24	29	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3770		4110	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage (Single Ended)	3050		3500	3050		3520	3050		3555	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.5		4.6	2.5		4.6	2.5		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.25 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

10EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		24	29		24	29		24	29	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1080	–990	–890	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1800	–1650	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1230		–890	–1130		–810	–1060		–720	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1950		–1500	–1950		–1480	–1950		–1445	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.5		–0.4	–2.5		–0.4	–2.5		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.25 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

100EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		24	29		24	29		30	36	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.5		4.6	2.5		4.6	2.5		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

100EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		24	29		24	29		30	36	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.5		–0.4	–2.5		–0.4	–2.5		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency	1.8	2.8		2.2	2.8		2.2	2.8		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK R	325 305	465 455	605 605	385 355	475 465	565 565	440 410	530 510	620 620	ps
t_S	Setup Time	150	0		150	0		150	0		ps
t_H	Hold Time	250	100		250	100		250	100		ps
t_{RR}	Reset Recovery	400	200		400	200		400	200		ps
t_{PW}	Minimum Pulse Width CLK, Reset	400			400			400			ps
V_{PP}	Input Swing (Note 2.)	150		1000	150		1000	150		1000	mV
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	100	225	350	100	225	350	100	225	350	ps

1. 10 Series: V_{EE} can vary +0.25 V / –0.5 V.
   100 Series: V_{EE} can vary +0.8 V / –0.5 V.
2. $V_{PP(}$min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

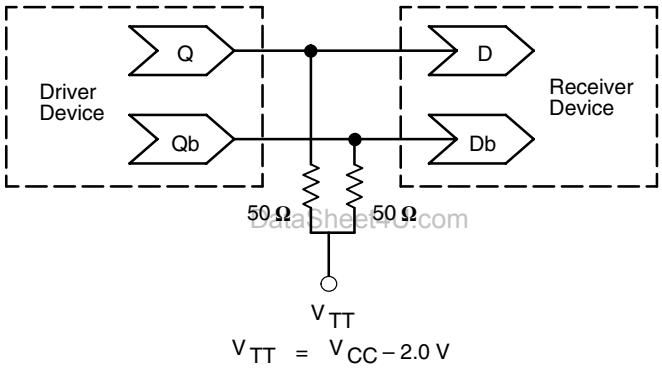


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels

AN1405 – ECL Clock Distribution Techniques

AN1406 – Designing with PECL (ECL at +5.0 V)

AN1503 – ECLinPS I/O SPICE Modeling Kit

AN1504 – Metastability and the ECLinPS Family

AN1560 – Low Voltage ECLinPS SPICE Modeling Kit

AN1568 – Interfacing Between LVDS and ECL

AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit

AN1650 – Using Wire–OR Ties in ECLinPS Designs

AN1672 – The ECL Translator Guide

AND8001 – Odd Number Counters Design

AND8002 – Marking and Date Codes

AND8020 – Termination of ECL Logic Devices

MC10EL52, MC100EL52

5V ECL Differential Data and Clock D Flip-Flop

The MC10EL/100EL52 is a differential data, differential clock D flip-flop with reset. The device is functionally equivalent to the E452 device with higher performance capabilities. With propagation delays and output transition times significantly faster than the E452, the EL52 is ideally suited for those applications which require the ultimate in AC performance.

Data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The differential clock inputs of the EL52 allow the device to also be used as a negative edge triggered device.

The EL52 employs input clamping circuitry so that under open input conditions (pulled down to V_{EE}) the outputs of the device will remain stable.

The 100 Series contains temperature compensation.

- 365 ps Propagation Delay
- 2.0 GHz Toggle Frequency
- ESD Protection: > 1 KV HBM, > 100 V MM
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors on D and CLK
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 48 devices

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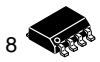
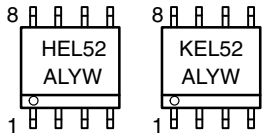
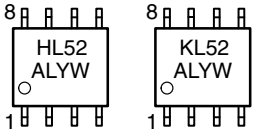
MARKING DIAGRAMS*



SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



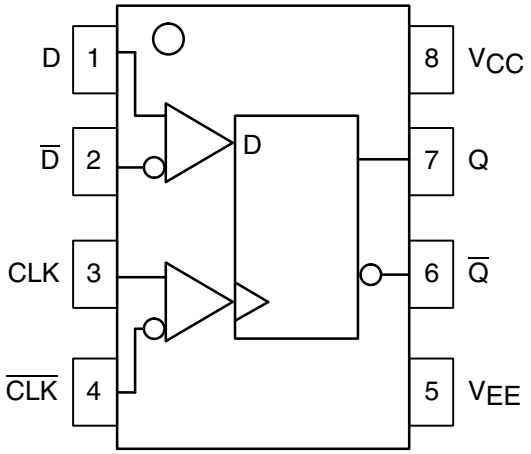
H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10EL52D	SO–8	98 Units/Rail
MC10EL52DR2	SO–8	2500 Tape & Reel
MC100EL52D	SO–8	98 Units/Rail
MC100EL52DR2	SO–8	2500 Tape & Reel
MC10EL52DT	TSSOP–8	98 Units/Rail
MC10EL52DTR2	TSSOP–8	2500 Tape & Reel
MC100EL52DT	TSSOP–8	98 Units/Rail
MC100EL52DTR2	TSSOP–8	2500 Tape & Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



TRUTH TABLE

D*	CLK*	Q
L H	Z Z	L H

Z = LOW to HIGH Transition

* Pin will default low when left open.

PIN DESCRIPTION

PIN	FUNCTION
D, $\overline{D}$	ECL Data Input
CLK, $\overline{CLK}$	ECL Clock Input
Q, $\overline{Q}$	ECL Data Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		21	25		21	25		21	25	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3770		4110	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage (Single Ended)	3050		3500	3050		3520	3050		3555	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (DIfferential) (Note 3.) D CLK	3.4 2.5		4.6 4.4	3.4 2.5		4.6 4.4	3.4 2.5		4.6 4.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}.
   V_{EE} can vary +0.25 V / –0.5 V for +25°C and +85°C. or V_{EE} can vary +0.06 V / –0.5 V for –40°C.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

10EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		21	25		21	25		21	25	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1080	–990	–890	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1800	–1650	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1230		–890	–1130		–810	–1060		–720	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1950		–1500	–1950		–1480	–1950		–1445	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (DIfferential) (Note 3.) D CLK	–1.6 –2.5		–0.4 –0.6	–1.6 –2.5		–0.4 –0.6	–1.6 –2.5		–0.4 –0.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}.
   V_{EE} can vary +0.25 V / –0.5 V for +25°C and +85°C. or V_{EE} can vary +0.06 V / –0.5 V for –40°C.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

100EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		21	25		21	25		24	29	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (DIfferential) (Note 3.) D CLK	2.6 2.5		4.6 4.2	2.6 2.5		4.6 4.2	2.6 2.5		4.6 4.2	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

100EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		21	25		21	25		24	29	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (DIfferential) (Note 3.) D CLK	–2.4 –2.5		–0.4 –0.8	–2.4 –2.5		–0.4 –0.8	–2.4 –2.5		–0.4 –0.8	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency	1.8	2.5		2.2	2.8		2.2	2.8		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK	225	335	515	275	365	465	320	410	510	ps
t_S	Setup Time	125	0		125	0		125	0		ps
t_H	Hold Time	150	50		150	50		150	50		ps
t_{PW}	Minimum Pulse Width	400			400			400			ps
V_{PP}	Input Swing (Note 2.)	150		1000	150		1000	150		1000	mV
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	100	225	350	100	225	350	100	225	350	ps

1. 10 Series: V_{EE} can vary +0.25 V / –0.5 V for +25°C and +85°C. or V_{EE} can vary +0.06 V / –0.5 V for –40°C
   100 Series: V_{EE} can vary +0.8 V / –0.5 V.
2. $V_{PP(}$min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

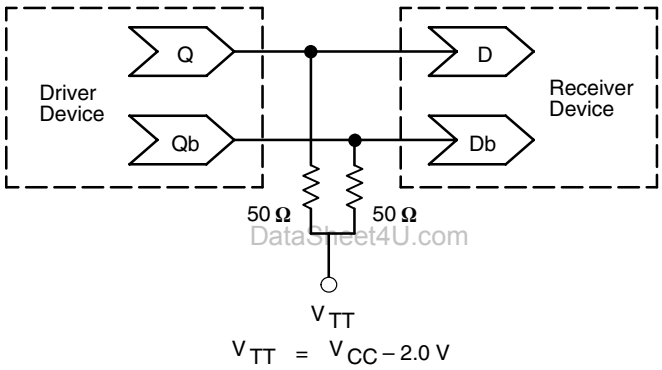


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels

AN1405 – ECL Clock Distribution Techniques

AN1406 – Designing with PECL (ECL at +5.0 V)

AN1503 – ECLinPS I/O SPICE Modeling Kit

AN1504 – Metastability and the ECLinPS Family

AN1560 – Low Voltage ECLinPS SPICE Modeling Kit

AN1568 – Interfacing Between LVDS and ECL

AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit

AN1650 – Using Wire–OR Ties in ECLinPS Designs

AN1672 – The ECL Translator Guide

AND8001 – Odd Number Counters Design

AND8002 – Marking and Date Codes

AND8020 – Termination of ECL Logic Devices

MC100EL56

5V ECL Dual Differential 2:1 Multiplexer

The MC100EL56 is a dual, fully differential 2:1 multiplexer. The differential data path makes the device ideal for multiplexing low skew clock or other skew sensitive signals. Multiple V_{BB} pins are provided to ease AC coupling input signals.

The V_{BB} pins, an internally generated voltage supply, are available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The device features both individual and common select inputs to address both data path and random logic applications.

The differential inputs have special circuitry which ensures device stability under open input conditions. When both differential inputs are left open, the D input will pull down to V_{EE}. The $\overline{D}$ input will bias around $V_{CC}/2$ forcing the Q output LOW.

- 440 ps Typical Propagation Delays
- Separate and Common Select
- ESD Protection: > 2 KV HBM, > 100 V MM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors on D(s), SEL(s), and COM_SEL
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 147 devices

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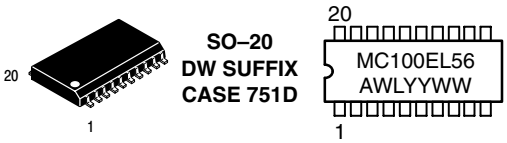
MARKING DIAGRAM

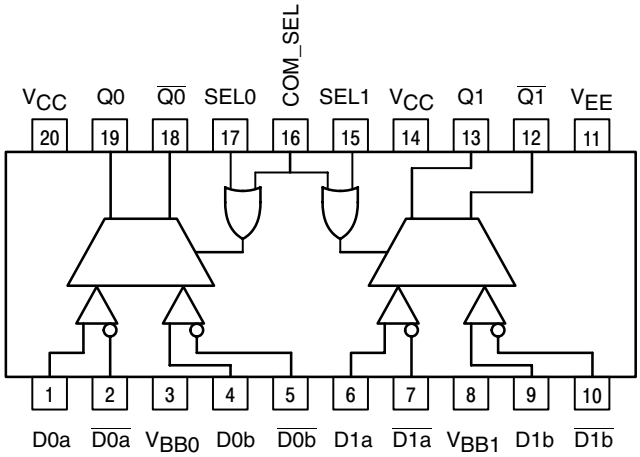


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC100EL56DW	SO–20	38 Units/Rail
MC100EL56DWR2	SO–20	1000 Units/Reel

Logic Diagram and Pinout: 20-Lead SOIC (Top View)



* All V_{CC} and V_{CCO} pins are tied together on the die.

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

TRUTH TABLE

SEL*	Data
H	a
L	b

* SEL will default low when left open.

PIN DESCRIPTION

PIN	FUNCTION
D0a–D1a, $\overline{D0a}$–$\overline{D1a}$	ECL Input Data a
D0b–D1b, $\overline{D0b}$–$\overline{D1b}$	ECL Input Data b
SEL0–SEL1	ECL Individual Select Input
COM_SEL	ECL Common Select Input
Q0–Q1	ECL True Outputs
$\overline{Q0}$–$\overline{Q1}$	ECL Inverted Outputs
V_{BB0}, V_{BB1}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

100EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		20	24		20	24		20	24	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Common Mode Range (Differential) (Note 3.)										V
	V_{PP} < 500 mV	1.3		4.6	1.2		4.6	1.2		4.6	
	$V_{PP} \geq$ 500 mV	1.5		4.6	1.4		4.6	1.4		4.6	
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

100EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		20	24		20	24		20	24	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Common Mode Range (Differential) (Note 3.)										V
	V_{PP} < 500 mV	–3.7		–0.4	–3.8		–0.4	–3.8		–0.4	
	$V_{PP} \geq$ 500 mV	–3.5		–0.4	–3.6		–0.4	–3.6		–0.4	
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output D (Diff) D (SE) SEL COMSEL	340 290 430 430		540 590 730 730	360 310 440 440		560 610 740 740	380 330 450 450		580 630 750 750	ps
t_{SKEW}	Within–Device Skew (Note 2.)		40	80		40	80		40	80	ps
t_{SKEW}	Duty Cycle Skew (Note 3.)			100			100			100	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 4.)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	200		540	200		540	200		540	ps

1. V_{EE} can vary +0.8 V / –0.5 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.
3. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.
4. $V_{PP(}$min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

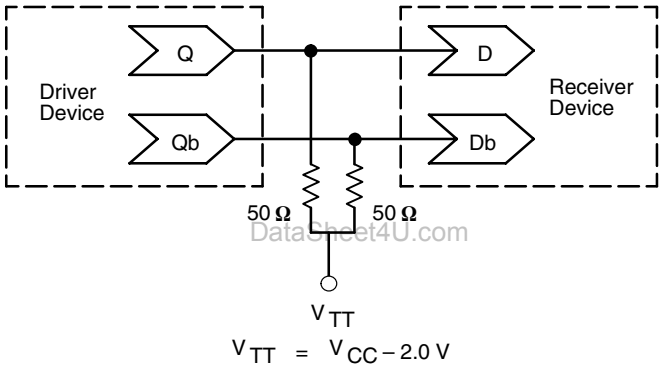


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels

AN1405 – ECL Clock Distribution Techniques

AN1406 – Designing with PECL (ECL at +5.0 V)

AN1503 – ECLinPS I/O SPICE Modeling Kit

AN1504 – Metastability and the ECLinPS Family

AN1560 – Low Voltage ECLinPS SPICE Modeling Kit

AN1568 – Interfacing Between LVDS and ECL

AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit

AN1650 – Using Wire–OR Ties in ECLinPS Designs

AN1672 – The ECL Translator Guide

AND8001 – Odd Number Counters Design

AND8002 – Marking and Date Codes

AND8020 – Termination of ECL Logic Devices

MC10EL57, MC100EL57

5V ECL 4:1 Differential Multiplexer

The MC10/100EL57 is a fully differential 4:1 multiplexer. By leaving the SEL1 line open (pulled LOW via the input pulldown resistors) the device can also be used as a differential 2:1 multiplexer with SEL0 input selecting between D0 and D1.

The SEL1 is the most significant select line. The binary number applied to the select inputs will select the same numbered data input (i.e., 00 selects D0).

Multiple V_{BB} outputs are provided for single-ended or AC coupled interfaces. The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

- Useful as Either 4:1 or 2:1 Multiplexer
- V_{BB} Output for Single-Ended Operation
- ESD Protection: > 1 KV HBM, > 100 V MM
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors on D(s) and SEL(s).
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 109 devices

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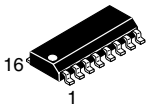
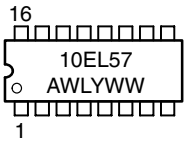
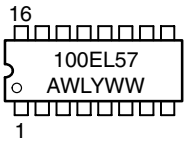
MARKING DIAGRAMS



SO–16
D SUFFIX
CASE 751B



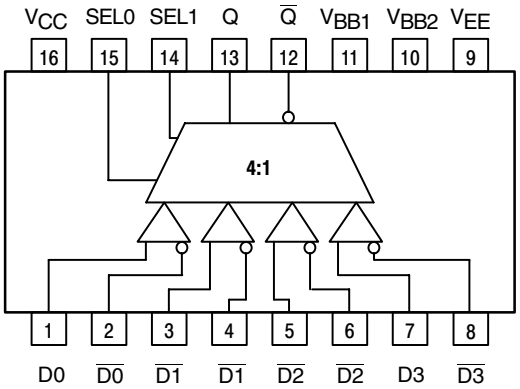
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week



ORDERING INFORMATION

Device	Package	Shipping
MC10EL57D	SO–16	48 Units / Rail
MC10EL57DR2	SO–16	2500 Units / Reel
MC100EL57D	SO–16	48 Units / Rail
MC100EL57DR2	SO–16	2500 Units / Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



FUNCTION TABLE

SEL1*	SEL0*	DATA OUT
L	L	D0
L	H	D1
H	L	D2
H	H	D3

* Pin will default low when left open.

PIN DESCRIPTION

PIN	FUNCTION
D0–3, $\overline{D0–3}$	ECL Diff Data Inputs
SEL0,1	ECL Mux Select Inputs
Q, $\overline{Q}$	ECL Data Outputs
V_{BB1}, V_{BB2}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	16 SOIC 16 SOIC	130 75	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	16 SOIC	33 to 36	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current			24			24			24	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3770		4110	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage (Single Ended)	3050		3500	3050		3520	3050		3555	mV
V_{BB}	Output Voltage Reference	3.57		3.7	3.65		3.75	3.69		3.81	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.5		4.6	2.5		4.6	2.5		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.06 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

10EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current			24			24			24	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1080	–990	–890	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1800	–1650	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1230		–890	–1130		–810	–1060		–720	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1950		–1500	–1950		–1480	–1950		–1445	mV
V_{BB}	Output Voltage Reference	–1.43		–1.30	–1.35		–1.25	–1.31		–1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.5		–0.4	–2.5		–0.4	–2.5		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.06 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

100EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current			24			24			27	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.5		4.6	2.5		4.6	2.5		4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

100EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current			24			24			27	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.5		–0.4	–2.5		–0.4	–2.5		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay DATA→Q/$\overline{Q}$ Propagation Delay SEL→Q/$\overline{Q}$	350 440		550 690	360 440		560 690	380 460		580 710	ps
t_{SKEW}	Input Skew D_n, D_m to Q			100			100			100	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 2.)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	125		375	125		375	125		375	ps

1. 10 Series: V_{EE} can vary +0.06 V / –0.5 V.
   100 Series: V_{EE} can vary +0.8 V / –0.5 V.
2. $V_{PP(}$min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

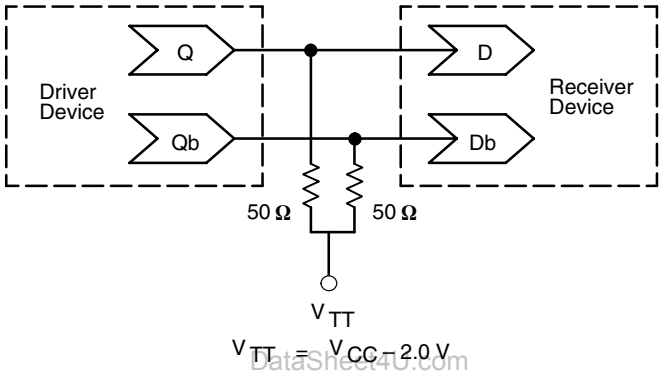


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405 – ECL Clock Distribution Techniques
AN1406 – Designing with PECL (ECL at +5.0 V)
AN1503 – ECLinPS I/O SPICE Modeling Kit
AN1504 – Metastability and the ECLinPS Family
AN1560 – Low Voltage ECLinPS SPICE Modeling Kit
AN1568 – Interfacing Between LVDS and ECL
AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650 – Using Wire–OR Ties in ECLinPS Designs
AN1672 – The ECL Translator Guide
AND8001 – Odd Number Counters Design
AND8002 – Marking and Date Codes
AND8020 – Termination of ECL Logic Devices

MC10EL58, MC100EL58

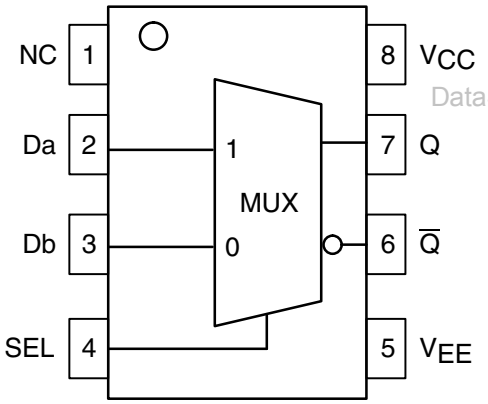
5V ECL 2:1 Multiplexer

The MC10EL/100EL58 is a 2:1 multiplexer. The device is functionally equivalent to the E158 device with higher performance capabilities. With propagation delays and output transition times significantly faster than the E158, the EL58 is ideally suited for those applications which require the ultimate in AC performance.

The 100 Series contains temperature compensation.

- 230 ps Propagation Delay
- ESD Protection: > 1 KV HBM, > 100 V MM
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors on D, D_b, and SEL
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 45 devices

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
Da, Db	ECL Data Inputs
Q, $\overline{Q}$	ECL Data Outputs
SEL	ECL Select Input
V_{CC}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

FUNCTION TABLE

SEL*	Data
H	a
L	b

* Pin will default low when left open.

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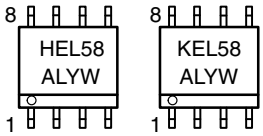
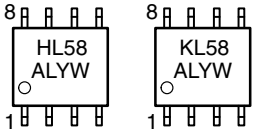
MARKING DIAGRAMS*

SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10EL58D	SO–8	98 Units/Rail
MC10EL58DR2	SO–8	2500 Tape & Reel
MC100EL58D	SO–8	98 Units/Rail
MC100EL58DR2	SO–8	2500 Tape & Reel
MC10EL58DT	TSSOP–8	98 Units/Rail
MC10EL58DTR2	TSSOP–8	2500 Tape & Reel
MC100EL58DT	TSSOP–8	98 Units/Rail
MC100EL58DTR2	TSSOP–8	2500 Tape & Reel

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		14	17		14	17		14	17	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage	3770		4110	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage	3050		3500	3050		3520	3050		3555	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.06 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

10EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		14	17		14	17		14	17	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1080	–990	–890	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1800	–1650	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage	–1230		–890	–1130		–810	–1060		–720	mV
V_{IL}	Input LOW Voltage	–1950		–1500	–1950		–1480	–1950		–1445	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.06 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		14	17		14	17		16	19	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage	3190		3525	3190		3525	3190		3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		14	17		14	17		16	19	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage	–1810		–1475	–1810		–1475	–1810		–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output D to Q SEL to Q	 60 90	 220 250	 380 410	 120 150	 230 260	 340 370	 140 170	 250 280	 360 390	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	100	225	350	100	225	350	100	225	350	ps

1. 10 Series: V_{EE} can vary +0.06 V / –0.5 V.
   100 Series: V_{EE} can vary +0.8 V / –0.5 V.

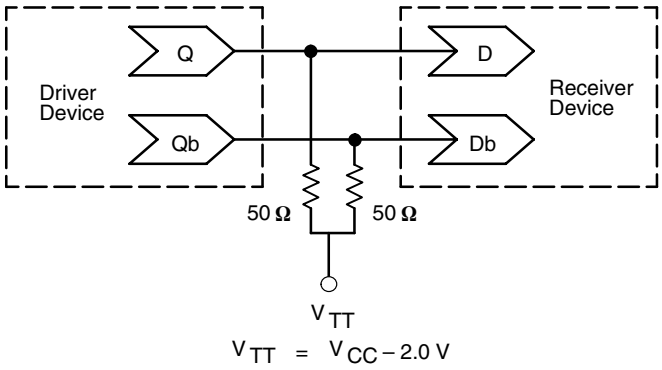


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

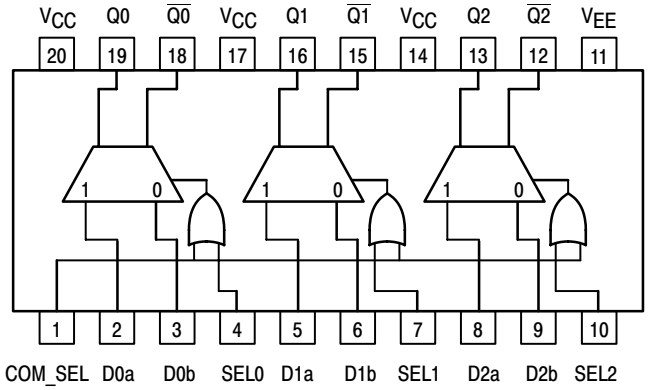
MC100EL59

5V ECL Triple 2:1 Multiplexer

The MC100EL59 is a triple 2:1 multiplexer with differential outputs. The output data of the multiplexers can be controlled individually via the select inputs or as a group via the common select input. The flexible selection scheme makes the device useful for both data path and random logic applications.

- Individual or Common Select Controls
- 500 ps Typical Propagation Delays
- ESD Protection: >2 KV HBM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 182 devices

Logic Diagram and Pinout: 20–Lead SOIC (Top View)



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

Pins	Function
D0a–D2a	ECL Input Data a*
D0b–D2b	ECL Input Data b*
SEL0–SEL2	ECL Individual Select Input*
COM_SEL	ECL Common Select Input*
Q0–Q2; $\overline{Q0}$–$\overline{Q2}$	ECL Differential Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

TRUTH TABLE

SEL*	Data
H	a
L	b

* Pins will default low when left open.

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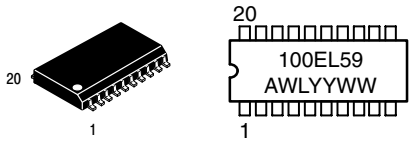
MARKING DIAGRAM*



SO–20
DW SUFFIX
CASE 751D

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100EL59DW	SO–20	38 Units/Rail
MC100EL59DWR2	SO–20	1000 Units/Reel

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		27	32		27	32		27	32	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage	3190		3525	3190		3525	3190		3525	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		27	32		27	32		27	32	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage	–1810		–1475	–1810		–1475	–1810		–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay DATA to Q/$\overline{Q}$ SEL to Q/$\overline{Q}$ COM_SEL to Q/$\overline{Q}$	340 340 340		690 690 690	340 340 340		690 690 690	340 340 340		690 690 690	ps
t_{skew}	Output–Output Skew Any D_n, D_m to Q			100			100			100	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	200		540	200		540	200		540	ps

1. V_{EE} can vary +0.8 V / –0.5 V.

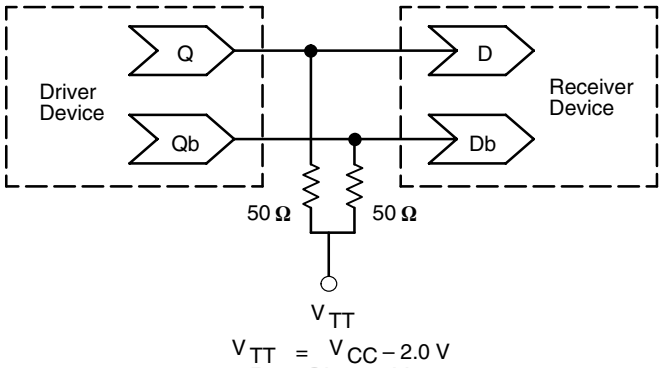


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels

AN1405 – ECL Clock Distribution Techniques

AN1406 – Designing with PECL (ECL at +5.0 V)

AN1503 – ECLinPS I/O SPICE Modeling Kit

AN1504 – Metastability and the ECLinPS Family

AN1560 – Low Voltage ECLinPS SPICE Modeling Kit

AN1568 – Interfacing Between LVDS and ECL

AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit

AN1650 – Using Wire–OR Ties in ECLinPS Designs

AN1672 – The ECL Translator Guide

AND8001 – Odd Number Counters Design

AND8002 – Marking and Date Codes

AND8020 – Termination of ECL Logic Devices

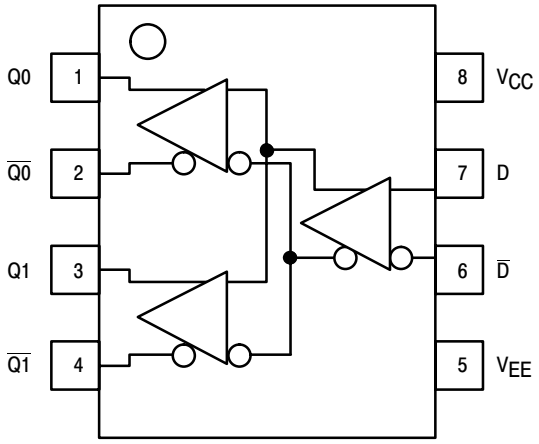
MC10EL89

5V ECL Coaxial Cable Driver

The MC10EL89 is a differential fanout gate specifically designed to drive coaxial cables. The device is especially useful in Digital Video Broadcasting applications; for this application, since the system is polarity free, each output can be used as an independent driver. The driver boasts a gain of approximately 40 and produces output swings twice as large as a standard ECL output. When driving a coaxial cable, proper termination is required at both ends of the line to minimize signal loss. The 1.6 V output swings allow for termination at both ends of the cable, while maintaining the required 800 mV swing at the receiving end of the cable. Because of the larger output swings, the device cannot be terminated into the standard –2.0 V. All of the DC parameters are tested with a 50 Ω to –3.0 V load. The driver accepts a standard differential ECL input and can run off of the Digital Video Broadcast standard –5.0 V supply.

- 375 ps Propagation Delay
- 1.6 V Output Swings
- ESD Protection: >1 KV HBM, >100 V MM
- PECL Mode Operating Range: V_{CC}= 4.2 V to 5.7 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –4.2 V to –5.7 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 31 devices

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	Function
D, $\overline{D}$	ECL Data Inputs
Q0, $\overline{Q0}$; Q1, $\overline{Q1}$	ECL Data Outputs (1.6 V_{pp})
V_{CC}	Positive Supply
V_{EE}	Negative Supply

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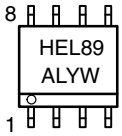
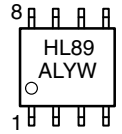
MARKING DIAGRAMS*

SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10EL89D	SO–8	98 Units / Rail
MC10EL89DR2	SO–8	2500 / Reel
MC10EL89DT	TSSOP–8	98 Units / Rail
MC10EL89DTR2	TSSOP–8	2500 / Reel

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10EL SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		23	28		23	28		23	28	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3770		4110	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage (Single Ended)	3050		3500	3050		3520	3050		3555	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.5		4.6	2.5		4.6	2.5		4.6	V
I_{IH}	Input HIGH Current		70	150		50	150		40	150	μA
I_{IL}	Input LOW Current	0.5	50		0.5	30		0.3	25		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.25 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–3 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}. V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

10EL SERIES NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		23	28		23	28		23	28	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1080	–990	–890	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1800	–1650	–1950	–1790	–1630	–1950	–1773	–1595	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1230		–890	–1130		–810	–1060		–720	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1950		–1500	–1950		–1480	–1950		–1445	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–2.5		–0.4	–2.5		–0.4	–2.5		–0.4	V
I_{IH}	Input HIGH Current		70	150		50	150		20	150	μA
I_{IL}	Input LOW Current	0.5	50		0.5	30		0.3	25		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.25 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–3 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}. V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –5.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		TBD			1.5			TBD		GBs
t_{PLH} t_{PHL}	Propagation Delay to Output	200	340	480	260	350	440	310	400	490	ps
t_{SKEW}	Within-Device Skew		5	20		5	20		5	20	ps
t_{JITTER}	Cycle–to–Cycle Jitter (PRBS) @ 1.5 GBs		TBD			400			TBD		ps
V_{PP}	Input Swing (Note 2.)	150			150			150			mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	205	330	455	205	330	455	205	330	455	ps

1. V_{EE} can vary +0.25 V / –0.5 V.
2. V_{PP}(min) is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈40.

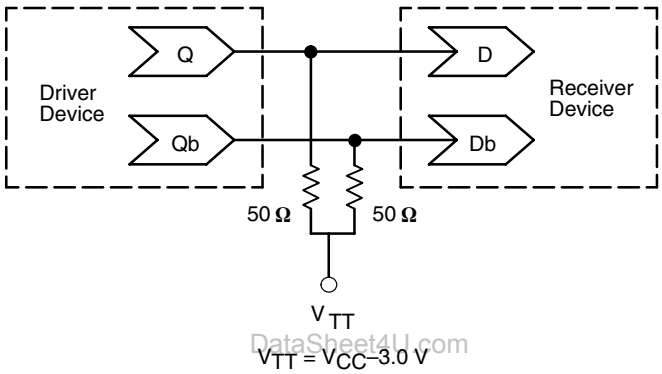


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

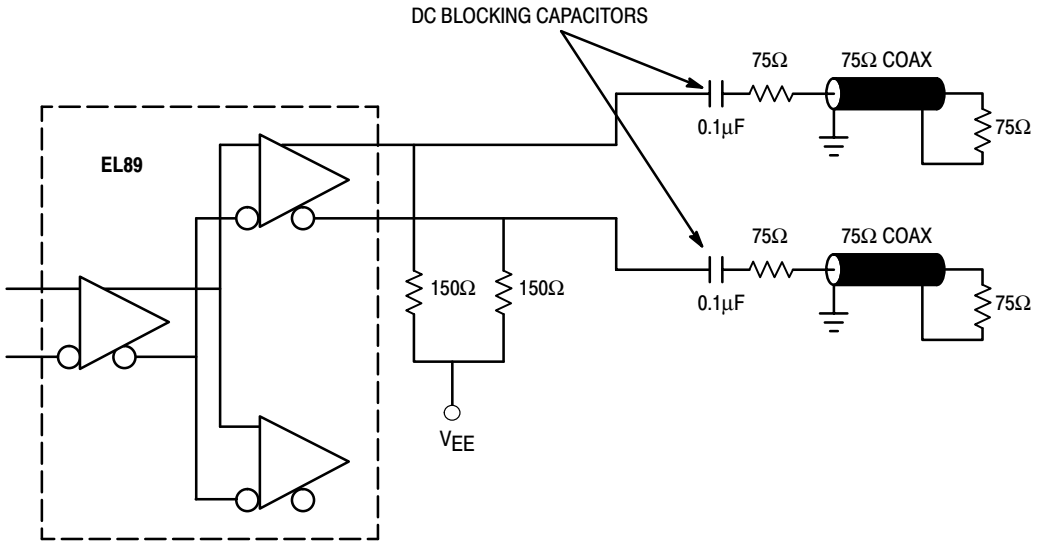


Figure 2. EL89 CATV Termination Configuration

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC100EL90

-3.3V / -5V Triple ECL Input to PECL Output Translator

The MC100EL90 is a triple ECL to PECL translator. The device receives either –3.3 V or –5 V differential ECL signals, determined by the V_{EE} supply level, and translates them to standard +5 V differential PECL output signals.

To accomplish the level translation, the EL90 requires three power rails. The V_{CC} supply should be connected to the positive supply, and the V_{EE} pin should be connected to the negative power supply. The GND pins, as expected, are connected to the system ground plane. Both V_{EE} and V_{CC} should be bypassed to ground via 0.01 μF capacitors.

Under open input conditions, the $\overline{D}$ input will be biased at $V_{EE}/2$ and the D input will be pulled to V_{EE}. This condition will force the Q output to a LOW, ensuring stability.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- 500 ps Propagation Delays
- ESD Protection: >2 KV HBM, >200 V MM
- The 100 Series Contains Temperature Compensation
- Operating Range: V_{CC}= 4.75 V to 5.25 V; V_{EE}= –3.0 V to –5.5 V; GND= 0 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 261 devices

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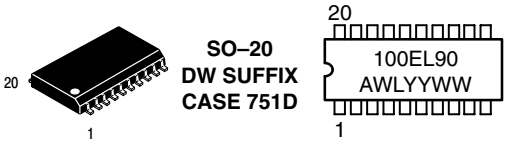
MARKING DIAGRAM*



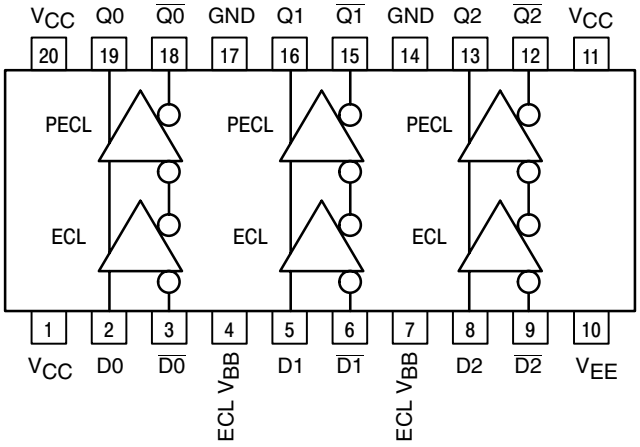
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100EL90DW	SO–20	38 Units/Rail
MC100EL90DWR2	SO–20	1000 Units/Reel

Logic Diagram and Pinout: 20-Lead SOIC (Top View)



* All V_{CC} pins are tied together on the die.

Warning: All V_{CC}, V_{EE}, and GND pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

PIN	FUNCTION
Dn, $\overline{Dn}$	ECL Inputs
Qn, $\overline{Qn}$	PECL Outputs
ECL V_{BB}	ECL Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
GND	Ground

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Power Supply	GND = 0 V		8 to 0	V
V_{EE}	NECL Power Supply	GND = 0 V		–8 to 0	V
V_I	NECL Input Voltage	GND = 0 V	$V_I \geq V_{EE}$	–6 to 0	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	ECL V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

NECL INPUT DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= –5.0 V; GND= 0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	V_{EE} Power Supply Current			8.0		6.0	8.0			8.0	mA
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
ECL V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 2.) Vpp < 500 mV Vpp ≧ 500 mV	 V_{EE}+1.3 VEE+1.5		 –0.4 –0.4	 V_{EE}+1.2 VEE+1.4		 –0.4 –0.4	 V_{EE}+1.2 VEE+1.4		 –0.4 –0.4	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5		——	0.5		——	0.5		——	μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input parameters vary 1:1 with GND. V_{EE} can vary –3.0 V / –5.5 V.
2. V_{IHCMR} min varies 1:1 with V_{EE}. V_{IHCMR} max varies 1:1 with GND.

PECL OUTPUT DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= –5.0 V; GND= 0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{CC}	V_{CC} Power Supply Current			24		20	24			26	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Output parameters vary 1:1 with V_{CC}. V_{CC} can vary ± 0.5 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CC}= 4.5 V to 5.5 V; V_{EE}= –3.0 V to –5.5 V; GND= 0 V

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		560			650			700		MHz
t_{PLH} t_{PHL}	Propagation Delay Differential D to Q S.E.	390 340		590 640	420 370		620 670	460 410		660 710	ps
t_{SKEW}	Skew Output–to–Output (Note 1) Part–to–Part (Differential) (Note 1) Duty Cycle (Differential) (Note 2)		20 25	100 200		20 25	100 200		20 25	100 200	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 3)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	230		500	230		500	230		500	ps

1. Skews are valid across specified voltage range, part–to–part skew is for a given temperature.
2. Duty cycle skew is the difference between a TPLH and TPHL propagation delay through a device.
3. V_{PP}(min) is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈40.

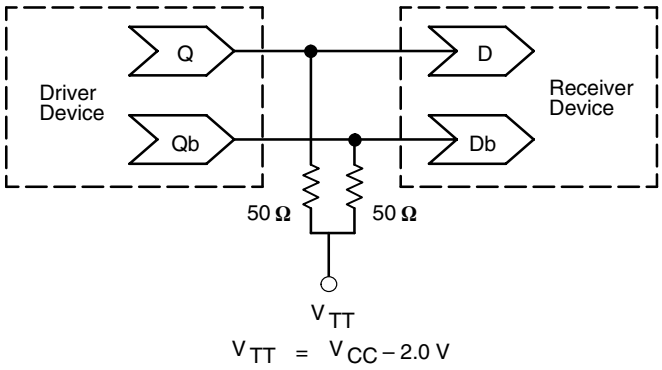


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC100EL91

3.3V / 5V Triple LVPECL / PECL Input to -5V ECL Output Translator

The MC100EL91 is a triple LVPECL / PECL input to ECL output translator. The device receives standard or low voltage differential PECL signals, determined by the V_{CC} supply level, and translates them to differential –5 V ECL output signals. (For translation to –3.3 V ECL output, see MC100LVEL91.)

To accomplish the level translation, the EL91 requires three power rails. The V_{CC} supply should be connected to the positive supply, and the V_{EE} pin should be connected to the negative power supply. The GND pins are connected to the system ground plane. Both V_{EE} and V_{CC} should be bypassed to ground via 0.01 μF capacitors.

Under open input conditions, the $\overline{D}$ input will be biased at $V_{CC}/2$ and the D input will be pulled to GND. This condition will force the Q output to a low, ensuring stability.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- 670 ps Typical Propagation Delay
- ESD Protection: >2 KV HBM
- The 100 Series Contains Temperature Compensation
- Operating Range: V_{CC}= 3.0 V to 5.25 V; V_{EE}= –4.2 V to –5.5 V; GND= 0 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at GND
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 282 devices

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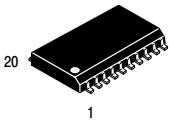
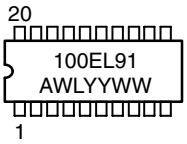
MARKING DIAGRAM*



SO–20
DW SUFFIX
CASE 751D



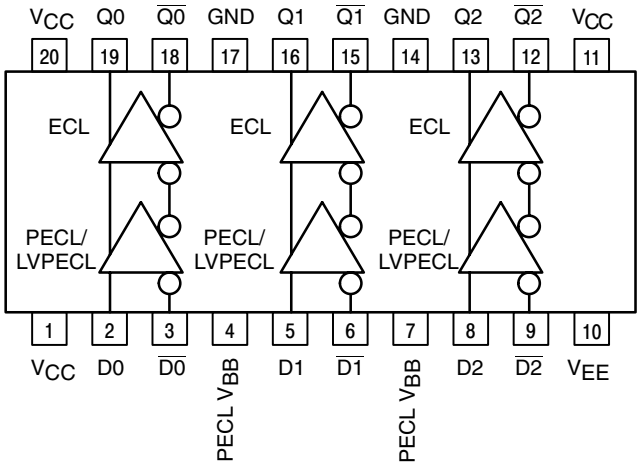
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100EL91DW	SO–20	38 Units/Rail
MC100EL91DWR2	SO–20	1000 Units/Reel

20–Lead Pinout (Top View) **and Logic Diagram**



* All V_{CC} pins are tied together on the die.

Warning: All V_{CC}, V_{EE}, and GND pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

PIN	FUNCTION
Dn, $\overline{Dn}$	PECL/LVPECL Inputs
Qn, $\overline{Qn}$	ECL Outputs
PECL V_{BB}	PECL Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
GND	Ground

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Power Supply	GND = 0 V		8 to 0	V
V_{EE}	NECL Power Supply	GND = 0 V		–8 to 0	V
V_I	PECL Input Voltage	GND = 0 V	$V_I \leq V_{CC}$	6 to 0	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	PECL V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL INPUT DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= –5.0 V; GND= 0 V (Note 1)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{CC}	V_{CC} Power Supply Current			11		6	11			11	mA
V_{IH}	Input HIGH Voltage (Single Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1490		1825	1490		1825	1490		1825	mV
LVPECL V_{BB}	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 2.)										
	Vpp < 500 mV	1.0		2.9	0.9		2.9	0.9		2.9	V
	Vpp ≧ 500 mV	1.2		2.9	1.1		2.9	1.1		2.9	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input parameters vary 1:1 with V_{CC}. V_{CC} can vary +0.5 / –0.3 V.
2. V_{IHCMR} min varies 1:1 with GND. V_{IHCMR} max varies 1:1 with V_{CC}.

PECL INPUT DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= –5.0 V; GND= 0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{CC}	V_{CC} Power Supply Current			11		6	11			11	mA
V_{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
PECL V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 2.)										V
	Vpp < 500 mV	1.0		4.6	0.9		4.6	0.9		4.6	
	Vpp ≧ 500 mV	1.2		4.6	1.1		4.6	1.1		4.6	
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input parameters vary 1:1 with V_{CC}. V_{CC} can vary ± 0.25 V.
2. V_{IHCMR} min varies 1:1 with GND. V_{IHCMR} max varies 1:1 with V_{CC}.

NECL OUTPUT DC CHARACTERISTICS V_{CC}= 3.3 V to 5.0 V; V_{EE}= –5.0 V; GND= 0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	V_{EE} Power Supply Current			28		22	28			30	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Output parameters vary 1:1 with GND. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to GND–2 volts.

AC CHARACTERISTICS V_{CC}= 3.0 V to 5.5 V; V_{EE}= –4.2 V to –5.5 V; GND= 0 V:

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay D to Q Diff S.E.	 540 490	 640 640	 740 790	 570 520	 670 670	 770 820	 610 560	 710 710	 810 860	ps
t_{SKEW}	Skew Output–to–Output (Note 4.) Part–to–Part (Diff) (Note 4.) Duty Cycle (Diff) (Note 5.)		 40 25	 100 200		 40 25	 100 200		 40 25	 100 200	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 6.)	200		1000	200		1000	200		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	320	400	580	320	400	580	320	400	580	ps

4. Skews are valid across specified voltage range, part–to–part skew is for a given temperature.
5. Duty cycle skew is the difference between a TPLH and TPHL propagation delay through a device.
6. V_{PP}(min) is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈40.

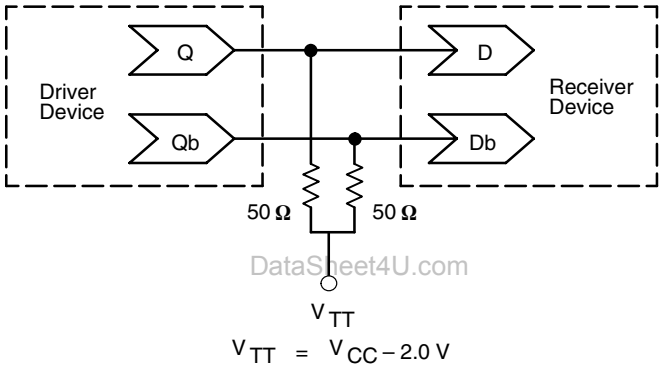


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels

AN1405 – ECL Clock Distribution Techniques

AN1406 – Designing with PECL (ECL at +5.0 V)

AN1503 – ECLinPS I/O SPICE Modeling Kit

AN1504 – Metastability and the ECLinPS Family

AN1560 – Low Voltage ECLinPS SPICE Modeling Kit

AN1568 – Interfacing Between LVDS and ECL

AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit

AN1650 – Using Wire–OR Ties in ECLinPS Designs

AN1672 – The ECL Translator Guide

AND8001 – Odd Number Counters Design

AND8002 – Marking and Date Codes

AND8020 – Termination of ECL Logic Devices

MC10ELT20, MC100ELT20

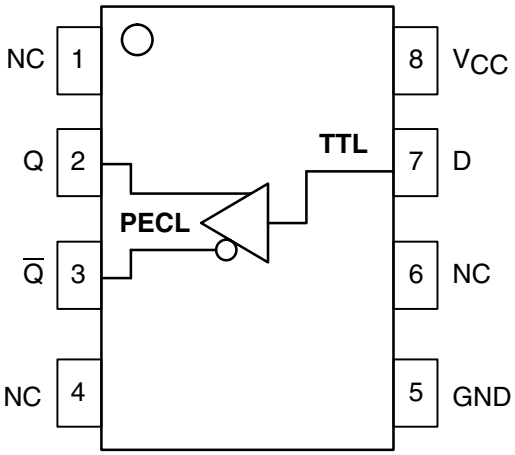
5V TTL to Differential PECL Translator

The MC10ELT/100ELT20 is a TTL to differential PECL translator. Because PECL (Positive ECL) levels are used, only +5 V and ground are required. The small outline 8-lead package and the single gate of the ELT20 makes it ideal for those applications where space, performance and low power are at a premium.

The 100 Series contains temperature compensation.

- 1.2 ns Typical Propagation Delay
- PNP TTL Inputs for Minimal Loading
- Flow Through Pinouts
- ESD Protection: >4 KV HBM, >200 V MM
- Operating Range: V_{CC}= 4.75 V to 5.25 V with GND= 0 V
- No Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 51 devices

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
Q, $\overline{Q}$	PECL Differential Outputs*
D	TTL Input
V_{CC}	Positive Supply
GND	Ground
NC	No Connect

* Output state undetermined when inputs are open.

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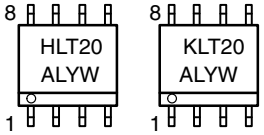
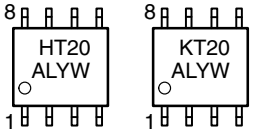
MARKING DIAGRAMS*

SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10ELT20D	SO–8	98 Units/Rail
MC10ELT20DR2	SO–8	2500 Tape & Reel
MC100ELT20D	SO–8	98 Units/Rail
MC100ELT20DR2	SO–8	2500 Tape & Reel
MC10ELT20DT	TSSOP–8	98 Units/Rail
MC10ELT20DTR2	TSSOP–8	2500 Tape & Reel
MC100ELT20DT	TSSOP–8	98 Units/Rail
MC100ELT20DTR2	TSSOP–8	2500 Tape & Reel

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Positive Power Supply	GND = 0 V		7	V
V_{IN}	Input Voltage	GND = 0 V	$V_I \leq V_{CC}$	7	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10ELT SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; GND= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{CC}	Power Supply Current			16			16			16	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Output parameters vary 1:1 with V_{CC}. V_{CC} can vary ± 0.25 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100ELT SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; GND= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{CC}	Power Supply Current			16			16			16	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Output parameters vary 1:1 with V_{CC}. V_{CC} can vary ± 0.25 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

TTL INPUT DC CHARACTERISTICS V_{CC} = 4.75V to 5.25V; T_A = –40°C to 85°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V			20	μA
I_{IHH}	Input HIGH Current	V_{IN} = 7.0 V			100	μA
I_{IL}	Input LOW Current	V_{IN} = 0.5 V			–0.6	mA
V_{IK}	Input Clamp Diode Voltage	I_{IN} = –18 mA			–1.2	V
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V

AC CHARACTERISTICS V_{CC}= 4.75 V to 5.25 V; GND= 0.0 V

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency	100			100			100			MHz
t_{PLH}	Propagation Delay (Note 1) 1.5 V to 50%	0.6		1.2	0.9	1.2	1.5	0.6		1.35	ns
t_{PHL}	Propagation Delay (Note 1) 1.5 V to 50%	0.4		1.0	0.5	0.8	1.1	0.7		1.30	ns
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r/t_f	Output Rise/Fall Time (20–80%)	0.15		1.5	0.15		1.5	0.15		1.5	ns

1. Specifications for standard TTL input signal.

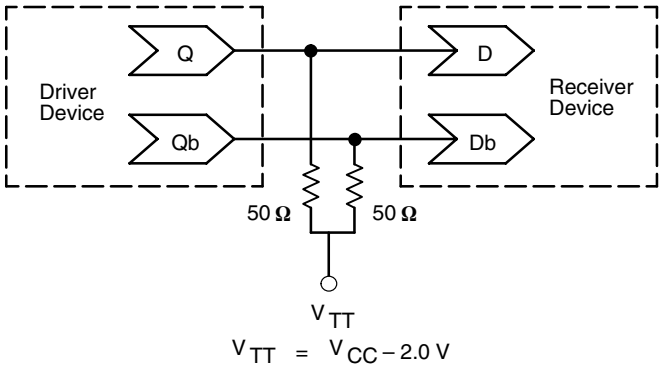


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10ELT21, MC100ELT21

5V Differential PECL to TTL Translator

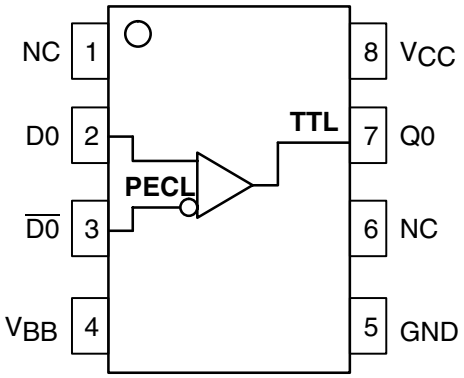
The MC10ELT/100ELT21 is a differential PECL to TTL translator. Because PECL (Positive ECL) levels are used, only +5 V and ground are required. The small outline 8-lead package and the single gate of the ELT21 makes it ideal for those applications where space, performance and low power are at a premium.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

- 3.5 ns Typical Propagation Delay
- 24 mA TTL Output
- Flow Through Pinouts
- ESD Protection: >2 KV HBM
- Operating Range: V_{CC}= 4.75 V to 5.25 V with GND= 0 V
- Q Output Will Default High with Inputs Left Open or < 1.3 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 81 devices

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
Q0	TTL Output
D0, $\overline{D0}$	PECL Differential Inputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
GND	Ground
NC	No Connect

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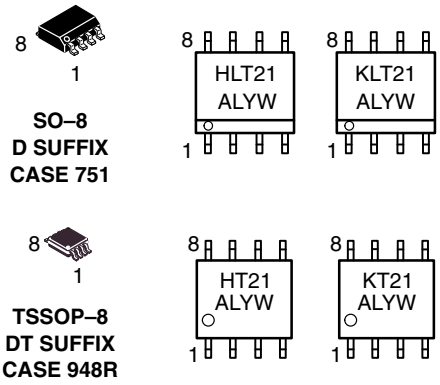
MARKING DIAGRAMS*



H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10ELT21D	SO–8	98 Units/Rail
MC10ELT21DR2	SO–8	2500 Tape & Reel
MC100ELT21D	SO–8	98 Units/Rail
MC100ELT21DR2	SO–8	2500 Tape & Reel
MC10ELT21DT	TSSOP–8	98 Units/Rail
MC10ELT21DTR2	TSSOP–8	2500 Tape & Reel
MC100ELT21DT	TSSOP–8	98 Units/Rail
MC100ELT21DTR2	TSSOP–8	2500 Tape & Reel

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Power Supply	GND = 0 V		7	V
V_{IN}	PECL Input Voltage	GND = 0 V	$V_I \leq V_{CC}$	0 to 6	V
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10ELT SERIES PECL INPUT DC CHARACTERISTICS V_{CC}= 5.0 V; GND= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage (Single Ended)	3770		4110	3870		4190	3930		4265	mV
V_{IL}	Input LOW Voltage (Single Ended)	3050		3500	3050		3520	3050		3555	mV
V_{BB}	Output Voltage Reference	3.57		3.7	3.65		3.75	3.69		3.81	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 2.)	2.2		5.0	2.2		5.0	2.2		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input parameters vary 1:1 with V_{CC}. V_{CC} can vary ± 0.25 V.
2. V_{IHCMR} min varies 1:1 with GND, V_{IHCMR} max varies 1:1 with V_{CC}.

100ELT SERIES PECL INPUT DC CHARACTERISTICS V_{CC}= 5.0 V; GND= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.745	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 2.)	2.2		5.0	2.2		5.0	2.2		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input parameters vary 1:1 with V_{CC}. V_{CC} can vary ± 0.25 V.
2. V_{IHCMR} min varies 1:1 with GND, V_{IHCMR} max varies 1:1 with V_{CC}.

TTL OUTPUT DC CHARACTERISTICS V_{CC}= 4.75 V to 5.25 V; T_A= –40°C to 85°C)

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.0mA	2.4		(Note 1.)	V
V_{OL}	Output LOW Voltage	I_{OL} = 24mA			0.5	V
I_{CCH}	Power Supply Current			20	29	mA
I_{CCL}	Power Supply Current			22	32	mA
I_{OS}	Output Short Circuit Current		–150		–60	mA

1. Max level is V_{CC}–0.7 by design.

AC CHARACTERISTICS V_{CC}= 4.75 V to 5.25 V; GND= 0.0 V

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency		TBD			100			TBD		MHz
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_{PLH}	Propagation Delay @ 1.5 V C_L = 20pF	2.0		5.5	2.0		5.5	2.0		5.5	ns
t_{PHL}	Propagation Delay @ 1.5 V C_L = 20pF	2.0		5.5	2.0		5.5	2.0		5.5	ns
V_{PP}	Input Swing (Note 1.)	200		1000	200		1000	200		1000	mV
t_r/t_f	Output Rise/Fall Time (10–90%) C_L = 20pF					750					ps

1. V_{PP}(min) is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈40.

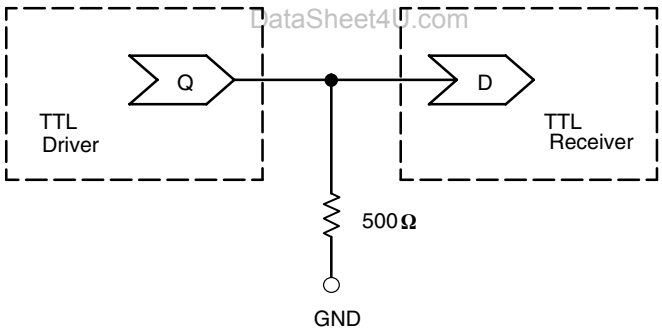


Figure 1. TTL Output Termination

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

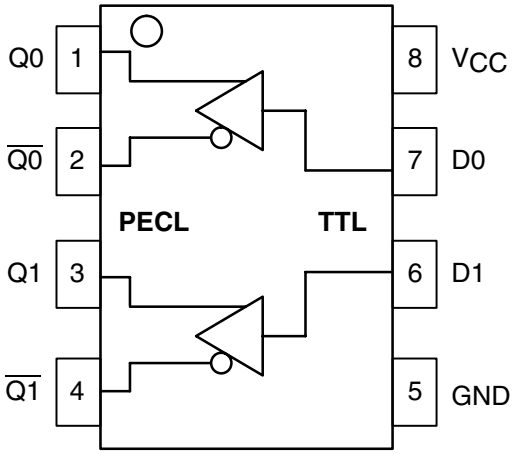
MC10ELT22, MC100ELT22

5V Dual TTL to Differential PECL Translator

The MC10ELT/100ELT22 is a dual TTL to differential PECL translator. Because PECL (Positive ECL) levels are used only +5 V and ground are required. The small outline 8-lead package and the low skew, dual gate design of the ELT22 makes it ideal for applications which require the translation of a clock and a data signal.

- 1.2 ns Typical Propagation Delay
- <300 ps Typical Output to Output Skew
- PNP TTL Inputs for Minimal Loading
- Flow Through Pinouts
- ESD Protection: >2 KV HBM, >200 V MM
- Operating Range: V_{CC}= 4.75 V to 5.25 V with GND= 0 V
- No Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 51 devices

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
Qn, $\overline{Qn}$	PECL Differential Outputs*
Dn	TTL Inputs
V_{CC}	Positive Supply
GND	Ground

* Output state undetermined when inputs are open.

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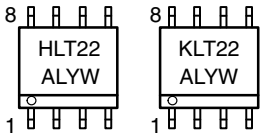
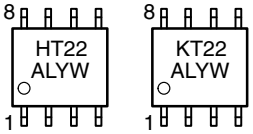
MARKING DIAGRAMS*

SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10ELT22D	SO–8	98 Units/Rail
MC10ELT22DR2	SO–8	2500 Tape & Reel
MC100ELT22D	SO–8	98 Units/Rail
MC100ELT22DR2	SO–8	2500 Tape & Reel
MC10ELT22DT	TSSOP–8	98 Units/Rail
MC10ELT22DTR2	TSSOP–8	2500 Tape & Reel
MC100ELT22DT	TSSOP–8	98 Units/Rail
MC100ELT22DTR2	TSSOP–8	2500 Tape & Reel

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Positive Power Supply	GND = 0 V		7	V
V_{IN}	Input Voltage	GND = 0 V	$V_I \leq V_{CC}$	7	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10ELT SERIES PECL DC CHARACTERISTICS V_{CC} = 5.0 V; GND = 0.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{CC}	Power Supply Current			22			22			22	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Output parameters vary 1:1 with V_{CC}. V_{CC} can vary ± 0.25 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

100ELT SERIES PECL DC CHARACTERISTICS V_{CC} = 5.0 V; GND = 0.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{CC}	Power Supply Current			22			22			22	mA
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Output parameters vary 1:1 with V_{CC}. V_{CC} can vary ± 0.25 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

TTL INPUT DC CHARACTERISTICS V_{CC} = 4.75 V to 5.25 V; T_A = –40°C to 85°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V			20	μA
I_{IHH}	Input HIGH Current	V_{IN} = 7.0 V			100	μA
I_{IL}	Input LOW Current	V_{IN} = 0.5 V			–0.6	mA
V_{IK}	Input Clamp Diode Voltage	I_{IN} = –18 mA			–1.2	V
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V

AC CHARACTERISTICS V_{CC}= 4.75 V to 5.25 V; GND= 0.0 V

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{MAX}	Maximum Input Frequency	100			100			100			MHz
t_{PLH}	Propagation Delay (Note 2.) 1.5 V to 50%	0.6		1.2	0.9	1.2	1.5	0.6		1.35	ns
t_{PHL}	Propagation Delay (Note 2.) 1.5 V to 50%	0.4		1.0	0.5	0.8	1.1	0.7		1.30	ns
t_{JITTER}	Cycle–to–Cycle Jitter			TBD	TBD			TBD			ps
t_r/t_f	Output Rise/Fall Time (20–80%)	0.4		1.6	0.4		1.6	0.4		1.6	ns

2. Specifications for standard TTL input signal.

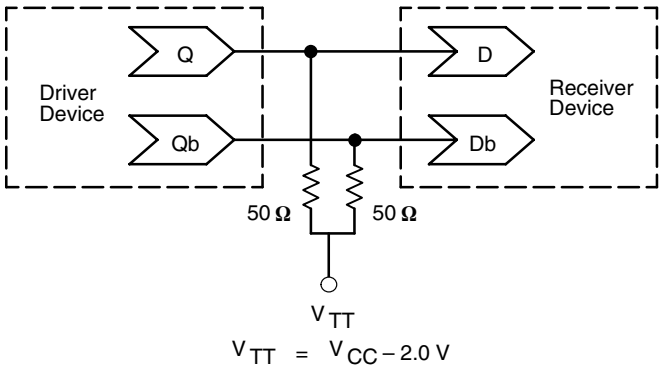


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1400	–	MC10/100H640 Clock Driver Family I/O SPICE Modeling Kit
AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC100ELT23

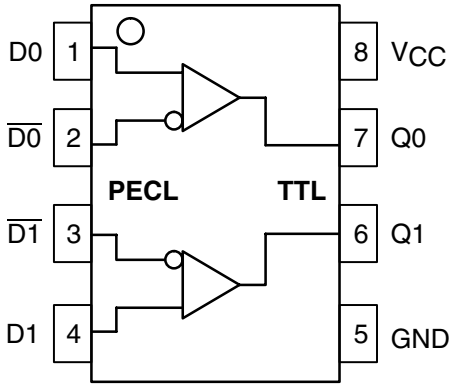
5V Dual Differential PECL to TTL Translator

The MC100ELT23 is a dual differential PECL to TTL translator. Because PECL (Positive ECL) levels are used, only +5 V and ground are required. The small outline 8-lead package and the dual gate design of the ELT23 makes it ideal for applications which require the translation of a clock and a data signal.

The PECL inputs are differential; therefore, the MC100ELT23 can accept any standard differential PECL input referenced from a V_{CC} of 5.0 V.

- 3.5 ns Typical Propagation Delay
- 24 mA TTL Outputs
- Flow Through Pinouts
- ESD Protection: >2 KV HBM, > 400 V MM
- The 100 Series Contains Temperature Compensation
- Operating Range V_{CC}= 4.75 V to 5.25 V with GND= 0 V
- Internal Input Pulldown Resistors
- Q Output Will Default High with Inputs Left Open or < 1.3 V
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 91 devices

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
Qn	TTL Outputs
Dn, $\overline{Dn}$	PECL Differential Inputs
V_{CC}	Positive Supply
GND	Ground

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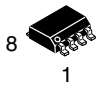
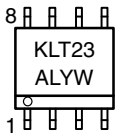
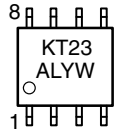
MARKING DIAGRAMS*



SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100ELT23D	SO–8	98 Units / Rail
MC100ELT23DR2	SO–8	2500 / Reel
MC100ELT23DT	TSSOP–8	98 Units / Rail
MC100ELT23DTR2	TSSOP–8	2500 / Reel

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Power Supply	GND = 0 V		7	V
V_I	Input Voltage	GND = 0 V	$V_I \leq V_{CC}$	0 to 6 	V V
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

PECL INPUT DC CHARACTERISTICS V_{CC}= 5.0 V; GND= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 2.)	2.2		5.0	2.2		5.0	2.2		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input parameters vary 1:1 with V_{CC}. V_{CC} can vary ± 0.25 V.
2. V_{IHCMR} min varies 1:1 with GND, V_{IHCMR} max varies 1:1 with V_{CC}.

TTL OUTPUT DC CHARACTERISTICS V_{CC} = 4.75V to 5.25V; T_A = –40°C to 85°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.0 mA	2.4		(Note 1.)	V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA			0.5	V
I_{CCH}	Power Supply Current			23	33	mA
I_{CCL}	Power Supply Current			26	36	mA
I_{OS}	Output Short Circuit Current		–150		–60	mA

1. Max level is V_{CC}–0.7 V by design.

AC CHARACTERISTICS V_{CC}= 5.0 V; GND= 0.0 V (Note 1.)

			–40°C			25°C			85°C			
Symbol	Characteristic		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency			TBD			TBD			TBD		MHz
t_{JITTER}	Cycle–to–Cycle Jitter			TBD			TBD			TBD		ps
t_{PLH}	Propagation Delay @ 1.5 V	C_L = 20 pF	2.0		5.5	2.0		5.5	2.0		5.5	ns
t_{PHL}	Propagation Delay @ 1.5 V	C_L = 20 pF	2.0		5.5	2.0		5.5	2.0		5.5	ns
V_{PP}	Input Swing (Note 2.)		200		1000	200		1000	200		1000	mV
t_r/t_f	Output Rise Time (10–90%) Output Fall Time (10–90%)	C_L = 20pF C_L = 20pF					1.6 1.1					ns ns

1. V_{CC} can vary ± 0.25 V.
2. V_{PP}(min) is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈40.

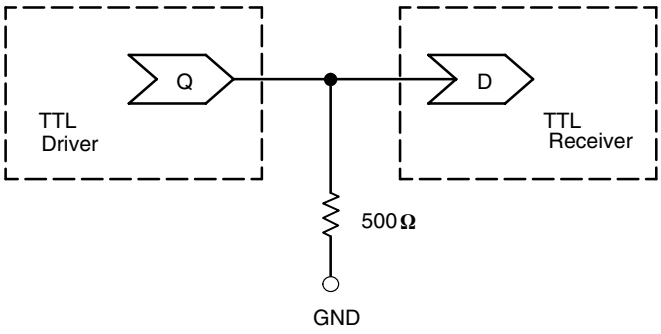


Figure 1. TTL Output Termination

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10ELT24, MC100ELT24

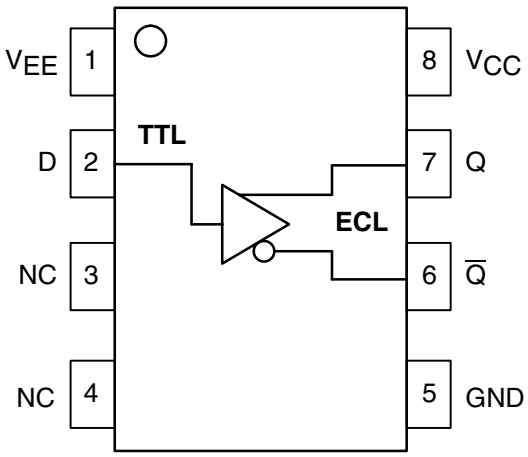
5V TTL to Differential ECL Translator

The MC10ELT/100ELT24 is a TTL to differential ECL translator. Because ECL levels are used a +5V, -5.2V (or -4.5V) and ground are required. The small outline 8-lead package and the single gate of the ELT24 makes it ideal for those applications where space, performance and low power are at a premium.

The 100 Series contains temperature compensation.

- 0.8 ns TPHL, 0.95 ns TPLH Typical Propagation Delay
- PNP TTL Inputs for Minimal Loading
- Flow Through Pinouts
- ESD Protection: >4 KV HBM, >200 V MM
- Operating Range: V_{CC}= 4.5 V to 5.5 V; V_{EE}= –4.2 V to –5.5 V with GND= 0 V
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 51 devices

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
Q, $\overline{Q}$	ECL Differential Outputs*
D	TTL Input
V_{CC}	Positive Supply
V_{EE}	Negative Supply
GND	Ground
NC	No Connect

* Output state undetermined when inputs are open.

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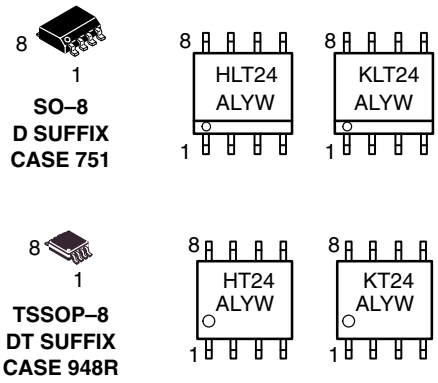
MARKING DIAGRAMS*



H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10ELT24D	SO–8	98 Units/Rail
MC10ELT24DR2	SO–8	2500 Tape & Reel
MC100ELT24D	SO–8	98 Units/Rail
MC100ELT24DR2	SO–8	2500 Tape & Reel
MC10ELT24DT	TSSOP–8	98 Units/Rail
MC10ELT24DTR2	TSSOP–8	2500 Tape & Reel
MC100ELT24DT	TSSOP–8	98 Units/Rail
MC100ELT24DTR2	TSSOP–8	2500 Tape & Reel

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Positive Power Supply	GND = 0 V	V_{EE} = –5.0 V	7	V
V_{EE}	Negative Power Supply	GND = 0 V	V_{CC} = +5.0 V	–8	V
V_{IN}	Input Voltage	GND = 0 V	$V_I \leq V_{CC}$	0 to V_{CC}	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10ELT SERIES NECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= –5.0 V; GND = 0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current			18		12.5	18			18	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1080	–990	–890	–980	–895	–810	–910	–815	–720	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1950	–1800	–1650	–1950	–1790	–1630	–1950	–1773	–1595	mV

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Output parameters vary 1:1 with GND. V_{EE} can vary +0.06 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to GND–2 volts.

100ELT SERIES NECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= –5.0 V; GND = 0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current			18		12.5	18			18	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Output parameters vary 1:1 with GND. V_{EE} can vary +0.8 V / –0.5 V.
2. Outputs are terminated through a 50 ohm resistor to GND–2 volts.

TTL INPUT DC CHARACTERISTICS V_{CC} = 4.75 V to 5.25 V; T_A = –40°C to +85°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V			20	μA
I_{IHH}	Input HIGH Current	V_{IN} = 7.0 V			100	μA
I_{IL}	Input LOW Current	V_{IN} = 0.5 V			–0.6	mA
V_{IK}	Input Clamp Diode Voltage	I_{IN} = –18 mA			–1.2	V
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V

AC CHARACTERISTICS V_{CC}= 4.75 V to 5.25 V; V_{EE}= –5.0 V; GND= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH}	Propagation Delay (Note 2.) 1.5 V to 50%	0.7		1.3	0.65	0.95	1.25	0.65		1.25	ns
t_{PHL}	Propagation Delay (Note 2.) 1.5 V to 50%	0.4		1.0	0.50	0.80	1.10	0.70		1.30	ns
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r/t_f	Output Rise/Fall Time (20–80%)	0.25		1.25	0.25		1.25	0.25		1.25	ns

1. V_{EE} can vary +0.06 V / –0.5 V for 10ELT; V_{EE} can vary +0.8 V / –0.5 V for 100ELT.
2. Specifications for standard TTL input signal.

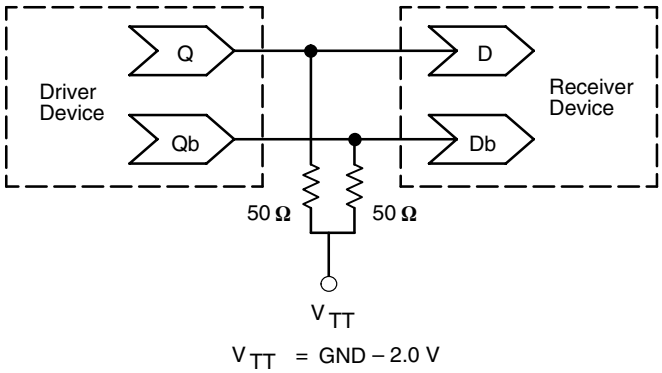


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10ELT25, MC100ELT25

-5V Differential ECL to TTL Translator

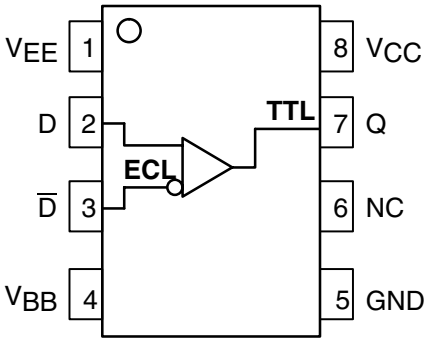
The MC10ELT/100ELT25 is a differential ECL to TTL translator. Because ECL levels are used, a +5 V, -5.2 V (or -4.5 V) and ground are required. The small outline 8-lead package and the single gate of the ELT25 makes it ideal for those applications where space, performance and low power are at a premium.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

- 2.6 ns Typical Propagation Delay
- 100 MHz F_{MAX} CLK
- 24 mA TTL Outputs
- Flow Through Pinouts
- ESD Protection: >1 KV HBM, > 400 V MM
- Operating Range: V_{CC}= 4.5 V to 5.5 V with GND= 0 V; V_{EE}= –4.2 V to –5.7 V with GND= 0 V
- Internal Input Pulldown Resistors
- Q Output will default HIGH with inputs open or < 1.3 V
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 38 devices

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
D, $\overline{D}$	ECL Differential Inputs
Q	TTL Output
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
GND	Ground
NC	No Connect

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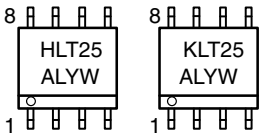
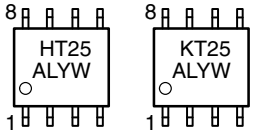
MARKING DIAGRAMS*

SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10ELT25D	SO–8	98 Units/Rail
MC10ELT25DR2	SO–8	2500 Tape & Reel
MC100ELT25D	SO–8	98 Units/Rail
MC100ELT25DR2	SO–8	2500 Tape & Reel
MC10ELT25DT	TSSOP–8	98 Units/Rail
MC10ELT25DTR2	TSSOP–8	2500 Tape & Reel
MC100ELT25DT	TSSOP–8	98 Units/Rail
MC100ELT25DTR2	TSSOP–8	2500 Tape & Reel

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Positive Power Supply	GND = 0 V	V_{EE} = –5.0 V	7	V
V_{EE}	Negative Power Supply	GND = 0 V	V_{CC} = +5.0 V	–8	V
V_{IN}	Input Voltage	GND = 0 V		0 to V_{EE}	V
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10ELT SERIES NECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= –5.0 V; GND= 0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage (Single Ended)	–1230		–890	–1130		–810	–1060		–720	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1950		–1500	–1950		–1480	–1950		–1445	mV
V_{BB}	Output Voltage Reference	–1.43		–1.30	–1.35		–1.25	–1.31		–1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 2.)	–2.8		0.0	–2.8		0.0	–2.8		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input parameters vary 1:1 with GND. V_{EE} can vary +0.06 V / –0.5 V.
2. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with GND.

100ELT SERIES NECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= –5.0 V; GND= 0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 2.)	–2.8		0.0	–2.8		0.0	–2.8		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input parameters vary 1:1 with GND. V_{EE} can vary +0.8 V / –0.5 V.
2. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with GND.

TTL OUTPUT DC CHARACTERISTICS V_{CC} = 4.5 V to 5.5 V; T_A = –40°C to +85°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.0 mA	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA			0.5	V
I_{CCH}	Power Supply Current			11	16	mA
I_{CCL}	Power Supply Current			13	18	mA
I_{EE}	Negative Power Supply Current			15	21	mA
I_{OS}	Output Short Circuit Current		–150		–60	mA

AC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= –5.0 V; GND= 0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency		100			100			100		MHz
t_{PLH}	Propagation Delay @ 1.5 V C_L = 20 pF	1.7		3.6	1.7		3.6	1.7		3.6	ns
t_{PHL}	Propagation Delay @ 1.5 V C_L = 20 pF	2.6		4.1	2.6		4.1	2.6		4.1	ns
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise/Fall Times QTTL 10% – 90%					1.9 2.3					ns
V_{PP}	Input Swing (Note 2.)	200		1000	200		1000	200		1000	mV

1. V_{CC} can vary ± 0.25 V.
   V_{EE} can vary +0.06 V / –0.5 V for 10ELT; V_{EE} can vary +0.8 V / –0.5 V for 100ELT.
2. V_{PP}(min) is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈40.

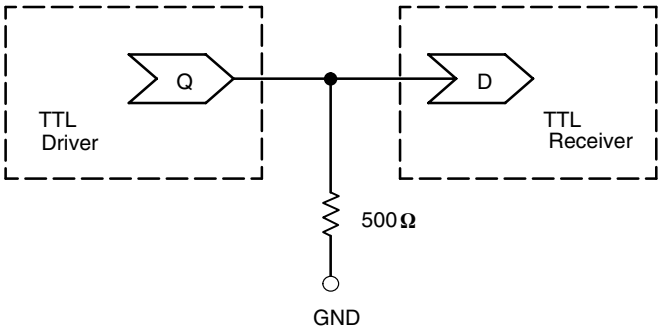


Figure 1. TTL Output Termination

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10ELT26, MC100ELT26

5V 1:2 Fanout Differential PECL to TTL Translator

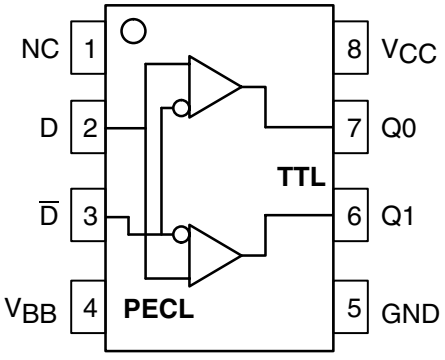
The MC10ELT/100ELT26 is a 1:2 fanout differential PECL to TTL translator. Because PECL (Positive ECL) levels are used, only +5 V and ground are required. The small outline 8-lead package and the 1:2 fanout design of the ELT26 makes it ideal for applications which require the low skew duplication of a signal in a tightly packed PC board.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The 100 Series contains temperature compensation.

- 3.5 ns Typical Propagation Delay
- <500 ps Typical Output to Output Skew
- 24 mA TTL Outputs
- Flow Through Pinouts
- ESD Protection: 2 KV HBM
- Operating Range V_{CC}= 4.75 V to 5.25 V with GND= 0 V
- Internal Input Pulldown Resistors
- Q Output Will Default High with Inputs Left Open or < 1.3 V
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 117 devices

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
Qn	TTL Outputs
D, $\overline{D}$	PECL Differential Inputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
GND	Ground
NC	No Connect

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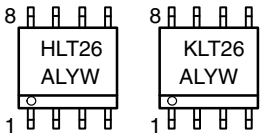
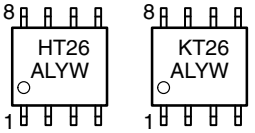
MARKING DIAGRAMS*

SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10ELT26D	SO–8	98 Units/Rail
MC10ELT26DR2	SO–8	2500 Tape & Reel
MC100ELT26D	SO–8	98 Units/Rail
MC100ELT26DR2	SO–8	2500 Tape & Reel
MC10ELT26DT	TSSOP–8	98 Units/Rail
MC10ELT26DTR2	TSSOP–8	2500 Tape & Reel
MC100ELT26DT	TSSOP–8	98 Units/Rail
MC100ELT26DTR2	TSSOP–8	2500 Tape & Reel

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Positive Power Supply	GND = 0 V		7	V
V_{IN}	Input Voltage	GND = 0 V	$V_I \leq V_{CC}$	0 to 6	V
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10ELT SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; GND= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage (Single Ended)	3770		4110	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage (Single Ended)	3050		3500	3050		3520	3050		3555	mV
V_{BB}	Output Voltage Reference	3.57		3.7	3.65		3.75	3.69		3.81	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 2.)	2.2		5.0	2.2		5.0	2.2		5.0	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	0.5			0.5			0.3			µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input parameters vary 1:1 with V_{CC}. V_{CC} can vary ± 0.25 V.
2. V_{IHCMR} min varies 1:1 with GND, V_{IHCMR} max varies 1:1 with V_{CC}.

100ELT SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; GND= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 2.)	2.2		5.0	2.2		5.0	2.2		5.0	V
I_{IH}	Input HIGH Current			150			150			150	µA
I_{IL}	Input LOW Current	0.5			0.5			0.5			µA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input parameters vary 1:1 with V_{CC}. V_{CC} can vary ± 0.25 V.
2. V_{IHCMR} min varies 1:1 with GND, V_{IHCMR} max varies 1:1 with V_{CC}.

TTL OUTPUT DC CHARACTERISTICS V_{CC} = 4.75V to 5.25V; GND = 0 V; T_A = –40°C to 85°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.0 mA	2.4		(Note 1.)	V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA			0.5	V
I_{CCH}	Power Supply Current			23	33	mA
I_{CCL}	Power Supply Current			26	36	mA
I_{OS}	Output Short Circuit Current		–150		–60	mA

1. Max level is V_{CC}–0.7 V by design.

AC CHARACTERISTICS V_{CC}= 5.0 V; GND= 0.0 V (Note 1.)

Symbol	Characteristic		–40°C			25°C			85°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency			TBD			100			TBD		MHz
t_{JITTER}	Cycle–to–Cycle Jitter			TBD			TBD			TBD		ps
t_{PLH}	Propagation Delay	C_L = 20 pF	2.0		5.5	2.0		5.5	2.0		5.5	ns
t_{PHL}	Propagation Delay	C_L = 20 pF	2.0		5.5	2.0		5.5	2.0		5.5	ns
V_{PP}	Input Swing (Note 2.)		200		1000	200		1000	200		1000	mV
t_r/t_f	Output Rise Time (10–90%) Output Fall Time (10–90%)	C_L = 20pF C_L = 20pF					1.6 1.1					ns ns

1. V_{CC} can vary ± 0.25 V.
2. V_{PP}(min) is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈40.

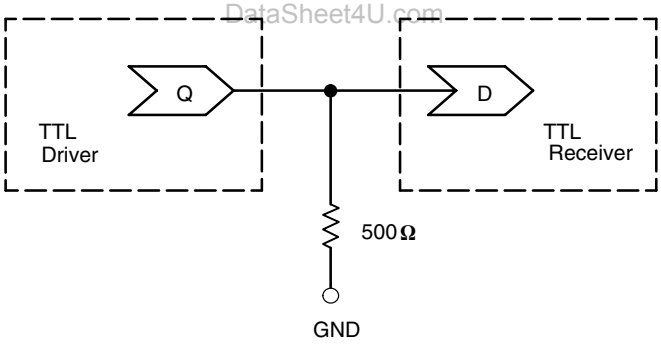


Figure 1. TTL Output Termination

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC10ELT28, MC100ELT28

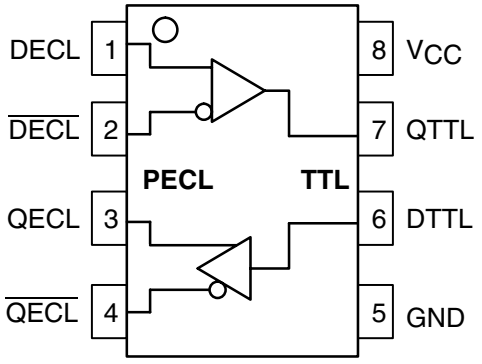
5V TTL to Differential PECL and Differential PECL to TTL Translator

The MC10ELT/100ELT28 is a differential PECL to TTL translator and a TTL to differential PECL translator in a single package. Because PECL (Positive ECL) levels are used, only +5 V and ground are required. The small outline 8-lead package and the dual translation design of the ELT28 makes it ideal for applications which are sending and receiving signals across a backplane.

The 100 Series contains temperature compensation.

- 3.5 ns Typical PECL to TTL Propagation Delay
- 1.2 ns Typical TTL to PECL Propagation Delay
- PNP TTL Inputs for Minimal Loading
- 24 mA TTL Outputs
- Flow Through Pinouts
- ESD Protection: >2 KV HBM
- Operating Range V_{CC}= 4.75 V to 5.25 V with GND= 0 V
- Q_{TTL} Output Will Default High with Inputs Left Open or < 1.3 V
- Q_{ECL} Output Will Default High with Inputs Left Open
- Internal PECL Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 71 devices

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
QTTL	TTL Output
DTTL	TTL Inputs
QECL, $\overline{QECL}$	PECL Differential Outputs
DECL, $\overline{DECL}$	PECL Differential Inputs
V_{CC}	Positive Supply
GND	Ground

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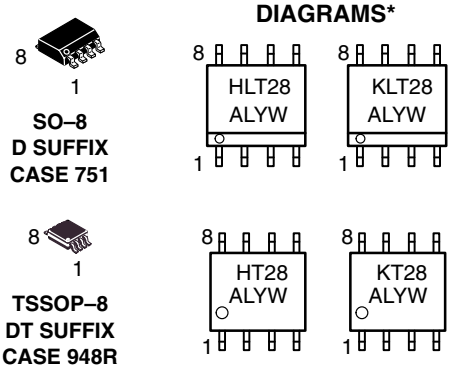
MARKING DIAGRAMS*



SO–8
D SUFFIX
CASE 751

TSSOP–8
DT SUFFIX
CASE 948R

H = MC10
K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10ELT28D	SO–8	98 Units/Rail
MC10ELT28DR2	SO–8	2500 Tape & Reel
MC100ELT28D	SO–8	98 Units/Rail
MC100ELT28DR2	SO–8	2500 Tape & Reel
MC10ELT28DT	TSSOP–8	98 Units/Rail
MC10ELT28DTR2	TSSOP–8	2500 Tape & Reel
MC100ELT28DT	TSSOP–8	98 Units/Rail
MC100ELT28DTR2	TSSOP–8	2500 Tape & Reel

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Positive Power Supply	GND = 0 V		7	V
V_{IN}	Input Voltage	GND = 0 V	$V_I \leq V_{CC}$	0 to 6	V
I_{out}	PECL Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

10ELT SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; GND= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage (Note 2.)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
V_{OL}	Output LOW Voltage (Note 2.)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3770		4110	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage (Single Ended)	3050		3500	3050		3520	3050		3555	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.2		5.0	2.2		5.0	2.2		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.3			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{CC} can vary ± 0.25 V.
2. PECL outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with GND, V_{IHCMR} max varies 1:1 with V_{CC}.

100ELT SERIES PECL DC CHARACTERISTICS V_{CC}= 5.0 V; GND= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	2.2		5.0	2.2		5.0	2.2		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{CC} can vary ± 0.25 V.
2. PECL outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with GND, V_{IHCMR} max varies 1:1 with V_{CC}.

TTL OUTPUT DC CHARACTERISTICS V_{CC} = 4.75V to 5.25V; T_A = –40°C to 85°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.0 mA	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA			0.5	V
I_{CCH}	Power Supply Current			27	40	mA
I_{CCL}	Power Supply Current			29	42	mA
I_{OS}	Output Short Circuit Current		–150		–60	mA

TTL INPUT DC CHARACTERISTICS V_{CC} = 4.75 V to 5.25 V; T_A = –40°C to 85°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V			20	μA
I_{IHH}	Input HIGH Current	V_{IN} = 7.0 V			100	μA
I_{IL}	Input LOW Current	V_{IN} = 0.5 V			–0.6	mA
V_{IK}	Input Clamp Diode Voltage	I_{IN} = –18 mA			–1.2	V
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V

AC CHARACTERISTICS V_{CC} = 4.75 V to 5.25 V

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency		TBD			100			TBD		MHz
t_{PLH}	Propagation Delay @ 1.5 V C_L = 20 pF DECL to QTTL DTTL to QECL	 2.0 0.6		 5.5 1.2	 2.0 0.9	 1.2	 5.5 1.5	 2.0 0.6		 5.5 1.35	ns
t_{PHL}	Propagation Delay @ 1.5 V C_L = 20 pF DECL to QTTL DTTL to QECL	 2.0 0.4		 5.5 1.0	 2.0 0.5	 0.8	 5.5 1.1	 2.0 0.7		 5.5 1.3	ns
t_r, t_f	Rise/Fall Times (20% – 80%) QECL	0.15		1.5	0.15		1.5	0.15		1.5	ns
V_{PP}	PECL Input Swing (Note 1.)	200		1000	200		1000	200		1000	mV
t_r/t_f	Output Rise Time (10–90%) C_L = 20pF Output Fall Time (10–90%) C_L = 20pF					1.6 1.1					ns ns

1. V_{PP}(min) is the minimum input swing for which AC parameters are guaranteed.

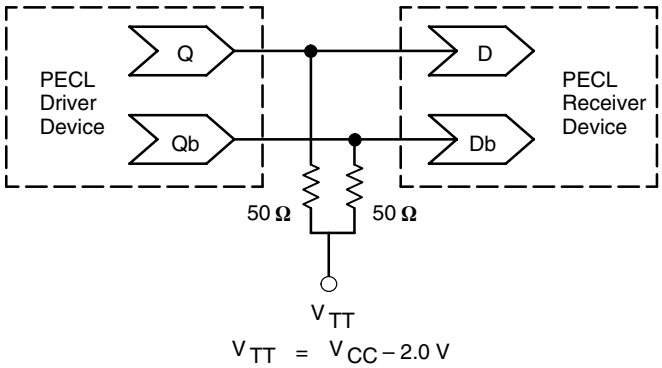


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

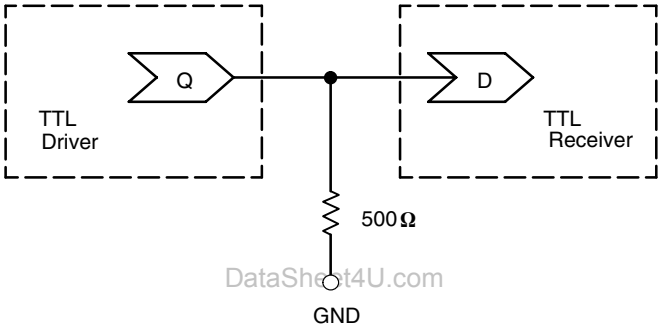


Figure 2. TTL Output Termination

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC100EL1648

5V ECL Voltage Controlled Oscillator

The MC100EL1648 requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C). A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (V_{CO}). This device may also be used in many other applications requiring a fixed frequency clock.

The MC100EL1648 is ideal in applications requiring a local oscillator. Systems include electronic test equipment and digital high–speed telecommunications.

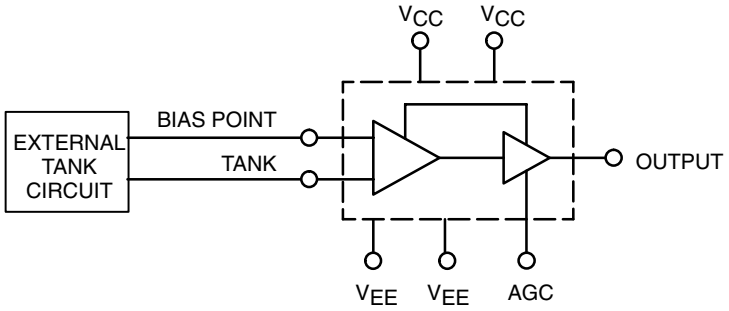
The MC100EL1648 is based on the V_{CO} circuit topology of the MC1648. The MC100EL1648 uses advanced bipolar process technology which results in a design which can operate at an extended frequency range.

The ECL output circuitry of the MC100EL1648 is not a traditional open emitter output structure and instead has an on–chip termination resistor with a nominal value of 510 ohms. This facilitates direct ac–coupling of the output signal into a transmission line. Because of this output configuration, an external pull–down resistor is not required to provide the output with a dc current path. This output is intended to drive one ECL load. If the user needs to fanout the signal, an ECL buffer such as the MC10EL16 Line Receiver/Driver should be used.

NOTE: The MC100EL1648 is NOT useable as a crystal oscillator.

- Typical Operating Frequency Up to 1100 MHz
- Low–Power 19 mA at 5.0 Vdc Power Supply
- Phase Noise –90 dBc/Hz at 25 kHz Typical
- ESD Protection: >2 KV HBM, >100 V MM
- PECL Mode Operating Range: V_{CC}= 5.0 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –5.2 V
- Input Capacitance= 6.0 pF (TYP)
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Maximum Series Resistance for L (External Inductance)= 50 Ω (TYP)
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 11 devices

LOGIC DIAGRAM



ON Semiconductor™

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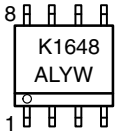
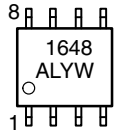
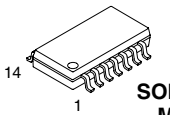
MARKING DIAGRAMS*

SO–8
D SUFFIX
CASE 751

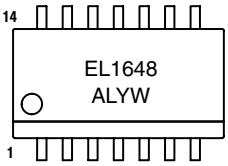


TSSOP–8
DT SUFFIX
CASE 948R





SOIC EIAJ–14
M SUFFIX
CASE 965



K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

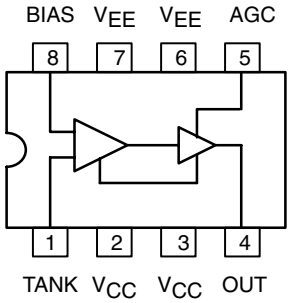
*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

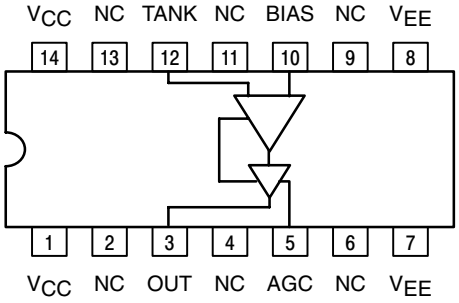
Device	Package	Shipping
MC100EL1648D	SO–8	98 Units / Rail
MC100EL1648DR2	SO–8	2500 Units / Reel
MC100EL1648DT	TSSOP–8	98 Units / Rail
MC100EL1648DTR2	TSSOP–8	2500 / Reel
MC100EL1648M	SOIC EIAJ–14	50 Units / Rail
MC100EL1648MEL	SOIC EIAJ–14	2500 Units / Reel

MC100EL1648

LOGIC DIAGRAMS AND PINOUT ASSIGNMENTS



8 Lead



14 Lead

PIN DESCRIPTION

PIN	FUNCTION	8 LD	14 LD
BIAS	OSC Input Reference Voltage	8	10
TANK	OSC Input Voltage	1	12
AGC	Automatic Gain Control Input	5	5
OUT	ECL Output	4	3
V_{CC}	Positive Supply	2, 3	1, 14
V_{EE}	Negative Supply	6, 7	7, 8
NC	No Connect		2, 4, 7, 9, 11, 13

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Power Supply PECL Mode	V_{EE} = 0 V		7 to 0	V
V_{EE}	Power Supply NECL Mode	V_{CC} = 0 V		–7 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	16 SOIC	TBD	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	14 SOIC 14 SOIC	TBD TBD	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	14 SOIC	TBD	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

PECL DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= 0.0 V +0.8 / –0.5 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current	18		19	18		19	18		19	mA
V_{OH}	Output HIGH Voltage (Note 2.)	4050		4285	4050		4285	4050		4285	mV
V_{OL}	Output LOW Voltage (Note 2.)	3363		3476	3363		3476	3363		3476	mV
AGC	Automatic Gain Control Input	1881		1690	1881		1690	1881		1690	mV
V_{BIAS}	Bias Voltage (Note 3.)	1529		1914	1529		1914	1529		1914	mV
V_{PP}	Peak–to–Peak Tank Voltage	300	400		300	400		300	400		mV

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Output parameters vary 1:1 with V_{CC}.
2. 1.0 MΩ impedance.
3. This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point.

NECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –5.0 V +0.8 / –0.5 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current	18		19	18		19	18		19	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–950		–715	–950		–715	–950		–715	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1637		–1524	–1637		–1524	–1637		–1524	mV
AGC	Automatic Gain Control Input	–3119		–3310	–3119		–3310	–3119		–3310	mV
V_{BIAS}	Bias Voltage (Note 3.)	–3471		–3086	–3471		–3086	–3471		–3086	mV
V_{PP}	Peak–to–Peak Tank Voltage	300	400		300	400		300	400		mV

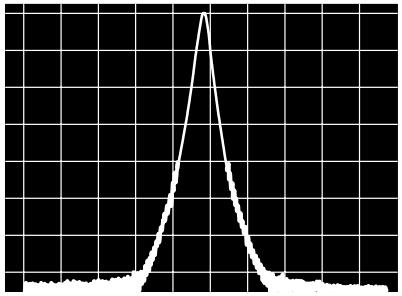
NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Output parameters vary 1:1 with V_{CC}.
2. 1.0 MΩ impedance.
3. This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point.

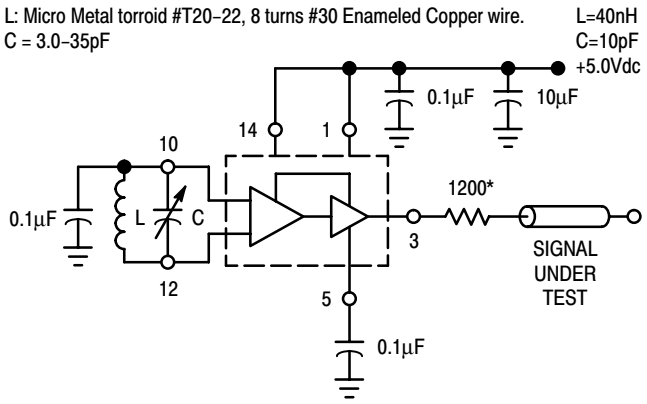
AC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= 5.0 (+0.8 / –0.5 V) or V_{CC} = 5.0 V; V_{EE} = 0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
ℒ (f)	CSR @ 25 kHz Offset, 1.0 Hz BW		–90			–90			–90		dBc/Hz
ℒ (f)	CSR @ 1.0 MHz Offset, 1.0 Hz BW		–120			–120			–120		dBc/Hz
SNR	Signal to Noise Ratio from Carrier		40			40			40		dB
F_{sts}	Frequency Stability (Supply Drift)		3.6			3.6			3.6		kHz/mV
F_{stt}	Frequency Stability (Thermal Drift)		0.1			0.1			0.1		kHz/°C
Hz	Second Harmonic from Carrier		–25			–25			–25		dBc
V_{dc}	Output Duty Cycle					50					%
f_{max}	(Note 1)		1.1			1.1			1.1		Ghz

1. Frequency variation over temperature is a direct function of the ΔC/Δ Temperature and ΔL/Δ Temperature.



B.W. = 10 kHz
Center Frequency = 100 MHz
Scan Width = 50 kHz/div
Vertical Scale = 10 dB/div



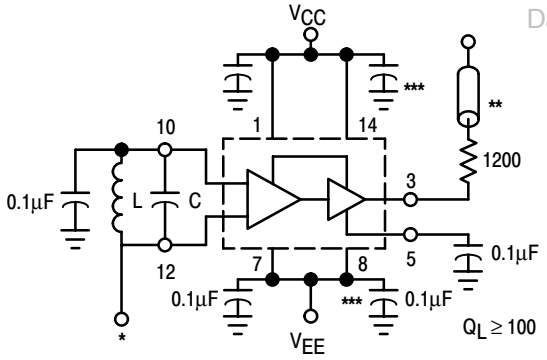
* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT-075-50 or equivalent.

Spectral Purity of Signal Output for 200MHz Testing

TEST VOLTAGE/CURRENT VALUES

@ Test Temperature	(Volts)			mAdc
	V_{IHmax}	V_{ILmin}	V_{EE}	I_L
MC1648				
–30°C	–3.2	–3.7	–5.2	–5.0
+25°C	–3.35	–3.85	–5.2	–5.0
+85°C	–3.5	–4.0	–5.2	–5.0

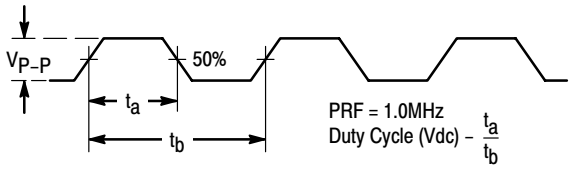
Note: SOIC "D" package guaranteed –30°C to +70°C only



* Use high impedance probe (>1.0 Megohm must be used).

** The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

*** Bypass only that supply opposite ground.



Test Circuit and Waveforms

OPERATING CHARACTERISTICS

Figure 1. illustrates the circuit schematic for the MC100EL1648. The oscillator incorporates positive feedback by coupling the base of transistor Q6 to the collector of Q7. An automatic gain control (AGC) is incorporated to limit the current through the emitter–coupled pair of transistors (Q7 and Q6) and allow optimum frequency response of the oscillator.

In order to maintain the high Q of the oscillator, and provide high spectral purity at the output, transistor Q4 is used to translate the oscillator signal to the output differential pair Q2 and Q3. Q2 and Q3, in conjunction with output transistor Q1, provides a highly buffered output which produces a square wave. Transistors Q9 and Q11 provide the bias drive for the oscillator and output buffer. 2 indicates the high spectral purity of the oscillator output (pin 3).

When operating the oscillator in the voltage controlled mode (Figure 3.), it should be noted that the cathode of the varactor diode (D) should be biased at least "2" V_{BE} above V_{EE} (≈1.4V for positive supply operation).

When the MC100EL1648 is used with a constant dc voltage to the varactor diode, the output frequency will vary slightly because of internal noise. This variation is plotted versus operating frequency in Figure 4.

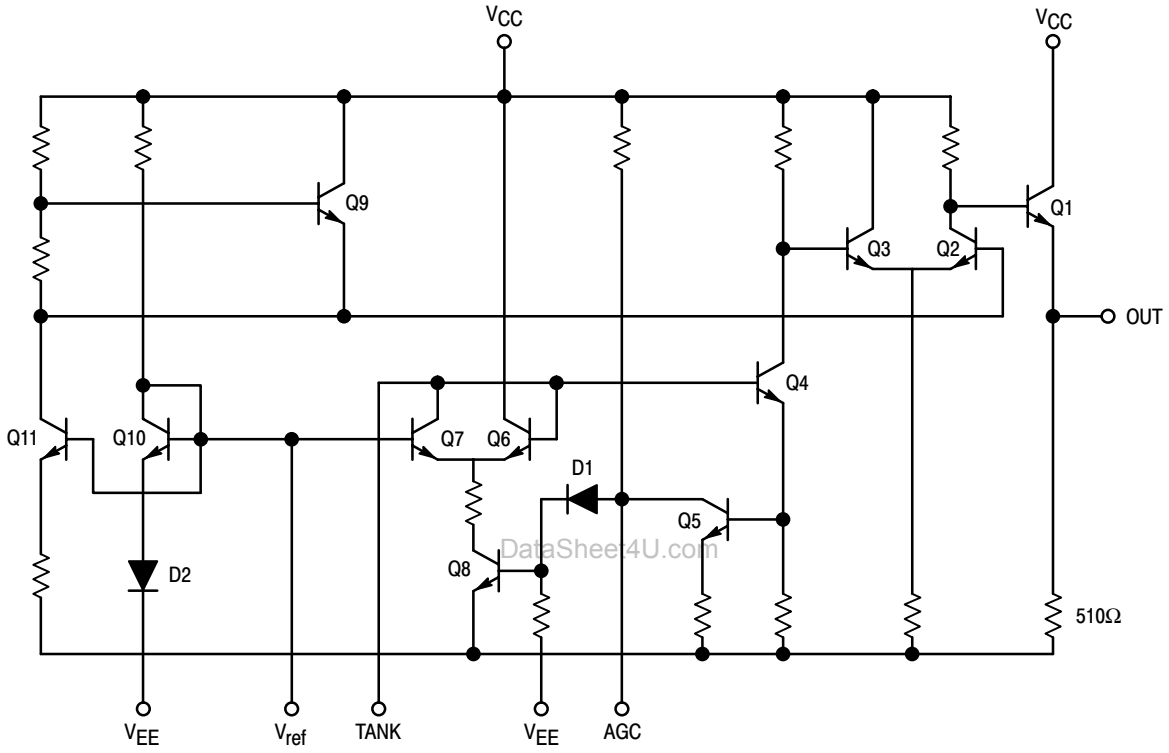


Figure 1. Circuit Schematic

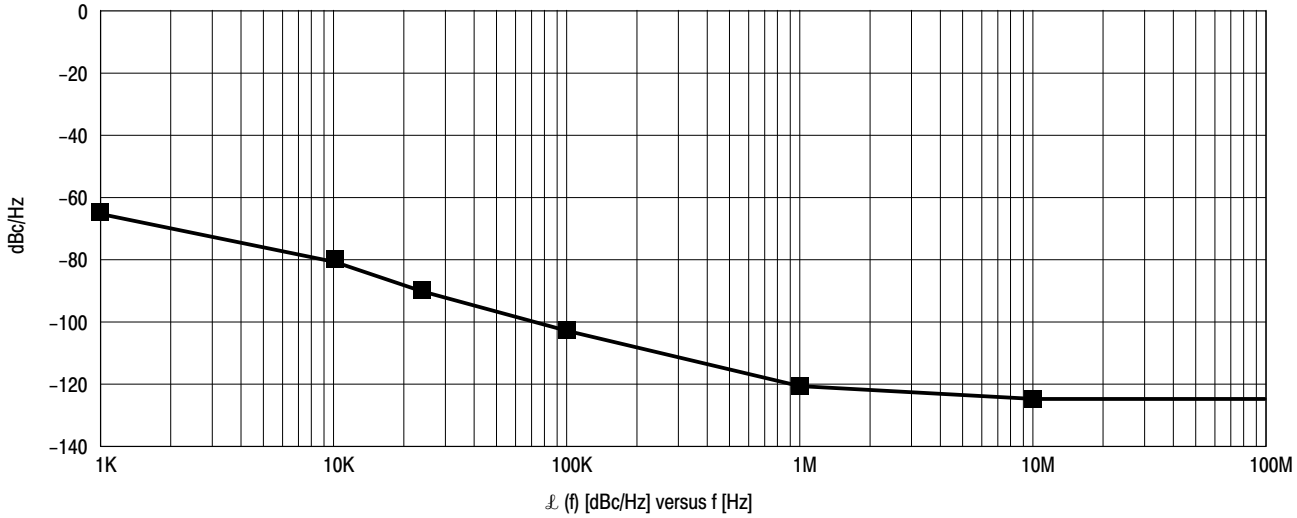


Figure 2. Typical Evaluation Results
(CSR MC100EL1648 5.0 Vdc; V_{CC} @ 25°C; 930 MHz CW)

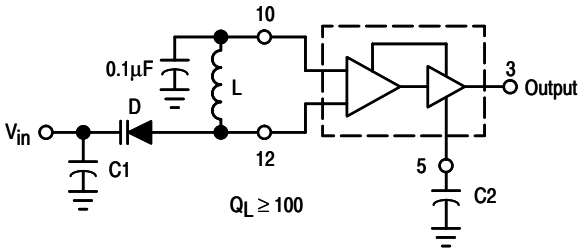
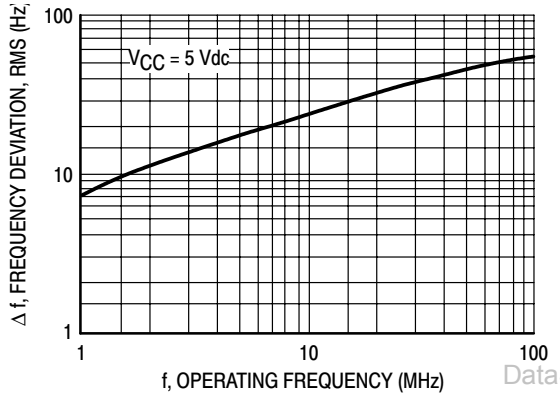
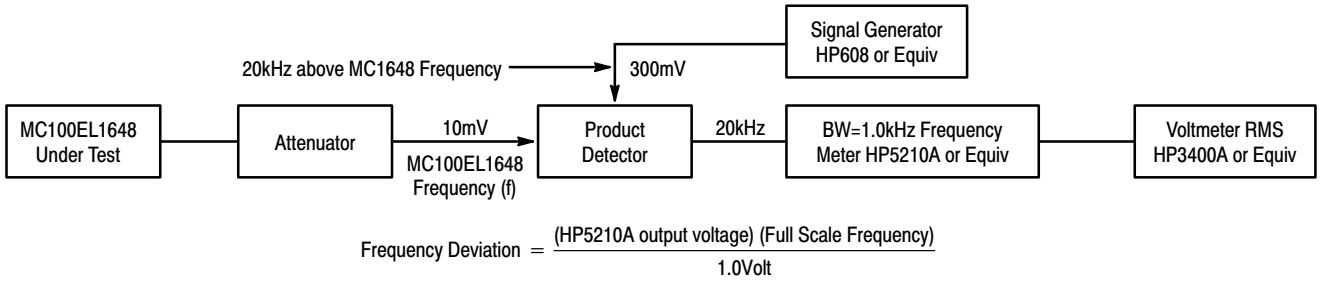


Figure 3. The MC100EL1648 Operating in the Voltage Controlled Mode



Oscillator Tank Components (Circuit of 3.)

f MHz	D	L μH
1.0–10	MV2115	100
10–60	MV2115	2.3
60–100	MV2106	0.15



$$\text{Frequency Deviation} = \frac{\text{(HP5210A output voltage) (Full Scale Frequency)}}{\text{1.0Volt}}$$

Figure 4. Noise Deviation Test Circuit and Waveform

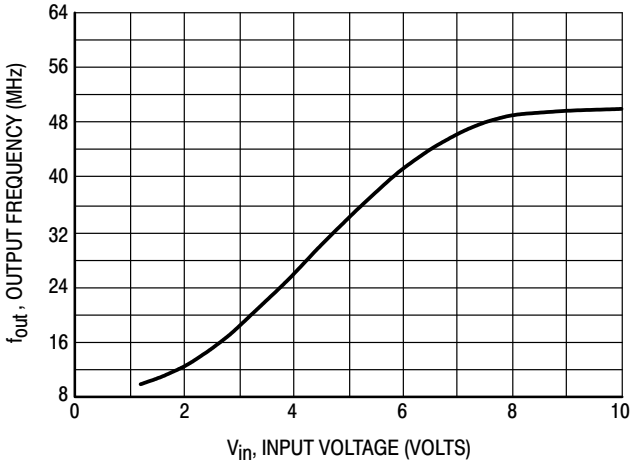
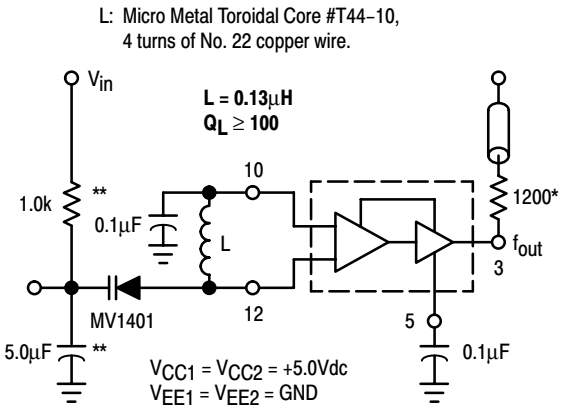


Figure 5.



* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT−070−50 or equivalent. NOT used in normal operation.

** Input resistor and cap are for test only. They are NOT necessary for normal operation.

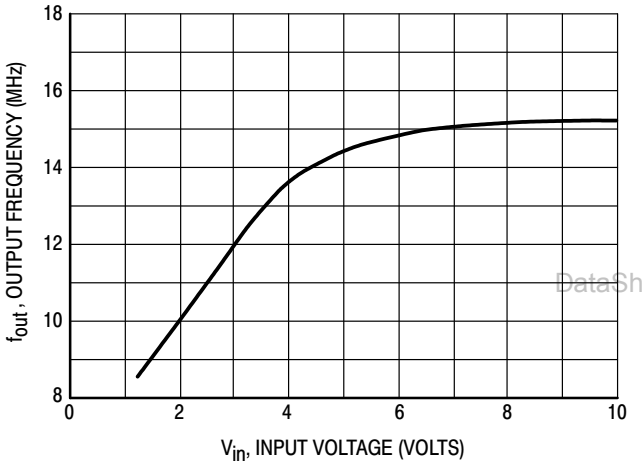
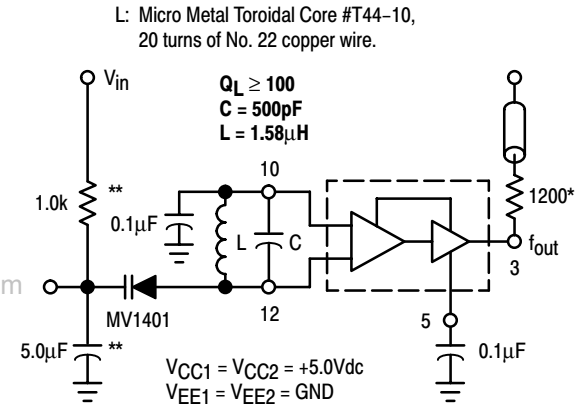


Figure 6.



* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT−070−50 or equivalent. NOT used in normal operation.

** Input resistor and cap are for test only. They are NOT necessary for normal operation.

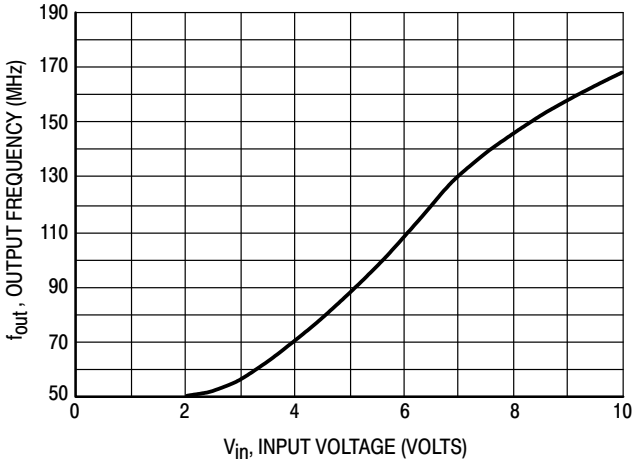
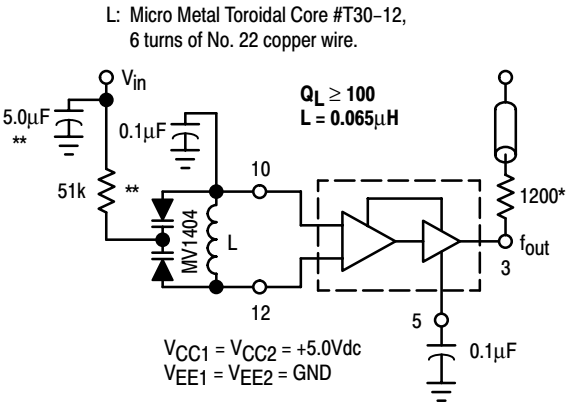


Figure 7.



* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT−070−50 or equivalent. NOT used in normal operation.

** Input resistor and cap are for test only. They are NOT necessary for normal operation.

Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figure 5., Figure 6., and Figure 7. Figure 5. and Figure 7. show transfer characteristics employing only the capacitance of the varactor diode (plus the input capacitance of the oscillator, 6.0pF typical). 6. illustrates the oscillator operating in a voltage controlled mode with the output frequency range limited. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1.0kΩ resistor in Figure 5. and Figure 6. is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased. The larger–valued resistor (51kΩ) in Figure 7. is required to provide isolation for the high–impedance junctions of the two varactor diodes.

The tuning range of the oscillator in the voltage controlled mode may be calculated as:

$$\frac{f_{max}}{f_{min}} = \frac{\sqrt{C_D(max) + C_S}}{\sqrt{C_D(min) + C_S}}$$

$$\text{where} \quad f_{min} = \frac{1}{2\pi\sqrt{L(C_D(max) + C_S)}}$$

CS = shunt capacitance (input plus external capacitance)
CD = varactor capacitance as a function of bias voltage

Good RF and low–frequency bypassing is necessary on the power supply pins.

Capacitors (C1 and C2 of Figure 3.) should be used to bypass the AGC point and the VCO input (varactor diode), guaranteeing only dc levels at these points.

For output frequency operation between 1.0MHz and 50MHz a 0.1μF capacitor is sufficient for C1 and C2. At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. At high frequencies the value of bypass capacitors depends directly upon the physical layout of the system. All bypassing should be as close to the package pins as possible to minimize unwanted lead inductance.

The peak–to–peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the MC100EL1648, a series resistor is tied from the AGC point to the most negative power potential (ground if +5.0 volt supply is used, –5.2 volts if a negative supply is used) as shown in Figure 9.

At frequencies above 100 MHz typ, it may be desirable to increase the tank circuit peak–to–peak voltage in order to shape the signal at the output of the MC100EL1648. This is accomplished by tying a series resistor (1.0kΩ minimum) from the AGC to the most positive power potential (+5.0 volts if a +5.0 volt supply is used, ground if a –5.2 volt supply is used). Figure 10. illustrates this principle.

APPLICATIONS INFORMATION

The phase locked loop shown in Figure 8. illustrates the use of the MC100EL1648 as a voltage controlled oscillator. The figure illustrates a frequency synthesizer useful in tuners for FM broadcast, general aviation, maritime and land/mobile communications, amateur and CB receivers. The system operates from a single +5.0Vdc supply, and requires no internal translations, since all components are compatible.

Frequency generation of this type offers the advantages of single crystal operation, simple channel selection, and elimination of special circuitry to prevent harmonic lockup. Additional features include dc digital switching (preferable over RF switching with a multiple crystal system), and a broad range of tuning (up to 150MHz, the range being set by the varactor diode).

The output frequency of the synthesizer loop is determined by the reference frequency and the number programmed at the programmable counter; $f_{out} = Nf_{ref}$. The channel spacing is equal to frequency (f_{ref}).

Figure 9. shows the MC100EL1648 in the variable frequency mode operating from a +5.0Vdc supply. To obtain a sine wave at the output, a resistor is added from the AGC circuit (pin 5) to V_{EE}.

Figure 10. shows the MC100EL1648 in the variable frequency mode operating from a +5.0Vdc supply. To extend the useful range of the device (maintain a square wave output above 175Mhz), a resistor is added to the AGC circuit at pin 5 (1.0 kohm minimum).

Figure 11. shows the MC100EL1648 operating from +5.0Vdc and +9.0Vdc power supplies. This permits a higher voltage swing and higher output power than is possible from the ECL output (pin 3). Plots of output power versus total collector load resistance at pin 1 are given in Figure 12. and Figure 13. for 100MHz and 10MHz operation. The total collector load includes R in parallel with R_p of L1 and C1 at resonance. The optimum value for R at 100MHz is approximately 850 ohms.

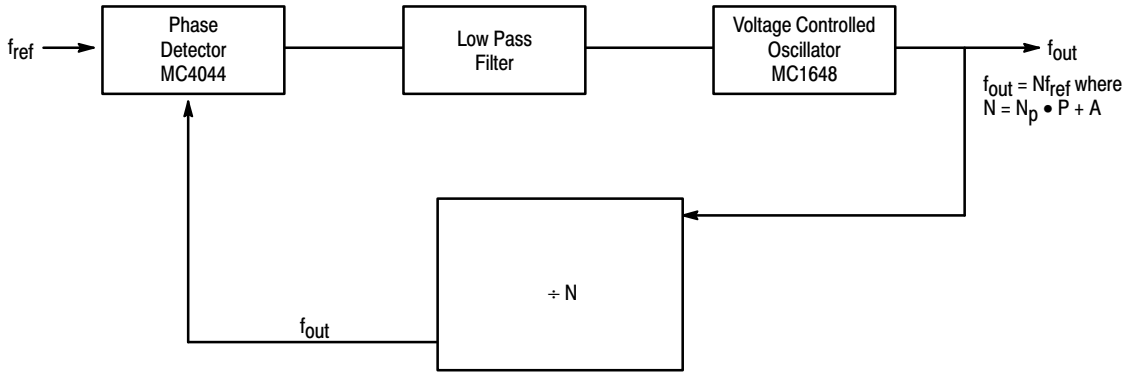


Figure 8. Typical Frequency Synthesizer Application

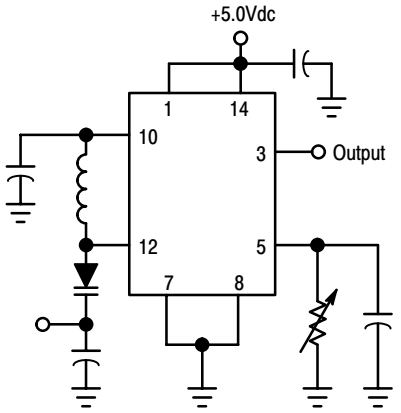


Figure 9. Method of Obtaining a Sine–Wave Output

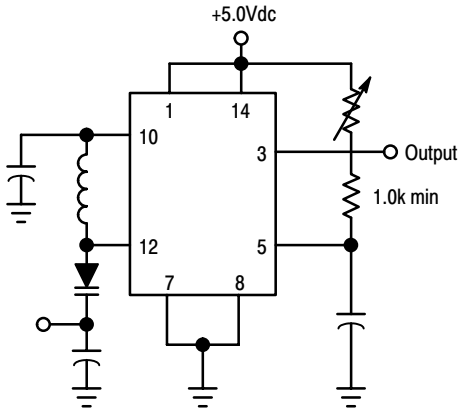


Figure 10. Method of Extending the Useful Range of the MC100EL1648 (Square Wave Output)

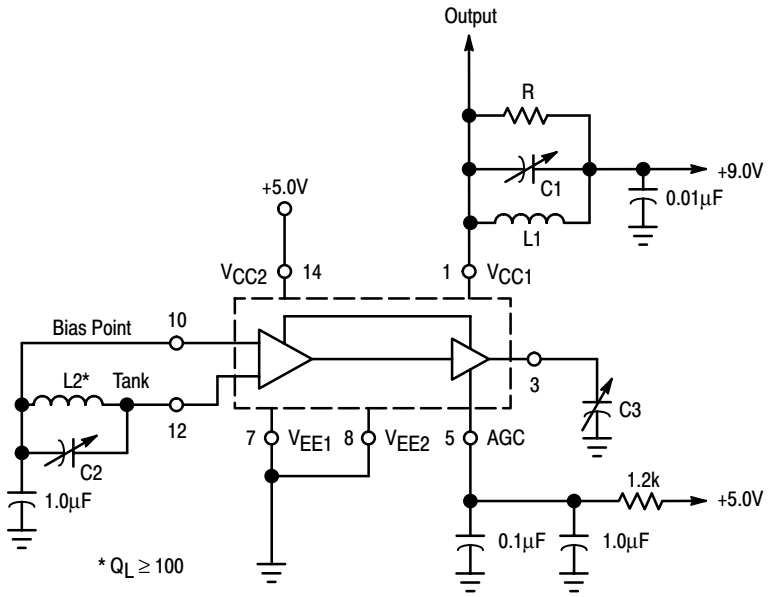
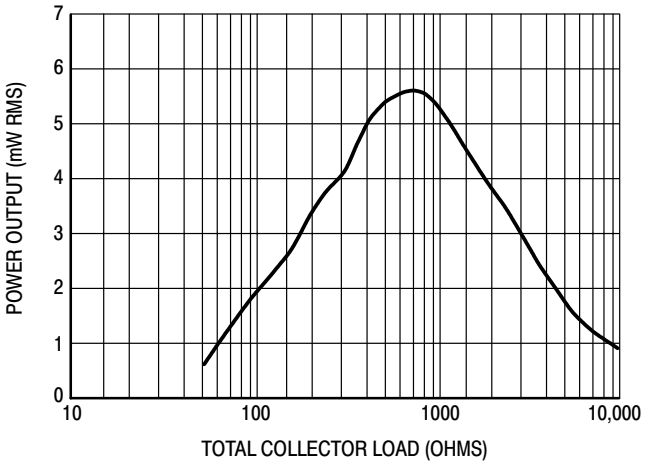


Figure 11. Circuit Used for Collector Output Operation



See test circuit, NO TAG, f = 100MHz
C3 = 3.0–35pF
Collector Tank
L1 = 0.22μH C1 = 1.0–7.0pF
R = 50Ω–10kΩ
R_P of L1 and C1 = 11kΩ @ 100MHz Resonance
Oscillator Tank
L2 = 4 turns #20 AWG 3/16” ID
C2 = 1.0–7.0pF

Figure 12. Power Output versus Collector Load

See test circuit, NO TAG, f = 10MHz
C3 = 470pF
Collector Tank
L1 = 2.7μH C1 = 24–200pF
R = 50Ω–10kΩ
R_P of L1 and C1 = 6.8kΩ @ 10MHz Resonance
Oscillator Tank
L2 = 2.7μH
C2 = 16–150pF

Figure 13. Power Output versus Collector Load

CHAPTER 3
Low Voltage ECLinPS Data Sheets

MC100LVE111

3.3V ECL 1:9 Differential Clock Driver

The MC100LVE111 is a low skew 1-to-9 differential driver, designed with clock distribution in mind. The MC100LVE111's function and performance are similar to the popular MC100E111, with the added feature of low voltage operation. It accepts one signal input, which can be either differential or single-ended if the V_{BB} output is used. The signal is fanned out to 9 identical differential outputs.

The LVE111 is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate to gate skew within a device, and empirical modeling is used to determine process control limits that ensure consistent t_{pd} distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50 Ω, even if only one side is being used. In most applications, all nine differential pairs will be used and therefore terminated. In the case where fewer than nine pairs are used, it is necessary to terminate at least the output pairs on the same package side as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20 ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

The MC100LVE111, as with most other ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the LVE111 to be used for high performance clock distribution in +3.3 V systems. Designers can take advantage of the LVE111's performance to distribute low skew clocks across the backplane or the board. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For systems incorporating GTL, parallel termination offers the lowest power by taking advantage of the 1.2 V supply as a terminating voltage. For more information on using PECL, designers should refer to Application Note AN1406/D.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- 200 ps Part-to-Part Skew
- 50 ps Output-to-Output Skew
- ESD Protection: >2 KV HBM, >200 V MM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC} = 3.0 V to 3.8 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = –3.0 V to –3.8 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8",
  Oxygen Index 28 to 34
- Transistor Count = 250 devices

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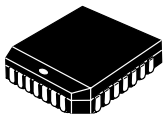
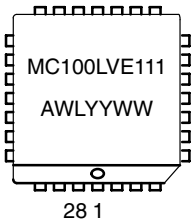


PLCC–28
FN SUFFIX
CASE 776

MARKING DIAGRAM*



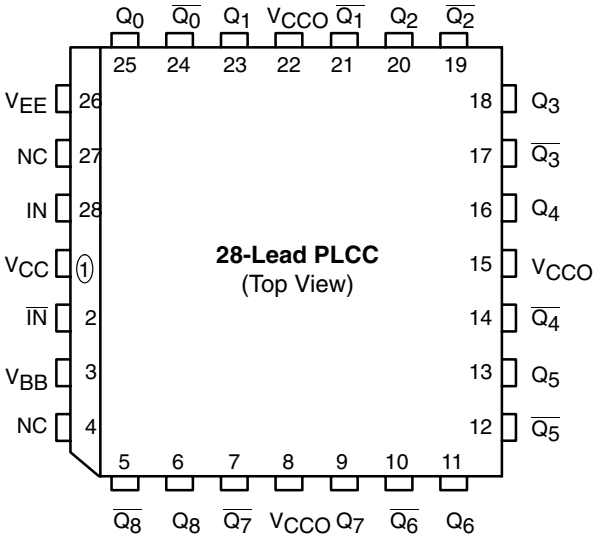
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

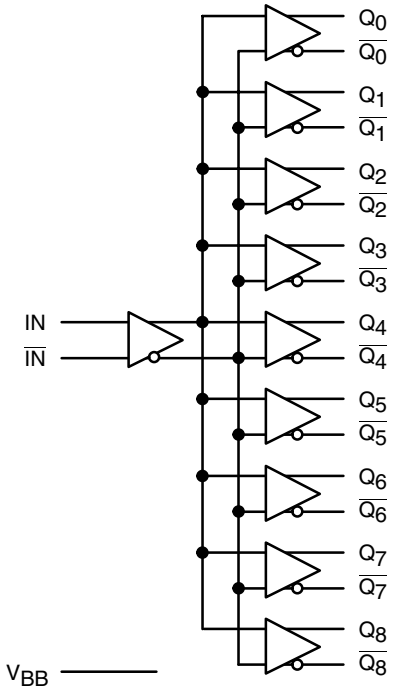
Device	Package	Shipping
MC100LVE111FN	PLCC–28	37 Units/Rail
MC100LVE111FNR2	PLCC–28	500 Units/Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC SYMBOL



PIN DESCRIPTION

PIN	FUNCTION
IN, $\overline{IN}$	ECL Differential Input Pair
Q_0, $\overline{Q_0}$–Q_8, $\overline{Q_8}$	ECL Differential Outputs
V_{BB}	Reference Voltage Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		55	66		55	66		65	78	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2345	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1490	1595	1680	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1490		1825	1490		1825	1490		1825	mV
V_{BB}	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	1.8		2.9	1.8		2.9	1.8		2.9	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. V_{IHCMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{PP}(min).

LVNECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		55	66		55	66		65	78	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–955	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1810	–1705	–1620	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–1.5		–0.4	–1.5		–0.4	–1.5		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. V_{IHCMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{PP}(min).

AC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output IN (differential) (Note 2.) IN (single-ended) (Note 3.)	 400 350		 650 700	 440 390		 630 680	 445 395		 635 685	ps
t_{skew}	Within-Device Skew (Note 4.) Part-to-Part Skew (Diff)			50 250			50 200			50 200	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 5.)	500		1000	500		1000	500		1000	mV
t_r/t_f	Output Rise/Fall Time (20%–80%)	200		600	200		600	200		600	ps

1. V_{EE} can vary ±0.3 V.
2. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
3. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
4. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
5. V_{PP}(min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP}(min) is AC limited for the E111 as a differential input as low as 50 mV will still produce full ECL levels at the output.

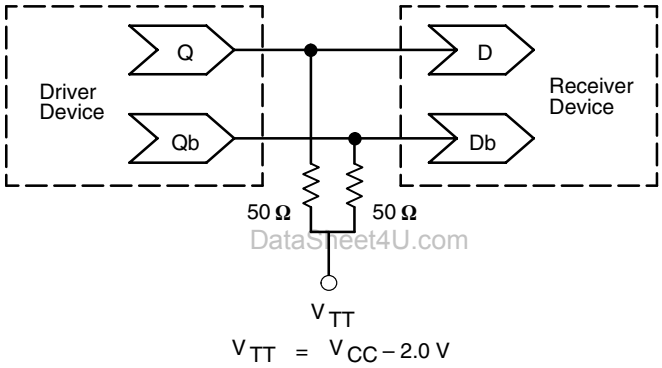


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels

AN1405 – ECL Clock Distribution Techniques

AN1406 – Designing with PECL (ECL at +5.0 V)

AN1503 – ECLinPS I/O SPICE Modeling Kit

AN1504 – Metastability and the ECLinPS Family

AN1560 – Low Voltage ECLinPS SPICE Modeling Kit

AN1568 – Interfacing Between LVDS and ECL

AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit

AN1650 – Using Wire–OR Ties in ECLinPS Designs

AN1672 – The ECL Translator Guide

AND8001 – Odd Number Counters Design

AND8002 – Marking and Date Codes

AND8020 – Termination of ECL Logic Devices

MC100LVE164

3.3V ECL 16:1 Multiplexer

The MC100LVE164 is a 16:1 multiplexer with a differential output. The select inputs (SEL0, 1, 2, 3) control which one of the sixteen data inputs (A0 – A15) is propragated to the output. The device is functionally equivalent to the MC100E164 except it operates from a 3.3 V supply. The device is packaged in the 32–lead TQFP. The TQFP has a 7x7 mm body with a 0.8 mm lead pitch.

Special attention to the design layout results in a typical skew between the 16 inputs of only 50 ps.

- 850 ps Data Input to Output
- Differential Output
- ESD Protection: >2 KV HBM, >200 V MM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 3.0 V to 3.8 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –3.0 V to –3.8 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 2
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 307 devices

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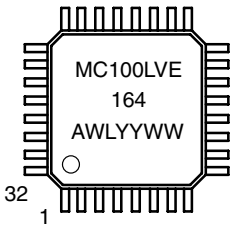
TQFP
FA SUFFIX
CASE 873A

MARKING DIAGRAM*



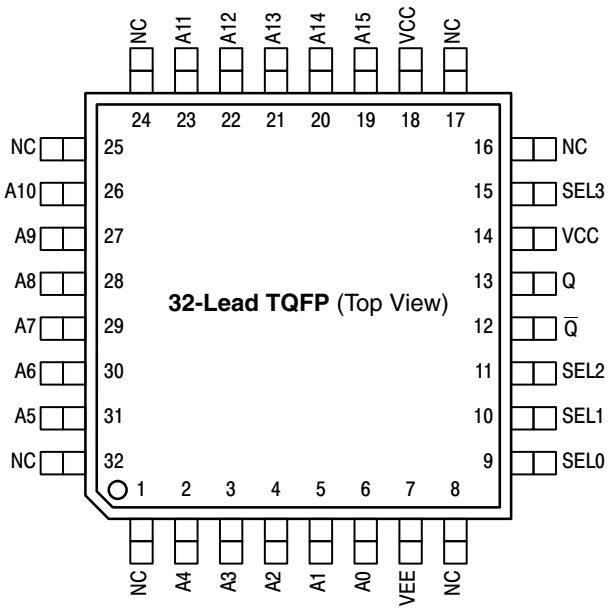
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

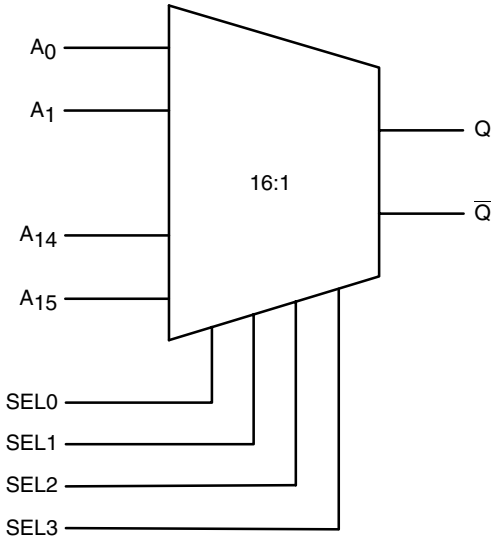
ORDERING INFORMATION

Device	Package	Shipping
MC100LVE164FA	TQFP	250 Units/Tray
MC100LVE164FAR2	TQFP	2000 Tape & Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



LOGIC DIAGRAM



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

PIN	FUNCTION
$A_0 - A_{15}$	ECL Data Inputs
SEL[0:3]	ECL Select Inputs
Q, $\overline{Q}$	ECL Differential Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

FUNCTION TABLE

SEL3	SEL2	SEL1	SEL0	Data
L	L	L	L	A0
L	L	L	H	A1
L	L	H	L	A2
L	L	H	H	A3
L	H	L	L	A4
L	H	L	H	A5
L	H	H	L	A6
L	H	H	H	A7
H	L	L	L	A8
H	L	L	H	A9
H	L	H	L	A10
H	L	H	H	A11
H	H	L	L	A12
H	H	L	H	A13
H	H	H	L	A14
H	H	H	H	A15

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	32 TQFP 32 TQFP	80 55	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	32 TQFP	12 to 17	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		34	45		34	45		37	45	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1490		1825	1490		1825	1490		1825	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

LVNECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		34	45		34	45		37	45	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic		–40°C			25°C			85°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency			TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output	A Input	350	600	850	350	600	850	350	600	850	ps
		SEL0	500	700	900	500	700	900	500	700	900	
		SEL1	400	675	900	400	675	900	400	675	900	
		SEL2	400	675	900	400	675	900	400	675	900	
		SEL3	400	550	700	400	550	700	400	550	700	
t_{SKEW}	Within Device Skew (Note 2.)			75			50			50		ps
t_{JITTER}	Cycle–to–Cycle Jitter			TBD			TBD			TBD		ps
t_r t_f	Rise/Fall Times (20% – 80%)		275	400	550	275	400	550	275	400	550	ps

1. V_{EE} can vary ±0.3 V.
2. Within Device skew is defined as the difference in the A to Q delay between the 16 different A inputs.

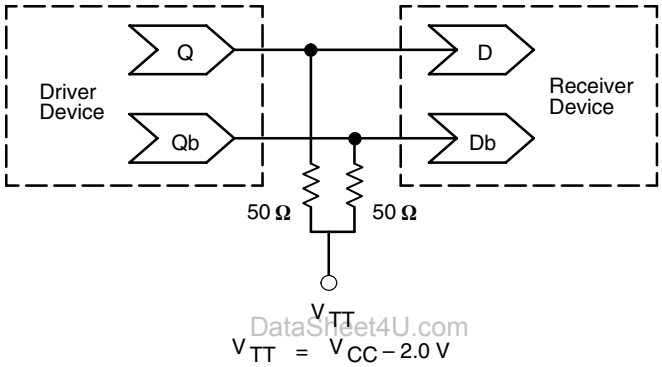


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405 – ECL Clock Distribution Techniques
AN1406 – Designing with PECL (ECL at +5.0 V)
AN1503 – ECLinPS I/O SPICE Modeling Kit
AN1504 – Metastability and the ECLinPS Family
AN1560 – Low Voltage ECLinPS SPICE Modeling Kit
AN1568 – Interfacing Between LVDS and ECL
AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650 – Using Wire–OR Ties in ECLinPS Designs
AN1672 – The ECL Translator Guide
AND8001 – Odd Number Counters Design
AND8002 – Marking and Date Codes
AND8020 – Termination of ECL Logic Devices

MC100LVE210

3.3V ECL Dual 1:4, 1:5 Differential Fanout Buffer

The MC100LVE210 is a low voltage, low skew dual differential ECL fanout buffer designed with clock distribution in mind. The device features two fanout buffers, a 1:4 and a 1:5 buffer, on a single chip. The device features fully differential clock paths to minimize both device and system skew. The dual buffer allows for the fanout of two signals through a single chip, thus reducing the skew between the two fundamental signals from a part–to–part skew down to an output–to–output skew. This capability reduces the skew by a factor of 4 as compared to using two LVE111's to accomplish the same task.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are identically terminated, even if only one side is being used. In most applications all nine differential pairs will be used and therefore terminated. In the case where fewer than nine pairs are used it is necessary to terminate at least the output pairs adjacent to the output pair being used in order to maintain minimum skew. Failure to follow this guideline will result in small degradations of propagation delay (on the order of 10–20 ps) of the outputs being used, while not catastrophic to most designs this will result in an increase in skew. Note that the package corners isolate outputs from one another such that the guideline expressed above holds only for outputs on the same side of the package.

The MC100LVE210, as with most ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the LVE210 to be used for high performance clock distribution in +3.3 V systems. Designers can take advantage of the LVE210's performance to distribute low skew clocks across the backplane or the board. In a PECL environment series or Thevenin line terminations are typically used as they require no additional power supplies, if parallel termination is desired a terminating voltage of V_{CC}–2.0 V will need to be provided. For more information on using PECL, designers should refer to Application Note AN1406/D.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- 200 ps Part–to–Part Skew
- 50 ps Typical Output–to–Output Skew
- The 100 Series Contains Temperature Compensation
- ESD Protection: >2 KV HBM, >200 V MM
- PECL Mode Operating Range: V_{CC}= 3.0 V to 3.8 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –3.0 V to –3.8 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8",
  Oxygen Index 28 to 34
- Transistor Count = 179 devices

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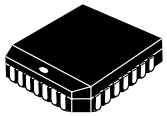
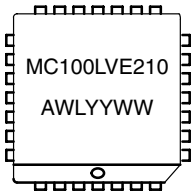
MARKING DIAGRAM*





PLCC–28
FN SUFFIX
CASE 776

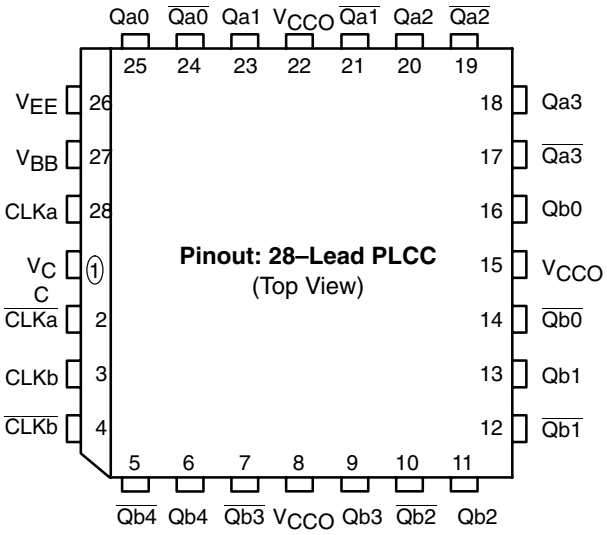
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

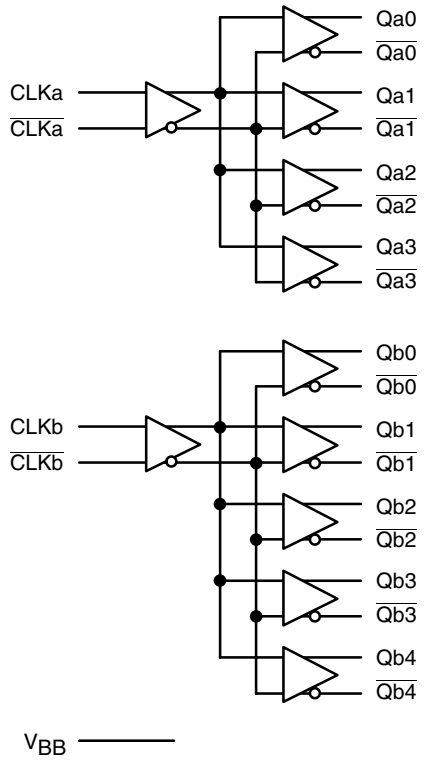
Device	Package	Shipping
MC100LVE210FN	PLCC–28	37 Units / Rail
MC100LVE210FNR2	PLCC–28	500 Tape & Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC SYMBOL



PIN DESCRIPTION

PIN	FUNCTION
CLKa, $\overline{CLKa}$	ECL Differential Input Pairs
CLKb, $\overline{CLKb}$	ECL Differential Input Pairs
Qa0:3, $\overline{Qa0:3}$	ECL Differential Outputs
Qb0:4, $\overline{Qb0:4}$	ECL Differential Outputs
V_{BB}	Reference Voltage Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current			55			55			65	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1490		1825	1490		1825	1490		1825	mV
V_{BB}	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	1.8		2.9	1.8		2.9	1.8		2.9	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. V_{IHCMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{PP}(min).

LVNECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current			55			55			65	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–1.5		–0.4	–1.5		–0.4	–1.5		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. V_{IHCMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{PP}(min).

AC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output IN (differential) (Note 2.) IN (single–ended) (Note 3.)	 475 400		 675 700	 500 450		 700 750	 500 450		 700 750	ps
t_{skew}	Within–Device Skew (Note 4.) Qa to Qb Qa to Qa,Qb to Qb Part–to–Part Skew (Diff)		50 50	75 75 200		50 30	75 50 200		50 30	75 50 200	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 5.)	500		1000	500		1000	500		1000	mV
t_r/t_f	Output Rise/Fall Time (20%–80%)	200		600	200		600	200		600	ps

1. V_{EE} can vary ±0.3 V.
2. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
3. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
4. The within–device skew is defined as the worst case difference between any two similar delay paths within a single device.
5. V_{PP}(min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP}(min) is AC limited for the LVE210 as a differential input as low as 50 mV will still produce full ECL levels at the output.

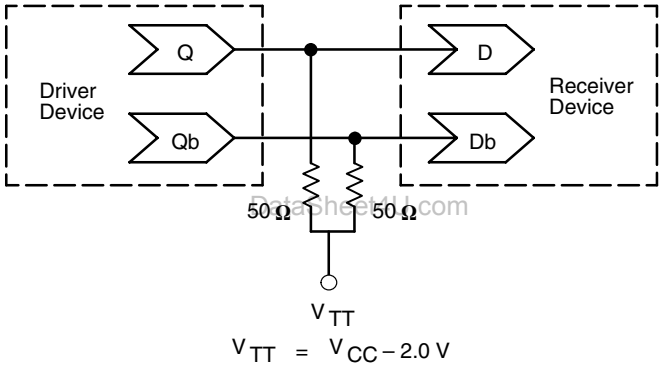


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels

AN1405 – ECL Clock Distribution Techniques

AN1406 – Designing with PECL (ECL at +5.0 V)

AN1503 – ECLinPS I/O SPICE Modeling Kit

AN1504 – Metastability and the ECLinPS Family

AN1560 – Low Voltage ECLinPS SPICE Modeling Kit

AN1568 – Interfacing Between LVDS and ECL

AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit

AN1650 – Using Wire–OR Ties in ECLinPS Designs

AN1672 – The ECL Translator Guide

AND8001 – Odd Number Counters Design

AND8002 – Marking and Date Codes

AND8020 – Termination of ECL Logic Devices

MC100LVE222

3.3V ECL 1:15 Differential ÷1/÷2 Clock Driver

The MC100LVE222 is a low skew 1:15 differential ÷1/÷2 ECL fanout buffer designed with clock distribution in mind. The LVECL/LVPECL input signal pairs can be differential or used single–ended (with VBB output reference bypassed and connected to the unused input of a pair). Either of two fully differential clock inputs may be selected. Each of the four output banks of 2, 3, 4, and 6 differential pairs may be independently configured to fanout 1X or 1/2X of the input frequency. The LVE222 specifically guarantees low output to output skew. Optimal design, layout, and processing minimize skew within a device and from lot to lot.

The fsel pins and CLK_Sel pin are asynchronous control inputs. Any changes may cause indeterminate output states requiring a MR pulse to resynchronize any 1/2X outputs.

To ensure that the tight skew specification is realized, both sides of any differential output pair need to be terminated identically even if only one side is being used. When fewer than all fifteen pairs are used, identically terminate all the output pairs on the same package side whether used or unused. If no outputs on a side are used, then leave all these outputs open (unterminated). This will maintain minimum output skew. Failure to do this will result in a 10–20 ps loss of skew margin (propagation delay) in the output(s) in use.

The MC100LVE222, as with most ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the LVE222 to be used for high performance clock distribution in +3.3 V systems. Designers can take advantage of the LVE222's performance to distribute low skew clocks across the backplane or the board. In a PECL environment series or Thevenin line, terminations are typically used as they require no additional power supplies. All power supply pins must be connected. For more information on using PECL, designers should refer to Application Note AN1406/D. For a SPICE model, see Application Note AN1560/D.

- 200 ps Part–to–Part Skew
- 50 ps Output–to–Output Skew
- Selectable 1x or 1/2x Frequency Outputs
- ESD Protection: >2 KV HBM, >200 V MM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 3.0 V to 3.8 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –3.0 V to –3.8 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 2
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8",
  Oxygen Index 28 to 34
- Transistor Count = 684 devices

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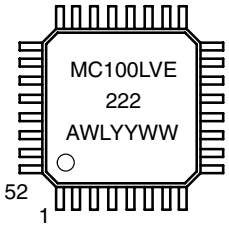
MARKING DIAGRAM*

TQFP
FA SUFFIX
CASE 848D



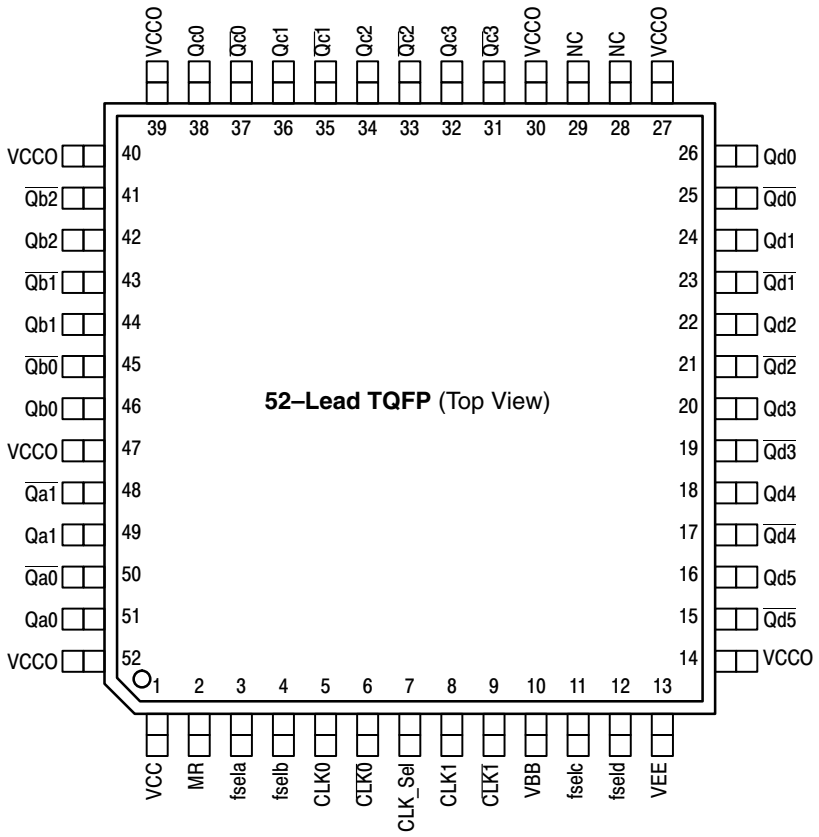
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVE222FA	TQFP	160 Units/Tray
MC100LVE222FAR2	TQFP	1500 Tape & Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



52–Lead TQFP (Top View)

FUNCTION TABLE

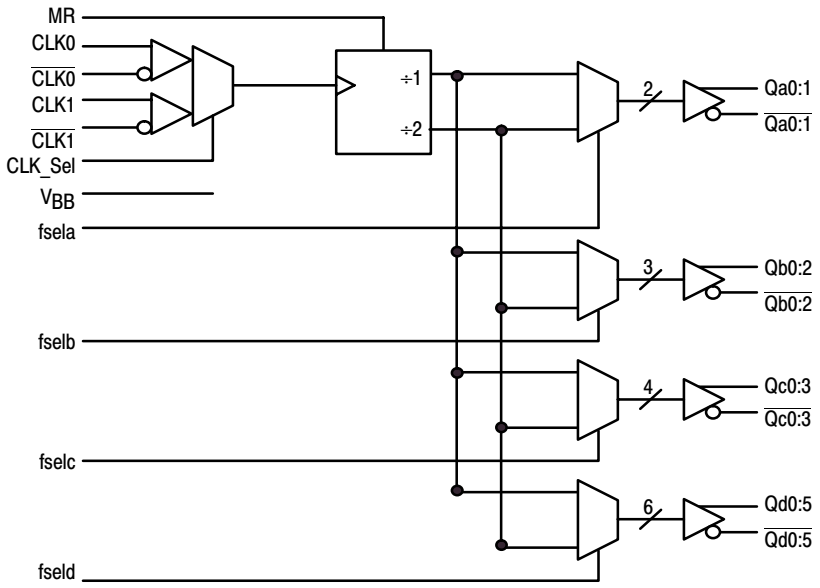
Input	Function	
	L	H
MR	Active	Reset
CLK_Sel	CLK0	CLK1
fseln	÷1	÷2

PIN DESCRIPTION

PIN	FUNCTION
CLK0, $\overline{\text{CLK0}}$	ECL Differential Input Clock
CLK1, $\overline{\text{CLK1}}$	ECL Differential Input Clock
CLK_Sel	ECL Clock Select
MR	ECL Master Reset
Qa0:1, $\overline{\text{Qa0:1}}$	ECL Differential Outputs
Qb0:2, $\overline{\text{Qb0:2}}$	ECL Differential Outputs
Qc0:3, $\overline{\text{Qc0:3}}$	ECL Differential Outputs
Qd0:5, $\overline{\text{Qd0:5}}$	ECL Differential Outputs
fseln	ECL ÷1 or ÷2 Select
V_{BB}	Reference Voltage Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC SYMBOL



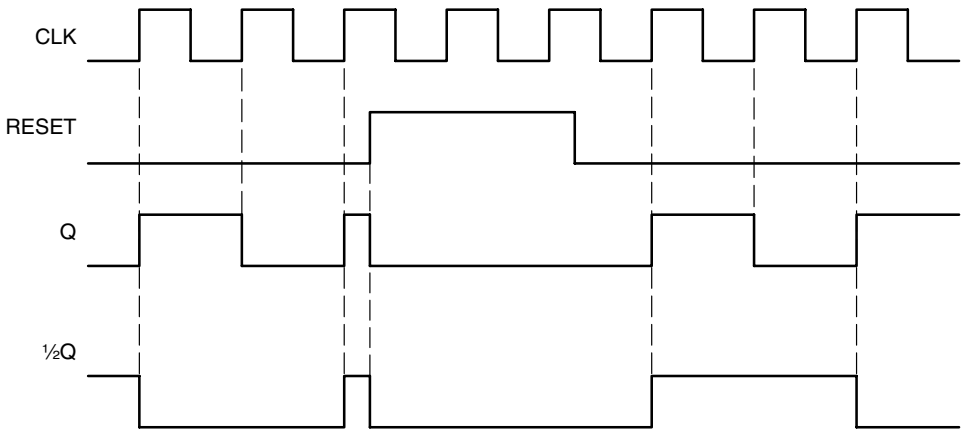


Figure 1. Timing Diagram

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	52 TQFP 52 TQFP	70 48	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	52 TQFP	TBD	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		122	136		122	136		125	139	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1490		1825	1490		1825	1490		1825	mV
V_{BB}	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.) Vpp < 500 mV Vpp ≧ 500 mV	 1.3 1.6		 2.9 2.9	 1.2 1.5		 2.9 2.9	 1.2 1.5		 2.9 2.9	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current Others $\overline{CLK0}$, $\overline{CLK1}$	0.5 –300			0.5 –300			0.5 –300			μA μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. V_{IHCMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{PP}(min).

LVNECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		122	136		122	136		125	139	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.) Vpp < 500 mV Vpp ≧ 500 mV	 –2.0 –1.7		 –0.4 –0.4	 –2.1 –1.8		 –0.4 –0.4	 –2.1 –1.8		 –0.4 –0.4	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current Others $\overline{CLK0}$, $\overline{CLK1}$	0.5 –300			0.5 –300			0.5 –300			μA μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. V_{IHCMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{PP}(min).

AC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output IN (differential) (Note 2.) IN (single–ended) (Note 3.) MR	 1040 990 1100	 1140 1140 1250	 1240 1290 1400	 1080 1030 1170	 1180 1180 1320	 1280 1330 1470	 1120 1070 1220	 1220 1220 1370	 1320 1370 1520	ps
t_{skew}	Within–Device Skew (Note 4.) Part–to–Part Skew (Diff)			50 200			50 200			50 200	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 5.)	400		1000	400		1000	400		1000	mV
t_r/t_f	Output Rise/Fall Time 20%–80%	200		600	200		600	200		600	ps

1. V_{EE} can vary ±0.3 V.
2. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
3. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
4. The within–device skew is defined as the worst case difference between any two similar delay paths within a single device.
5. V_{PP}(min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP}(min) is AC limited for the LVE222. A differential input as low as 50 mV will still produce full ECL levels at the output.

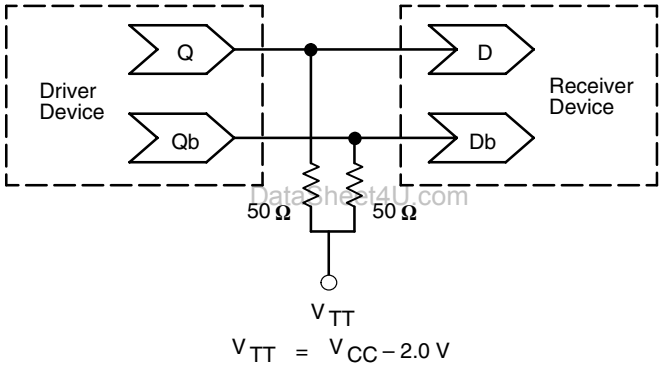


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels

AN1405 – ECL Clock Distribution Techniques

AN1406 – Designing with PECL (ECL at +5.0 V)

AN1503 – ECLinPS I/O SPICE Modeling Kit

AN1504 – Metastability and the ECLinPS Family

AN1560 – Low Voltage ECLinPS SPICE Modeling Kit

AN1568 – Interfacing Between LVDS and ECL

AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit

AN1650 – Using Wire–OR Ties in ECLinPS Designs

AN1672 – The ECL Translator Guide

AND8001 – Odd Number Counters Design

AND8002 – Marking and Date Codes

AND8020 – Termination of ECL Logic Devices

MC100LVE310

3.3V ECL 2:8 Differential Fanout Buffer

The MC100LVE310 is a low voltage, low skew 2:8 differential ECL fanout buffer designed with clock distribution in mind. The device features fully differential clock paths to minimize both device and system skew. The LVE310 offers two selectable clock inputs to allow for redundant or test clocks to be incorporated into the system clock trees.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50 Ω, even if only one side is being used. In most applications all eight differential pairs will be used and therefore terminated. In the case where fewer than eight pairs are used it is necessary to terminate at least the output pairs adjacent to the output pair being used in order to maintain minimum skew. Failure to follow this guideline will result in small degradations of propagation delay (on the order of 10–20 ps) of the outputs being used, while not catastrophic to most designs this will result in an increase in skew. Note that the package corners isolate outputs from one another such that the guideline expressed above holds only for outputs on the same side of the package.

The MC100LVE310, as with most ECL devices, can be operated from a positive V_{CC} supply in LVPECL mode. This allows the LVE310 to be used for high performance clock distribution in +3.3 V systems. Designers can take advantage of the LVE310's performance to distribute low skew clocks across the backplane or the board. In a PECL environment series or Thevenin line terminations are typically used as they require no additional power supplies, if parallel termination is desired a terminating voltage of V_{CC}–2.0 V will need to be provided. For more information on using PECL, designers should refer to Application Note AN1406/D.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- 200 ps Part–to–Part Skew
- 50 ps Output–to–Output Skew
- The 100 Series Contains Temperature Compensation
- ESD Protection: >2 KV HBM, >200 V MM
- PECL Mode Operating Range: V_{CC}= 3.0 V to 3.8 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –3.0 V to –3.8 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with All Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8",
  Oxygen Index 28 to 34
- Transistor Count = 212 devices

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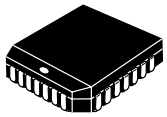
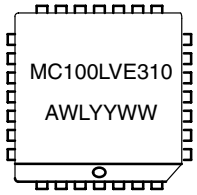
MARKING DIAGRAM



PLCC–28
FN SUFFIX
CASE 776

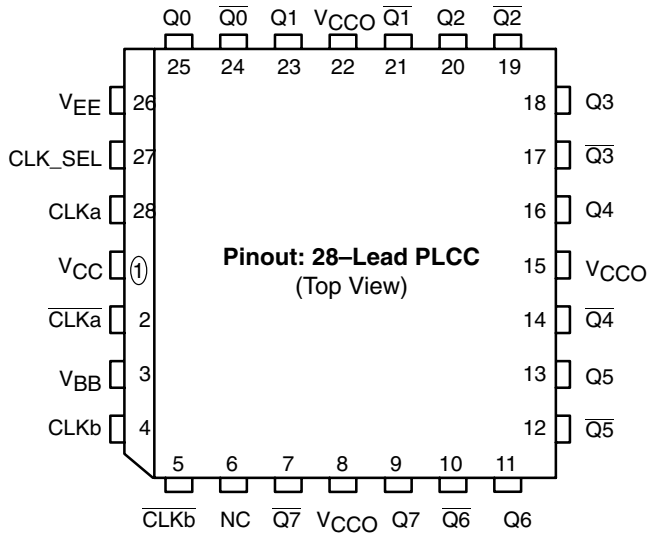


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

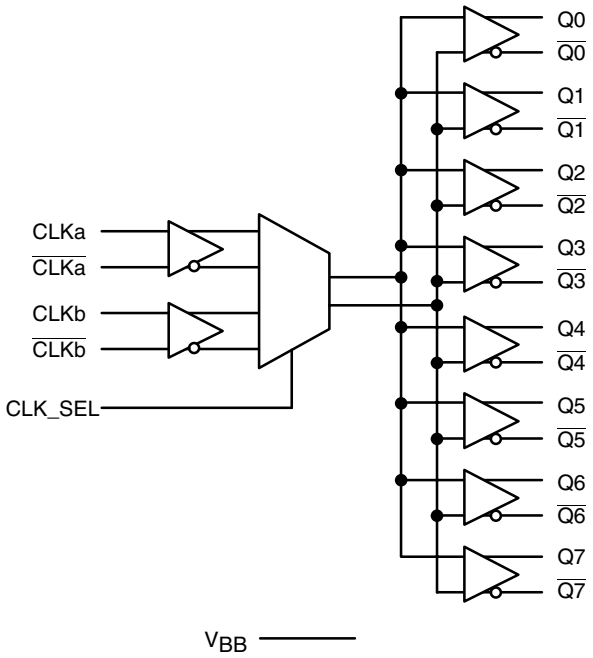
Device	Package	Shipping
MC100LVE310FN	PLCC–28	37 Units/Rail
MC100LVE310FNR2	PLCC–28	500 Units/Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



Warning: All V_{CC}, V_{CCO}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC SYMBOL



PIN DESCRIPTION

PIN	FUNCTION
CLKa, $\overline{CLKa}$; ,CLKb $\overline{CLKb}$	ECL Differential Input Clocks
Q0:7, $\overline{Q0:7}$	ECL Differential Outputs
CLK_SEL	ECL Input Clock Select
V_{BB}	Reference Voltage Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

CLK_SEL	Input Clock
L	CLKa Selected
H	CLKb Selected

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		55	60		55	60		65	70	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1490		1825	1490		1825	1490		1825	mV
V_{BB}	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	1.8		2.9	1.8		2.9	1.8		2.9	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. V_{IHCMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{PP}(min).

LVNECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		55	60		55	60		65	70	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–1.5		–0.4	–1.5		–0.4	–1.5		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. V_{IHCMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{PP}(min).

AC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output IN (differential) (Note 2.) IN (single–ended) (Note 3.)	 525 500		 725 750	 550 550		 750 800	 575 600		 775 850	ps
t_{skew}	Within–Device Skew (Note 4.) Part–to–Part Skew (Differential)			75 250			50 200			50 200	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 5.)	500		1000	500		1000	500		1000	mV
t_r/t_f	Output Rise/Fall Time (20%–80%)	200		600	200		600	200		600	ps

1. V_{EE} can vary ±0.3 V.
2. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
3. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
4. The within–device skew is defined as the worst case difference between any two similar delay paths within a single device.
5. V_{PP}(min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP}(min) is AC limited for the LVE310 as a differential input as low as 50 mV will still produce full ECL levels at the output.

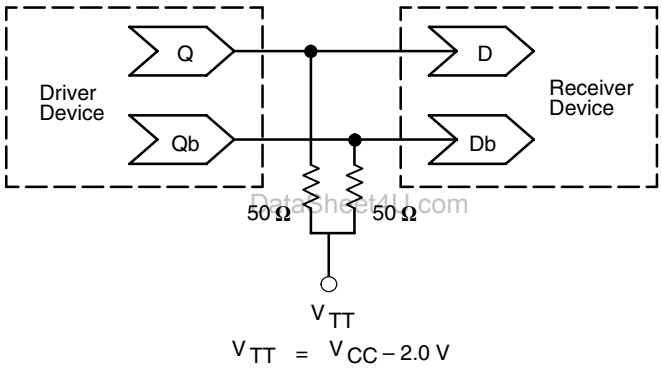


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels

AN1405 – ECL Clock Distribution Techniques

AN1406 – Designing with PECL (ECL at +5.0 V)

AN1503 – ECLinPS I/O SPICE Modeling Kit

AN1504 – Metastability and the ECLinPS Family

AN1560 – Low Voltage ECLinPS SPICE Modeling Kit

AN1568 – Interfacing Between LVDS and ECL

AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit

AN1650 – Using Wire–OR Ties in ECLinPS Designs

AN1672 – The ECL Translator Guide

AND8001 – Odd Number Counters Design

AND8002 – Marking and Date Codes

AND8020 – Termination of ECL Logic Devices

MC100LVEL01

3.3V ECL 4-Input OR/NOR

The MC100LVEL01 is a 4–input OR/NOR gate. The device is functionally equivalent to the EL01 device and works from a 3.3 V supply. With AC performance similar to the EL01 device, the LVEL01 is ideal for low voltage applications which require the ultimate in AC performance.

- 370 ps Propagation Delay
- High Bandwidth Output Transitions
- ESD Protection: >2 KV HBM, >200 V MM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 3.0 V to 3.8 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –3.0 V to –3.8 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with All Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 83 devices

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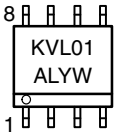
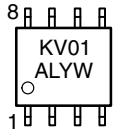
MARKING DIAGRAMS*

SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



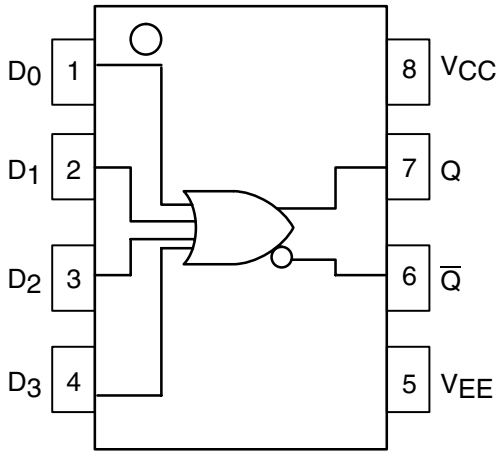
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL01D	SO–8	98 Units / Rail
MC100LVEL01DR2	SO–8	2500 / Reel
MC100LVEL01DT	TSSOP–8	98 Units / Rail
MC100LVEL01DTR2	TSSOP–8	2500 / Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
D0–D3	ECL Data Inputs
Q, $\overline{Q}$	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44 ± 5%	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		15	20		15	20		17	22	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage	1490		1825	1490		1825	1490		1825	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

LVNECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		15	20		15	20		17	22	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage	–1810		–1475	–1810		–1475	–1810		–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output	210	310	510	270	370	470	290	390	490	ps
t_{skew}	Within Device Skew		40	100		40	100		40	100	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	120	225	320	120	225	320	120	225	320	ps

1. V_{EE} can vary ±0.3 V.

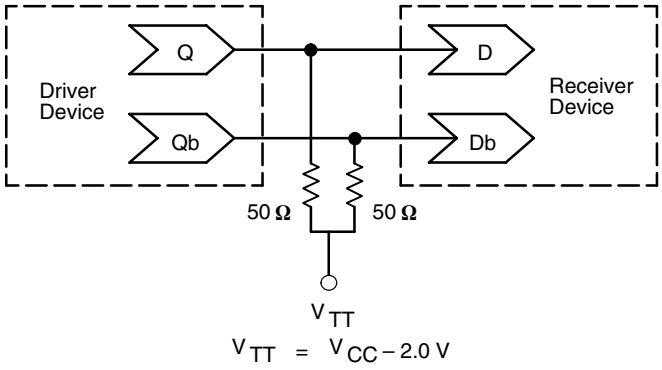


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC100LVEL05

3.3V ECL 2-Input Differential AND/NAND

The MC100LVEL05 is a 2-input differential AND/NAND gate. The device is functionally equivalent to the MC100EL05 device and operates from a 3.3 V supply voltage. With propagation delays and output transition times equivalent to the EL05, the LVEL05 is ideally suited for those applications which require the ultimate in AC performance at low voltage power supplies.

Because a negative 2-input NAND is equivalent to a 2-input OR function, the differential inputs and outputs of the device allows the LVEL05 to also be used as a 2-input differential OR/NOR gate.

- 340 ps Propagation Delay
- High Bandwidth Output Transitions
- ESD Protection: >4 KV HBM, >200 V MM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 3.0 V to 3.8 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –3.0 V to –3.8 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with All Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 69 devices

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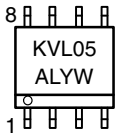
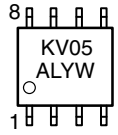
MARKING DIAGRAMS*

SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

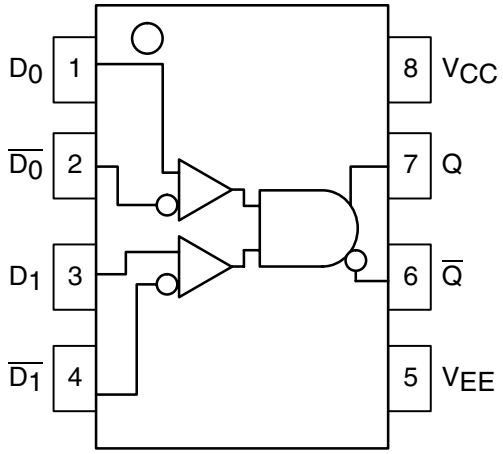
*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL05D	SO–8	98 Units / Rail
MC100LVEL05DR2	SO–8	2500 / Reel
MC100LVEL05DT	TSSOP–8	98 Units / Rail
MC100LVEL05DTR2	TSSOP–8	2500 / Reel

MC100LVEL05

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
D0, $\overline{D0}$; D1, $\overline{D1}$	ECL Data Inputs
Q, $\overline{Q}$	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44 ± 5%	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		18	25		18	25		19	26	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1490		1825	1490		1825	1490		1825	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.) Vpp < 500 mV Vpp ≧ 500 mV	 1.2 1.5		 2.9 2.9	 1.1 1.4		 2.9 2.9	 1.1 1.4		 2.9 2.9	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V.

LVNECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		18	25		18	25		19	26	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.) Vpp < 500 mV Vpp ≧ 500 mV	 –2.1 –1.8		 –0.4 –0.4	 –2.2 –1.9		 –0.4 –0.4	 –2.2 –1.9		 –0.4 –0.4	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V.

AC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output	240	260	440	240	340	440	250		450	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 2.)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	100		320	100	210	320	100		320	ps

1. V_{EE} can vary ±0.3 V.
2. V_{PP}(min) is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈40.

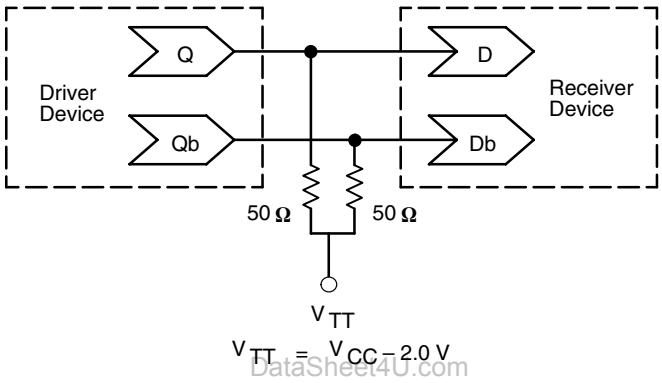


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405 – ECL Clock Distribution Techniques
AN1406 – Designing with PECL (ECL at +5.0 V)
AN1503 – ECLinPS I/O SPICE Modeling Kit
AN1504 – Metastability and the ECLinPS Family
AN1560 – Low Voltage ECLinPS SPICE Modeling Kit
AN1568 – Interfacing Between LVDS and ECL
AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650 – Using Wire–OR Ties in ECLinPS Designs
AN1672 – The ECL Translator Guide
AND8001 – Odd Number Counters Design
AND8002 – Marking and Date Codes
AND8020 – Termination of ECL Logic Devices

MC100LVEL11

3.3V ECL 1:2 Differential Fanout Buffer

The MC100LVEL11 is a differential 1:2 fanout buffer. The device is functionally similar to the E111 device but with higher performance capabilities. Having within-device skews and output transition times significantly improved over the E111, the LVEL11 is ideally suited for those applications which require the ultimate in AC performance.

The differential inputs of the LVEL11 employ clamping circuitry to maintain stability under open input conditions. If the inputs are left open (pulled to V_{EE}) the Q outputs will go LOW.

- 330 ps Propagation Delay
- 5 ps Skew Between Outputs
- High Bandwidth Output Transitions
- ESD Protection: >4 KV HBM, >200 V MM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 3.0 V to 3.8 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE} = –3.0 V to –3.8 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 63 devices

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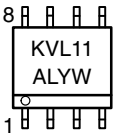
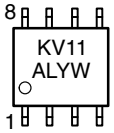
MARKING DIAGRAMS*

SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



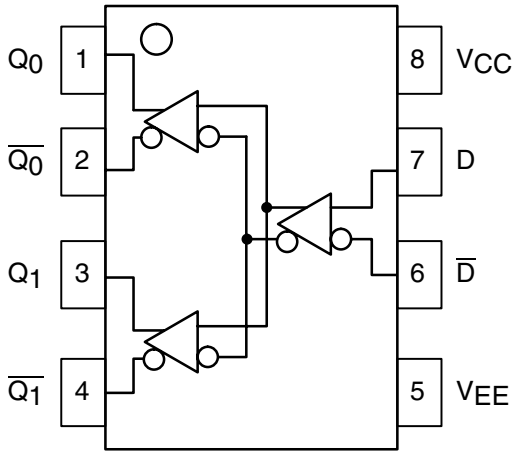
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL11D	SO–8	98 Units / Rail
MC100LVEL11DR2	SO–8	2500 / Reel
MC100LVEL11DT	TSSOP–8	98 Units / Rail
MC100LVEL11DTR2	TSSOP–8	2500 / Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
Q0, $\overline{Q0}$; Q1, $\overline{Q1}$	ECL Data Outputs
D, $\overline{D}$	ECL Data Inputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44 ± 5%	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		24	28		24	28		25	30	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1490		1825	1490		1825	1490		1825	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.) Vpp < 500 mV Vpp ≧ 500 mV	 1.2 1.4		 3.1 3.1	 1.1 1.3		 3.1 3.1	 1.1 1.3		 3.1 3.1	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –600			0.5 –600			0.5 –600			μA μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

LVNECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		24	28		24	28		25	30	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.) Vpp < 500 mV Vpp ≧ 500 mV	 –2.1 –1.9		 –0.2 –0.2	 –2.2 –2.0		 –0.2 –0.2	 –2.2 –2.0		 –0.2 –0.2	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –600			0.5 –600			0.5 –600			μA μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency	1.0		2.0	1.0		2.0	1.0		2.0	GHz
t_{PLH} t_{PHL}	Propagation Delay to Output	235		385	255	330	405	285		435	ps
t_{SKEW}	Within-Device Skew (Note 2.) Duty Cycle Skew (Note 3.)		5 5	20 20		5 5	20 20		5 5	20 20	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 4.)	200		1000	200	1000		200	1000		mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	120		320	120	220	320	120		320	ps

1. V_{EE} can vary ±0.3 V.
2. Within-device skew defined as identical transitions on similar paths through a device.
3. Duty cycle skew is the difference between a TPLH and TPHL propagation delay through a device.
4. V_{PP}(min) is the minimum input swing for which AC parameters guaranteed. The device will function properly with input swings below 200 mV, however, AC delays may move outside of the specified range. The device has a DC gain of ≈40.

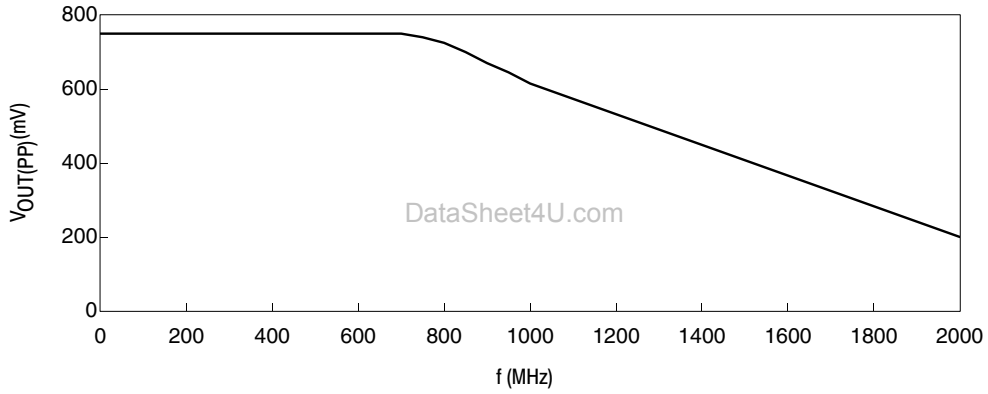


Figure 1. Output Swing versus Frequency

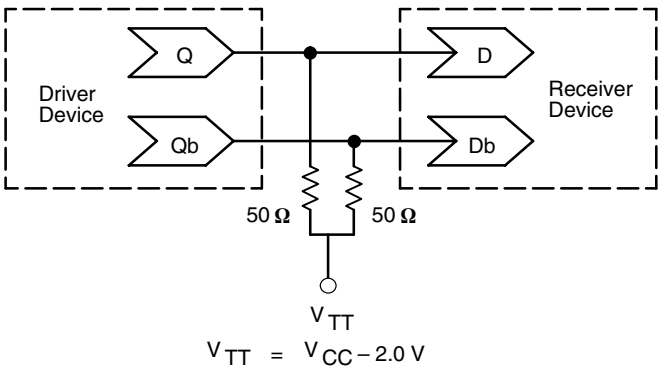


Figure 2. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC100LVEL12

3.3V ECL Low Impedance Driver

The MC100LVEL12 is a low impedance drive buffer. With two pairs of OR/NOR outputs the device is ideally suited for high drive applications such as memory addressing. The device is functionally equivalent to the EL12 device and operates from a 3.3 V power supply. With propagation delays equivalent to the EL12, the LVEL12 is ideally suited for those applications which require the ultimate in AC performance in a low voltage environment.

- 445 ps Propagation Delay
- Dual Outputs for 25 Ω Drive Applications
- ESD Protection: >4 KV HBM, > 200 V MM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC} = 3.0 V to 3.8 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = –3.0 V to –3.8 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with All Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 83 devices

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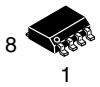
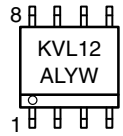
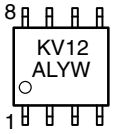
MARKING DIAGRAMS*



SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

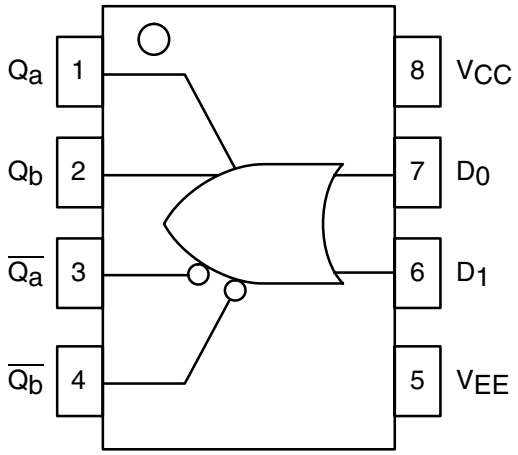
*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL12D	SO–8	98 Units / Rail
MC100LVEL12DR2	SO–8	2500 / Reel
MC100LVEL12DT	TSSOP–8	98 Units / Rail
MC100LVEL12DTR2	TSSOP–8	2500 / Reel

MC100LVEL12

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
D0, D1	ECL Data Inputs
Qa, $\overline{Qa}$; Qb, $\overline{Qb}$	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44 ± 5%	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		17	24		17	24		18	25	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage	1490		1825	1490		1825	1490		1825	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

LVNECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		17	24		17	24		18	25	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage	–1810		–1475	–1810		–1475	–1810		–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output	310		580	310	445	580	320		590	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	230	400	550	230	400	550	230	400	550	ps

1. V_{EE} can vary ±0.3 V.

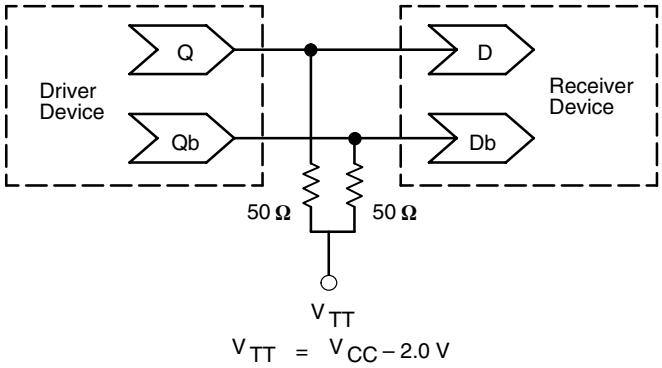


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC100LVEL13

3.3V ECL Dual 1:3 Fanout Buffer

The MC100LVEL13 is a dual, fully differential 1:3 fanout buffer. The Low Output–Output Skew of the device makes it ideal for distributing two different frequency synchronous signals.

The differential inputs have special circuitry which ensures device stability under open input conditions. When both differential inputs are left open the D input will pull down to V_{EE}, The $\overline{D}$ input will bias around $V_{CC}/2$ and the Q output will go LOW.

- 500 ps Typical Propagation Delays
- 50 ps Output–Output Skews
- ESD Protection: >2 KV HBM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 3.0 V to 3.8 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE} = –3.0 V to –3.8 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 143 devices

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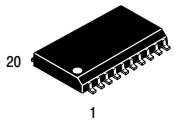
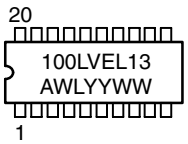
MARKING DIAGRAM



SO–20
DW SUFFIX
CASE 751D

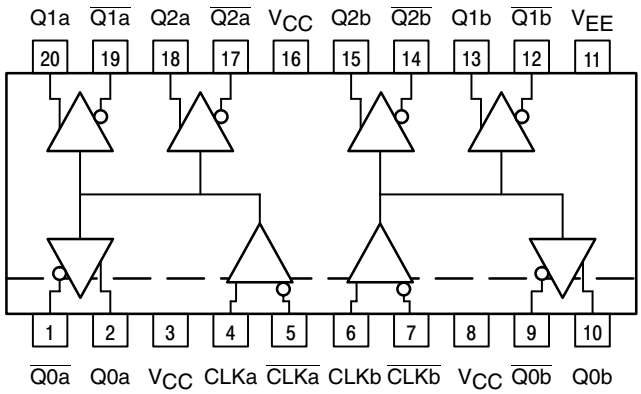


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL13DW	SOIC–20	38 Units/Rail
MC100LVEL13DWR2	SOIC–20	1000 Units/Reel

Logic Diagram and Pinout: 20–Lead SOIC (Top View)



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

PIN	FUNCTION
Qna, $\overline{Qna}$	ECL Differential Clock Outputs
Qnb, $\overline{Qnb}$	ECL Differential Clock Outputs
CLKn, $\overline{CLKn}$	ECL Differential Clock Inputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		30	38		30	38		32	40	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1490		1825	1490		1825	1490		1825	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.) Vpp < 500 mV Vpp ≧ 500 mV	 1.3 1.5		 2.9 2.9	 1.2 1.4		 2.9 2.9	 1.2 1.4		 2.9 2.9	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLKn $\overline{CLKn}$	0.5 –300			0.5 –300			0.5 –300			μA μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

LVNECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		30	38		30	38		32	40	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.) Vpp < 500 mV Vpp ≧ 500 mV	 –2.0 –1.8		 –0.4 –0.4	 –2.1 –1.9		 –0.4 –0.4	 –2.1 –1.9		 –0.4 –0.4	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLKn $\overline{CLKn}$	0.5 –300			0.5 –300			0.5 –300			μA μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay CLK to Q/$\overline{Q}$	410		600	430	500	620	450		640	ps
$t_{sk(O)}$	Output–Output Skew Any Qa to Qa, Any Qb to Qb Any Qa to Any Qb			 50 75			 50 75			 50 75	ps
t_{skew}	Duty Cycle Skew $\lvert t_{PLH} - t_{PHL} \rvert$			50			50			50	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 2.)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	230		500	230		500	230		500	ps

1. V_{EE} can vary ±0.3 V.
2. V_{PP}(min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

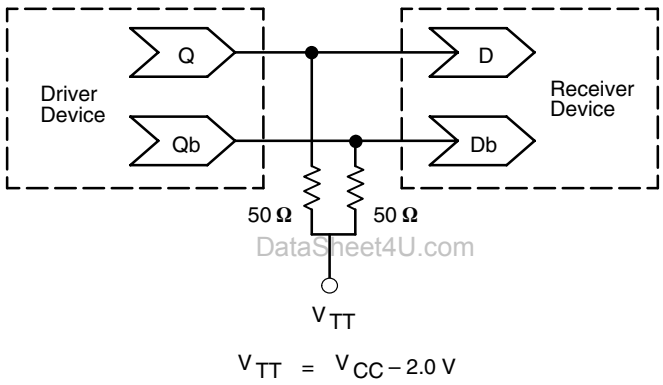


Figure 1. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405 – ECL Clock Distribution Techniques
AN1406 – Designing with PECL (ECL at +5.0 V)
AN1503 – ECLinPS I/O SPICE Modeling Kit
AN1504 – Metastability and the ECLinPS Family
AN1560 – Low Voltage ECLinPS SPICE Modeling Kit
AN1568 – Interfacing Between LVDS and ECL
AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650 – Using Wire–OR Ties in ECLinPS Designs
AN1672 – The ECL Translator Guide
AND8001 – Odd Number Counters Design
AND8002 – Marking and Date Codes
AND8020 – Termination of ECL Logic Devices

MC100LVEL14

3.3V ECL 1:5 Clock Distribution Chip

The MC100LVEL14 is a low skew 1:5 clock distribution chip designed explicitly for low skew clock distribution applications. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. The LVEL14 is functionally and pin compatible with the EL14 but is designed to operate in ECL or PECL mode for a voltage supply range of –3.0 V to –3.8 V (or 3.0 V to 3.8 V).

The LVEL14 features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open and pulled LOW by the input pulldown resistor) the SEL pin will select the differential clock input.

The common enable ($\overline{EN}$) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock, therefore all associated specification limits are referenced to the negative edge of the clock input.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- 50 ps Output-to-Output Skew
- Synchronous Enable/Disable
- Multiplexed Clock Input
- ESD Protection: >2 KV HBM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 3.0 V to 3.8 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE} = –3.0 V to –3.8 V
- Internal Input Pulldown Resistors on CLK
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 303 devices

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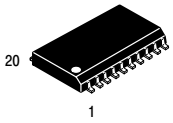
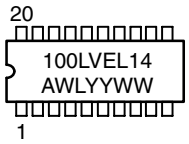


SOIC–20
DW SUFFIX
CASE 751D

MARKING DIAGRAM

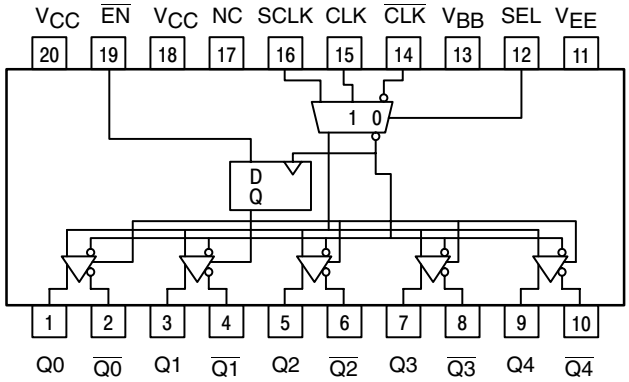


A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL14DW	SOIC–20	38 Units/Rail
MC100LVEL14DWR2	SOIC–20	1000 Units/Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

PIN	FUNCTION
CLK, $\overline{CLK}$	ECL Diff Clock Inputs
SCLK	ECL Scan Clock Input
$\overline{EN}$	ECL Sync Enable
SEL	ECL Clock Select Input
$Q_{0–4}$, $\overline{Q_{0–4}}$	ECL Diff Clock Outputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

FUNCTION TABLE

CLK	SCLK	SEL	$\overline{EN}$	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L*

*On next negative transition of CLK or SCLK
X = Don't Care

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		32	40		32	40		34	42	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1490		1825	1490		1825	1490		1825	mV
V_{BB}	Output Voltage Reference	1.87		2	1.95		2.05	1.99		2.11	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)										
	Vpp < 500 mV	1.3		2.9	1.2		2.9	1.2		2.9	V
	Vpp ≧ 500 mV	1.5		2.9	1.4		2.9	1.4		2.9	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current Others	0.5			0.5			0.5			μA
	$\overline{CLK}$	–300			–300			–300			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

LVNECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		32	40		32	40		34	42	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.43		–1.30	–1.35		–1.25	–1.31		–1.19	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)										
	Vpp < 500 mV	–2.0		–0.4	–2.1		–0.4	–2.1		–0.4	V
	Vpp ≧ 500 mV	–1.8		–0.4	–1.9		–0.4	–1.9		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current Others	0.5			0.5			0.5			μA
	$\overline{CLK}$	–300			–300			–300			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Prop Delay CLK to Q (Diff) CLK to Q (SE) SCLK to Q	520 470 470		720 770 770	580 530 530	680 680 680	780 830 830	630 580 580		830 880 880	ps
t_{SKEW}	Part-to-Part Skew Within-Device Skew (Note 2.)			200 50			200 50			200 50	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_S	Setup Time $\overline{EN}$	0			0			0			ps
t_H	Hold Time $\overline{EN}$	0			0			0			ps
V_{PP}	Input Swing CLK (Note 3.)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	230		500	230		500	230		500	ps

1. V_{EE} can vary ±0.3 V.
2. Skews are specified for identical LOW-to-HIGH or HIGH-to-LOW transitions.
3. $V_{PP(min)}$ is minimum input swing for which AC parameters guaranteed.

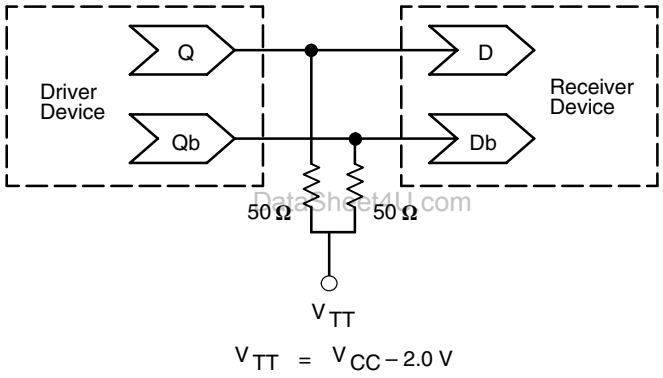


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405 – ECL Clock Distribution Techniques
AN1406 – Designing with PECL (ECL at +5.0 V)
AN1503 – ECLinPS I/O SPICE Modeling Kit
AN1504 – Metastability and the ECLinPS Family
AN1560 – Low Voltage ECLinPS SPICE Modeling Kit
AN1568 – Interfacing Between LVDS and ECL
AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650 – Using Wire–OR Ties in ECLinPS Designs
AN1672 – The ECL Translator Guide
AND8001 – Odd Number Counters Design
AND8002 – Marking and Date Codes
AND8020 – Termination of ECL Logic Devices

MC100LVEL16

3.3V ECL Differential Receiver

The MC100LVEL16 is a differential receiver. The device is functionally equivalent to the EL16 device, operating from a 3.3 V supply. The LVEL16 exhibits a wider V_{IHCMR} range than its EL16 counterpart. With output transition times and propagation delays comparable to the EL16 the LVEL16 is ideally suited for interfacing with high frequency sources at 3.3 V supplies.

Under open input conditions, the Q input will be pulled down to V_{EE} and the $\overline{Q}$ input will be biased to $V_{CC}/2$. This condition will force the Q output low.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- 300 ps Propagation Delay
- High Bandwidth Output Transitions
- ESD Protection: >2 KV HBM, > 200 V MM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 3.0 V to 3.8 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –3.0 V to –3.8 V
- Internal Input Pulldown Resistors on D, Pullup and Pulldown Resistors on $\overline{D}$
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 79 devices

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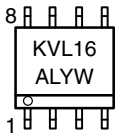
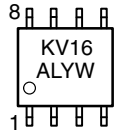
MARKING DIAGRAMS*

SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



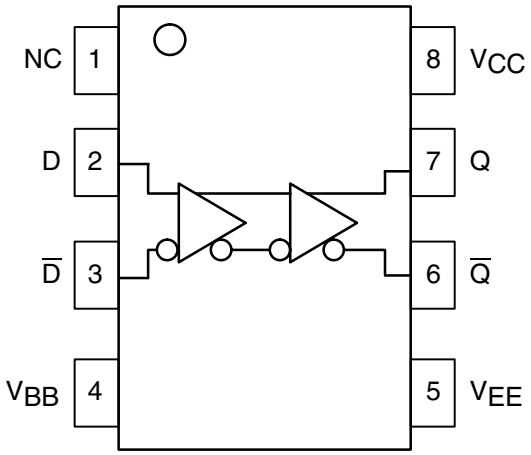
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL16D	SO–8	98 Units / Rail
MC100LVEL16DR2	SO–8	2500 / Reel
MC100LVEL16DT	TSSOP–8	98 Units / Rail
MC100LVEL16DTR2	TSSOP–8	2500 / Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
D, $\overline{D}$	ECL Data Inputs
Q, $\overline{Q}$	ECL Data Outputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44 ± 5%	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		17	23		17	23		18	24	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1490		1825	1490		1825	1490		1825	mV
V_{BB}	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.) Vpp < 500 mV Vpp ≧ 500 mV	 1.2 1.5		 2.9 2.9	 1.1 1.4		 2.9 2.9	 1.1 1.4		 2.9 2.9	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –600			0.5 –600			0.5 –600			μA μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.0
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

LVNECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		17	23		17	23		18	24	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.) Vpp < 500 mV Vpp ≧ 500 mV	 –2.1 –1.8		 –0.4 –0.4	 –2.2 –1.9		 –0.4 –0.4	 –2.2 –1.9		 –0.4 –0.4	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –600			0.5 –600			0.5 –600			μA μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output (Diff) (SE)	150 100	275 275	400 450	225 175	300 300	375 425	240 190	315 315	390 440	ps
t_{SKEW}	Duty Cycle Skew (Diff) (Note 2.)		5	30		5	20		5	20	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 3.)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	120	220	320	120	220	320	120	220	320	ps

1. V_{EE} can vary ±0.3 V.
2. Duty cycle skew is the difference between a TPLH and TPHL propagation delay through a device.
3. $V_{PP(}$min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

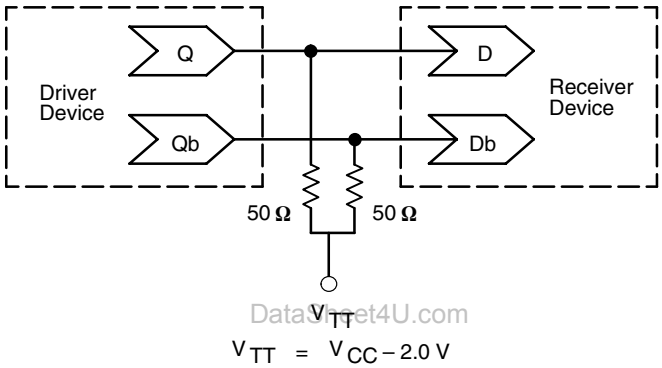


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405 – ECL Clock Distribution Techniques
AN1406 – Designing with PECL (ECL at +5.0 V)
AN1503 – ECLinPS I/O SPICE Modeling Kit
AN1504 – Metastability and the ECLinPS Family
AN1560 – Low Voltage ECLinPS SPICE Modeling Kit
AN1568 – Interfacing Between LVDS and ECL
AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650 – Using Wire–OR Ties in ECLinPS Designs
AN1672 – The ECL Translator Guide
AND8001 – Odd Number Counters Design
AND8002 – Marking and Date Codes
AND8020 – Termination of ECL Logic Devices

MC100LVEL17

3.3V ECL Quad Differential Receiver

The MC100LVEL17 is a 3.3 V ECL, quad differential receiver. The device is functionally equivalent to the E116 device with the capability of operation from either a –3.3 V or +3.3 V supply voltage.

Under open input conditions, the $\overline{D}$ input will be biased at $V_{CC}/2$ and the D input will be pulled down to V_{EE}. This operation will force the Q output LOW and ensure stability.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- 325 ps Propagation Delay
- High Bandwidth Output Transitions
- ESD Protection: >2 KV HBM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 3.0 V to 3.8 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE} = –3.0 V to –3.8 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 141 devices

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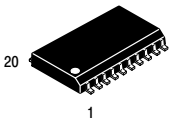
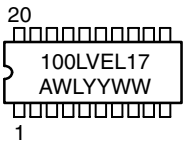


SO–20
DW SUFFIX
CASE 751D

MARKING DIAGRAM*



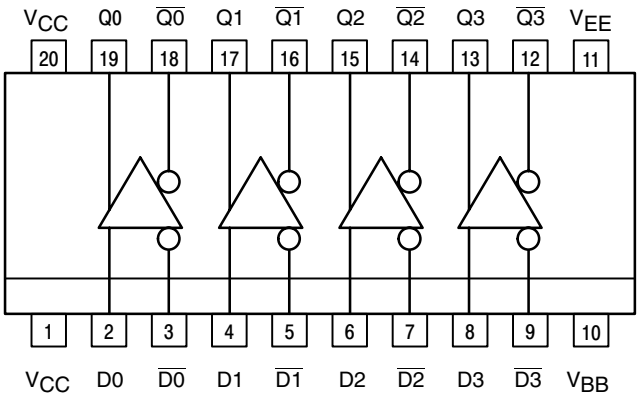
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL17DW	SOIC–20	38 Units/Rail
MC100LVEL17DWR2	SOIC–20	1000 Units/Reel

Logic Diagram and Pinout: 20-Lead SOIC (Top View)



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

PIN	FUNCTION
Dn, $\overline{Dn}$	ECL Data Inputs
Qn, $\overline{Qn}$	ECL Data Outputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		26	31		26	31		27	33	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1490		1825	1490		1825	1490		1825	mV
V_{BB}	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)										
	Vpp < 500 mV	1.3		2.9	1.2		2.9	1.2		2.9	V
	Vpp ≧ 500 mV	1.5		2.9	1.4		2.9	1.4		2.9	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current Dn	0.5			0.5			0.5			μA
	$\overline{Dn}$	–300			–300			–300			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

LVNECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		26	31		26	31		27	33	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)										
	Vpp < 500 mV	–2.0		–0.4	–2.1		–0.4	–2.1		–0.4	V
	Vpp ≧ 500 mV	–1.8		–0.4	–1.9		–0.4	–1.9		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current Dn	0.5			0.5			0.5			μA
	$\overline{Dn}$	–300			–300			–300			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay Diff D to Q S.E.	330 280		530 580	350 300		550 600	360 310		560 610	ps
t_{SKEW}	Skew Output–to–Output (Note 2.) Part–to–Part (Diff) (Note 2.) Duty Cycle (Diff) (Note 3.)			75 200 25			75 200 25			75 200 25	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 4.)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	280		550	280		550	280		550	ps

1. V_{EE} can vary ±0.3 V.
2. Skews are valid across specified voltage range, part–to–part skew is for a given temperature.
3. Duty cycle skew is the difference between a TPLH and TPHL propagation delay through a device.
4. V_{PP}(min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

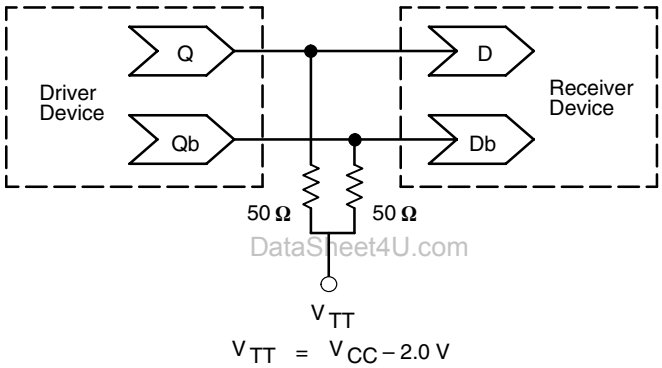


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405 – ECL Clock Distribution Techniques
AN1406 – Designing with PECL (ECL at +5.0 V)
AN1503 – ECLinPS I/O SPICE Modeling Kit
AN1504 – Metastability and the ECLinPS Family
AN1560 – Low Voltage ECLinPS SPICE Modeling Kit
AN1568 – Interfacing Between LVDS and ECL
AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650 – Using Wire–OR Ties in ECLinPS Designs
AN1672 – The ECL Translator Guide
AND8001 – Odd Number Counters Design
AND8002 – Marking and Date Codes
AND8020 – Termination of ECL Logic Devices

MC100LVELT22

3.3V Dual LVTTL/LVCMOS to Differential LVPECL Translator

The MC100LVELT22 is a dual LVTTL/LVCMOS to differential LVPECL translator. Because LVPECL (Low Voltage Positive ECL) levels are used, only +3.3 V and ground are required. The small outline 8-lead package and the low skew, dual gate design of the LVELT22 makes it ideal for applications which require the translation of a clock and a data signal.

- 350 ps Typical Propagation Delay
- <100 ps Output–to–Output Skew
- ESD Protection: >4 KV HBM, >200 V MM
- Flow Through Pinouts
- The 100 Series Contains Temperature Compensation
- LVPECL Operating Range: V_{CC}= 3.0 V to 3.8 V with GND= 0 V
- When Unused TTL Input is left Open, Q Output will Default High
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 164 devices

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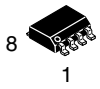
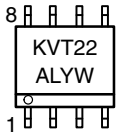
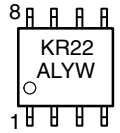
MARKING DIAGRAMS*



SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R

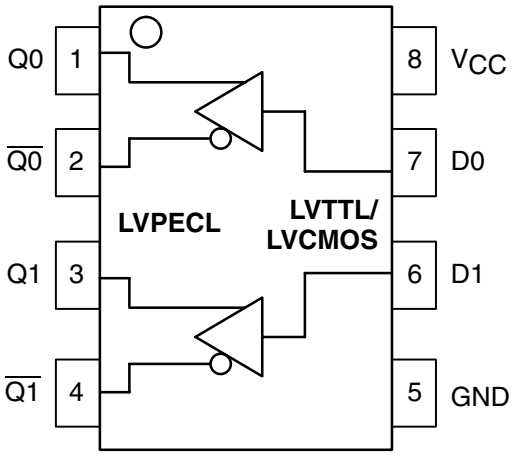


A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVELT22D	SO–8	98 Units / Rail
MC100LVELT22DR2	SO–8	2500 / Reel
MC100LVELT22DT	TSSOP–8	98 Units / Rail
MC100LVELT22DTR2	TSSOP–8	2500 / Reel



PIN DESCRIPTION

PIN	FUNCTION
Qn, $\overline{Qn}$	LVPECL Differential Outputs
D0, D1	LVTTL/LVCMOS Inputs
V_{CC}	Positive Supply
GND	Ground

Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Positive Power Supply	GND = 0 V		7	V
V_I	Input Voltage	GND = 0 V	$V_I \leq V_{CC}$	7	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44 ± 5%	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC}= 3.3 V; GND= 0.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{CC}	Power Supply Current			28			28			29	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2275		2420	2275		2420	2275		2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1490		1680	1490		1680	1490		1680	mV

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Output parameters vary 1:1 with V_{CC}. V_{CC} can vary ±0.15V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

LVTTL/LVCMOS INPUT DC CHARACTERISTICS V_{CC} = 3.3V; T_A = –40°C to 85°C (Note 1.)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current			20	μA	V_{IN} = 2.7V
I_{IHH}	Input HIGH Current			100	μA	V_{IN} = V_{CC}
I_{IL}	Input LOW Current			–0.2	mA	V_{IN} = 0.5V
V_{IK}				–1.2	V	I_{IN} = –18mA
V_{IH}	Input HIGH Voltage	2.0			V	
V_{IL}	Input LOW Voltage			0.8	V	

1. V_{CC} can vary ±0.15V.

AC CHARACTERISTICS V_{CC}= 3.3 V; GND= 0.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH}	Propagation Delay (Note 2.)	200	350	600	200	350	600	200	350	600	ps
t_{skew}	Skew Output–to–Output Part–to–Part		30	100 400		30	100 400		30	100 400	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r/t_f	Output Rise/Fall Time (20–80%)	200		550	200		500	200		500	ps

1. V_{CC} can vary ±0.15 V.
2. Specifications for standard TTL input signal.

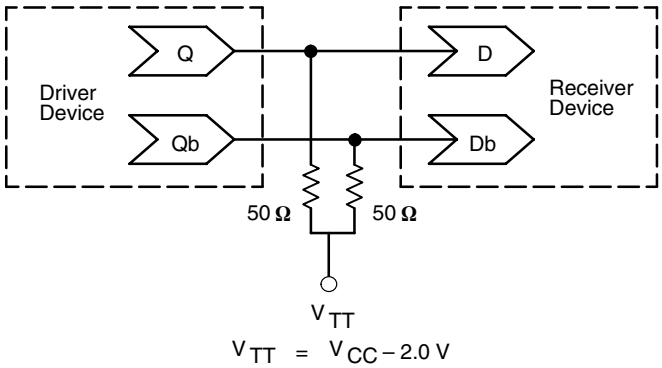


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC100LVELT23

3.3V Dual Differential LVPECL to LVTTL Translator

The MC100LVELT23 is a dual differential LVPECL to LVTTL translator. Because LVPECL (Positive ECL) levels are used only +3.3 V and ground are required. The small outline 8-lead package and the dual gate design of the LVELT23 makes it ideal for applications which require the translation of a clock and a data signal.

The LVELT23 is available in only the ECL 100K standard. Since there are no LVPECL outputs or an external V_{BB} reference, the LVELT23 does not require both ECL standard versions. The LVPECL inputs are differential. Therefore, the MC100LVELT23 can accept any standard differential LVPECL input referenced from a V_{CC} of +3.3 V.

- 2.0 ns Typical Propagation Delay
- Maximum Frequency > 180 MHz
- Differential LVPECL Inputs
- PECL Mode Operating Range: V_{CC} = 3.0 V to 3.8 V with GND= 0 V
- 24 mA LVTTL Outputs
- Flow Through Pinouts
- Internal Pulldown Resistors
- Q Output will default LOW with inputs open or at GND
- ESD Protection: >1.2 KV HBM, >150 V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 91 devices

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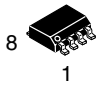
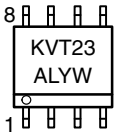
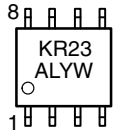
MARKING DIAGRAMS*



SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVELT23D	SO–8	98 Units / Rail
MC100LVELT23DR2	SO–8	2500 / Reel
MC100LVELT23DT	TSSOP–8	98 Units / Rail
MC100LVELT23DTR2	TSSOP–8	2500 / Reel

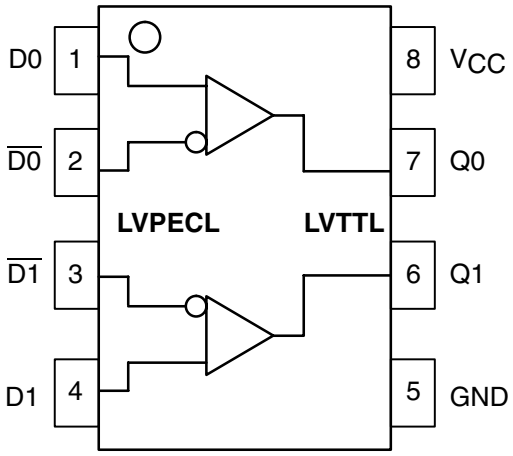


Figure 1. 8–Lead Pinout (Top View) **and Logic Diagram**

PIN DESCRIPTION

PIN	FUNCTION
Q0, Q1	LVTTL Outputs
D0, D1, $\overline{D0}$, $\overline{D1}$	Differential LVPECL Inputs
V_{CC}	Positive Supply
GND	Ground

MAXIMUM RATINGS*

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Power Supply	GND = 0 V		3.8	V
V_I	Input Voltage	GND = 0 V, V_I not more positive than V_{CC}		3.8	V
I_{out}	Output Current	Continuous Surge		50 100	mA
T_A	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44 ± 5%	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Solder Temperature	<2 to 3 Seconds: 245°C desired		265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

LVPECL DC CHARACTERISTICS V_{CC} = 3.3 V; GND = 0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{CCH}	Power Supply Current (Outputs set to HIGH)	10	18	25	10	18	25	10	18	25	mA
I_{CCL}	Power Supply Current (Outputs set to LOW)	15	26	33	15	26	33	15	26	33	mA
V_{IH}	Input HIGH Voltage	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage	1490		1825	1490		1825	1490		1825	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 2.)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	 –150		0.5	 –150		0.5	 –150		0.5	μA

NOTE: Circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

1. All values vary 1:1 with V_{CC}. V_{CC} can vary ±0.3 V.
2. V_{IHCMR} min varies 1:1 with GND, max varies 1:1 with V_{CC}.

TTL DC CHARACTERISTICS V_{CC} = 3.3 V; GND = 0V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage (I_{OH} = –3.0 mA) (Note 2.)	2.4			2.4			2.4			V
V_{OL}	Output LOW Voltage (I_{OL} = 24 mA) (Note 2.)			0.5			0.5			0.5	V
I_{OS}	Output Short Circuit Current	–180		–50	–180		–50	–180		–50	mA

NOTE: Circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. All values vary 1:1 with V_{CC}. V_{CC} can vary ±0.3 V.
2. All loading with 500 ohms to GND, CL = 20 pF.

AC CHARACTERISTICS V_{CC} = 3.3 V; GND = 0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency (Note 2.)	180			180			180			MHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	1.0	1.5	2.5	1.0	1.7	2.5	1.0	1.7	2.5	ns
t_{SK++} t_{SK--} t_{SKPP}	Output–to–Output Skew++ Output–to–Output Skew– – Part–to–Part Skew (Note 3.)			60 25 500			60 25 500			60 25 500	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Voltage Swing (Differential) (Note 4.)	200	800	1000	200	800	1000	200	800	1000	mV
t_r t_f	Output Rise/Fall Times (0.8 V – 2.0 V) Q, $\overline{Q}$	330	600	900	330	600	900	330	650	900	ps

1. V_{CC} can vary ±0.3 V.
2. F_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.
3. Skews are measured between outputs under identical conditions.
4. 200 mV input guarantees full logic swing at the output.

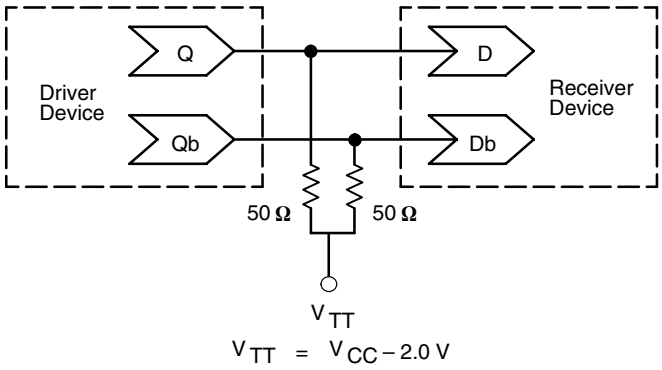


Figure 2. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC100LVEL29

3.3V ECL Dual Differential Data and Clock D Flip-Flop With Set and Reset

The MC100LVEL29 is a dual master–slave flip flop. The device features fully differential Data and Clock inputs as well as outputs. The MC100LVEL29 is pin and functionally equivalent to the MC100EL29. Data enters the master latch when the clock is LOW and transfers to the slave upon a positive transition on the clock input.

The differential inputs have special circuitry which ensures device stability under open input conditions. When both differential inputs are left open the D input will pull down to V_{EE} and the $\overline{D}$ input will bias around $V_{CC}/2$. The outputs will go to a defined state, however the state will be random based on how the flip flop powers up.

Both flip flops feature asynchronous, overriding Set and Reset inputs. Note that the Set and Reset inputs cannot both be HIGH simultaneously.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- 1100 MHz Flip–Flop Toggle Frequency
- ESD Protection: >2 KV HBM
- 580 ps Typical Propagation Delays
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 3.0 V to 3.8 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –3.0 V to –3.8 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 313 devices

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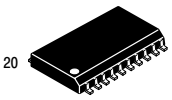
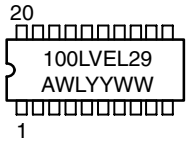


SOIC–20
DW SUFFIX
CASE 751D

MARKING DIAGRAM*



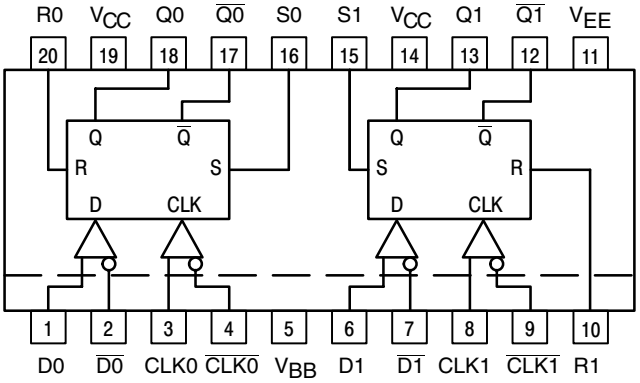
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL29DW	SOIC–20	38 Units/Rail
MC100LVEL29DWR2	SOIC–20	1000 Units/Reel

Logic Diagram and Pinout: 20-Lead SOIC (Top View)



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

PIN	FUNCTION
D0, $\overline{D0}$; D1, $\overline{D1}$	ECL Differential Data Inputs
R0, R1	ECL Reset Inputs
CLK0, $\overline{CLK0}$	ECL Differential Clock Inputs
CLK1, $\overline{CLK1}$	ECL Differential Clock Inputs
S0, S1	ECL Set Inputs
Q0, $\overline{Q0}$; Q1, $\overline{Q1}$	ECL Differential Data Outputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

TRUTH TABLE

R	S	D	CLK	Q	$\overline{Q}$
L	L	L	Z	L	H
L	L	H	Z	H	L
H	L	X	X	L	H
L	H	X	X	H	L
H	H	X	X	Undef	Undef

Z = LOW to HIGH Transition
X = Don't Care

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		35	50		35	50		35	50	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1490		1825	1490		1825	1490		1825	mV
V_{BB}	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)										
	Vpp < 500 mV	1.3		2.9	1.2		2.9	1.2		2.9	V
	Vpp ≧ 500 mV	1.5		2.9	1.4		2.9	1.4		2.9	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current Dn	0.5			0.5			0.5			μA
	$\overline{Dn}$	–300			–300			–300			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

LVNECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		35	50		35	50		35	50	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)										
	Vpp < 500 mV	–2.0		–0.4	–2.1		–0.4	–2.1		–0.4	V
	Vpp ≧ 500 mV	–1.8		–0.4	–1.9		–0.4	–1.9		–0.4	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current Dn	0.5			0.5			0.5			μA
	$\overline{Dn}$	–300			–300			–300			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency	1.1			1.1			1.1			GHz
t_{PLH} t_{PHL}	Propagation Delay CLK to Output S, R	480 480		680 700	500 500	580	700 720	520 520		720 740	ps
t_S t_H	Setup Time Hold Time	0 100			0 100			0 100			ps
t_{RR}	Set/Reset Recovery	100			100			100			ps
t_{PW}	Minimum Pulse Width CLK, Set, Reset	400			400			400			ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 2.)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	280		550	280		550	280		550	ps

1. V_{EE} can vary ±0.3 V.
2. V_{PP}(min) is the minimum input swing for which AC parameters guaranteed.

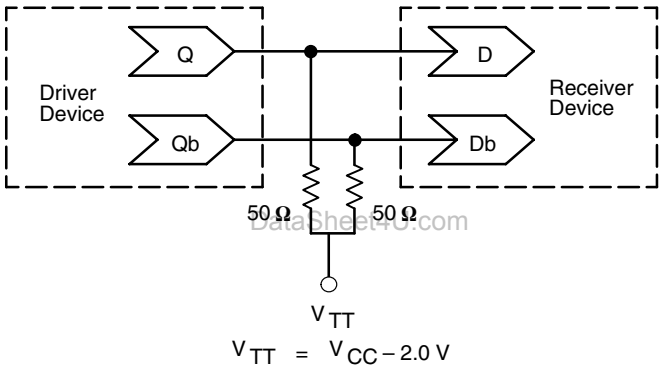


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405 – ECL Clock Distribution Techniques
AN1406 – Designing with PECL (ECL at +5.0 V)
AN1503 – ECLinPS I/O SPICE Modeling Kit
AN1504 – Metastability and the ECLinPS Family
AN1560 – Low Voltage ECLinPS SPICE Modeling Kit
AN1568 – Interfacing Between LVDS and ECL
AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650 – Using Wire–OR Ties in ECLinPS Designs
AN1672 – The ECL Translator Guide
AND8001 – Odd Number Counters Design
AND8002 – Marking and Date Codes
AND8020 – Termination of ECL Logic Devices

MC100LVEL30

3.3V ECL Triple D Flip-Flop with Set and Reset

The MC100LVEL30 is a triple master–slave D flip flop with differential outputs. Data enters the master latch when the clock input is LOW and transfers to the slave upon a positive transition on the clock input.

In addition to a common Set input individual Reset inputs are provided for each flip flop. Both the Set and Reset inputs function asynchronous and overriding with respect to the clock inputs.

- 1200 MHz Minimum Toggle Frequency
- 450 ps Typical Propagation Delays
- ESD Protection: >2 KV HBM
- The 100 Series Contains Temperature Compensation.
- PECL Mode Operating Range: V_{CC}= 3.0 V to 3.8 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –3.0 V to –3.8 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 347 devices

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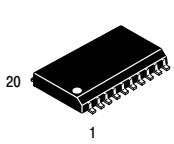
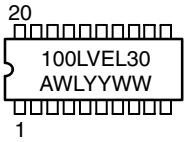


SO–20
DW SUFFIX
CASE 751D

MARKING DIAGRAM*



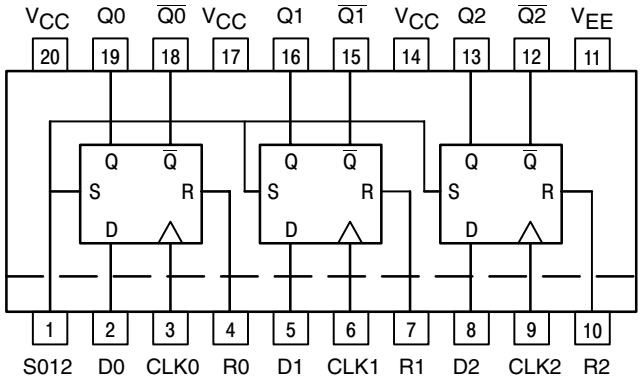
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL30DW	SO–20	38 Units/Rail
MC100LVEL30DWR2	SO–20	1000 Units/Reel

Logic Diagram and Pinout: 20-Lead SOIC (Top View)



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

PIN	FUNCTION
D0–D2	ECL Data Inputs
R0–R2	ECL Reset Inputs
CLK0–CLK2	ECL Clock Inputs
S012	ECL Common Set Input
Q0–Q2; $\overline{Q0–Q2}$	ECL Differential Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

TRUTH TABLE

R	S	D	CLK	Q	$\overline{Q}$
L	L	L	Z	L	H
L	L	H	Z	H	L
H	L	X	X	L	H
L	H	X	X	H	L
H	H	X	X	Undef	Undef

Z = LOW to HIGH Transition
X = Don't Care

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		55	62		55	62		55	64	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage	1490		1825	1490		1825	1490		1825	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

LVNECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		55	62		55	62		55	64	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage	–1810		–1475	–1810		–1475	–1810		–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Toggle Frequency	1.2			1.2			1.2			GHz
t_{PLH} t_{PHL}	Propagation Delay CLK to Output S, R	460 470		690 710	480 490		710 730	500 515		730 755	ps
t_S t_H	Setup Time Hold Time	150 200	0 100		150 200	0 100		150 200	0 100		ps
t_{RR}	Set/Reset Recovery	400	200		400	200		400	200		ps
t_{PW}	Minimum Pulse Width CLK Set, Reset	400 650			400 650			400 650			ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	280		550	280	450	550	280		550	ps

1. V_{EE} can vary ±0.3 V.

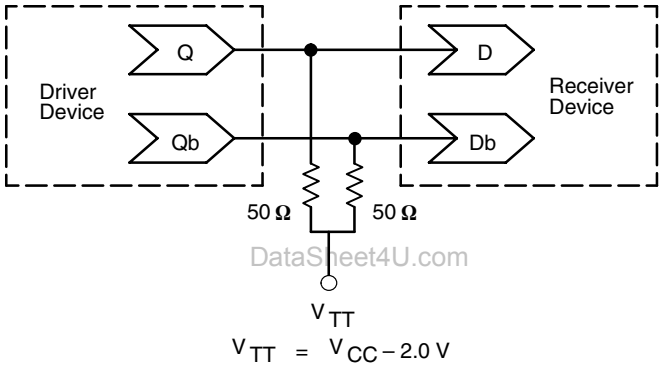


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels

AN1405 – ECL Clock Distribution Techniques

AN1406 – Designing with PECL (ECL at +5.0 V)

AN1503 – ECLinPS I/O SPICE Modeling Kit

AN1504 – Metastability and the ECLinPS Family

AN1560 – Low Voltage ECLinPS SPICE Modeling Kit

AN1568 – Interfacing Between LVDS and ECL

AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit

AN1650 – Using Wire–OR Ties in ECLinPS Designs

AN1672 – The ECL Translator Guide

AND8001 – Odd Number Counters Design

AND8002 – Marking and Date Codes

AND8020 – Termination of ECL Logic Devices

MC100LVEL31

3.3V ECL D Flip-Flop with Set and Reset

The MC100LVEL31 is a D flip-flop with set and reset. The device is functionally equivalent to the EL31 device but operates from a 3.3 V supply. With propagation delays and output transition times essentially equivalent to the EL31, the LVEL31 is ideally suited for those applications which require the ultimate in AC performance at low power supply voltages.

Both set and reset inputs are asynchronous, level triggered signals. Data enters the master portion of the flip-flop when clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock.

- 475 ps Typical Propagation Delay
- 2.9 GHz Toggle Frequency
- ESD Protection: >4 KV HBM, >200 V MM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 3.0 V to 3.8 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE} = –3.0 V to –3.8 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 121 devices

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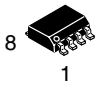
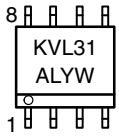
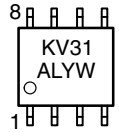
MARKING DIAGRAMS*



SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



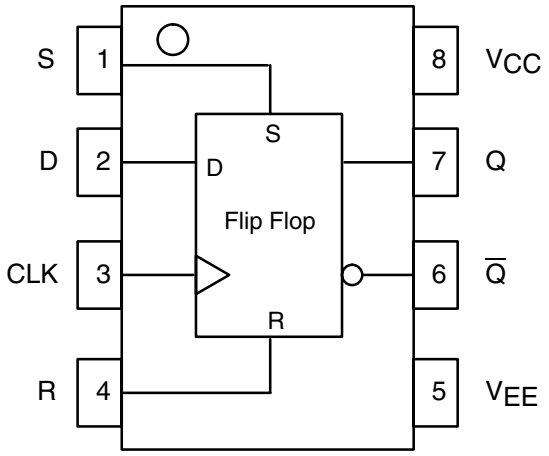
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL31D	SO–8	98 Units / Rail
MC100LVEL31DR2	SO–8	2500 / Reel
MC100LVEL31DT	TSSOP–8	98 Units / Rail
MC100LVEL31DTR2	TSSOP–8	2500 / Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
CLK	ECL Clock Input
Q, $\overline{Q}$	ECL Differential Data Outputs
D	ECL Data Input
R	ECL Reset Input
S	ECL Set Input
V_{CC}	Positive Supply
V_{EE}	Negative Supply

TRUTH TABLE

D	S	R	CLK	Q	$\overline{Q}$
L	L	L	Z	L	H
H	L	L	Z	H	L
X	H	L	X	H	L
X	L	H	X	L	H
X	H	H	X	Undef	Undef

Z = LOW to HIGH Transition
X = Don't Care

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44 ± 5%	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V (Note 1)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		30	35		30	35		32	38	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage	1490		1825	1490		1825	1490		1825	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

LVNECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		30	35		30	35		32	38	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage	–1810		–1475	–1810		–1475	–1810		–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency	2.7			2.9			2.9			GHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK S, R	365 385	465 475	580 620	375 395	475 485	590 630	415 435	530 525	630 670	ps
t_S t_H	Setup Time Hold Time	150 250	0 100		150 250	0 100		150 250	0 100		ps
t_{RR}	Set/Reset Recovery	400	200		400	200		400	200		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_{PW}	Minimum Pulse Width CLK Set, Reset	340 600			340 600			340 600			ps
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	120	220	320	120	220	320	120	220	320	ps

1. V_{EE} can vary ±0.3 V.

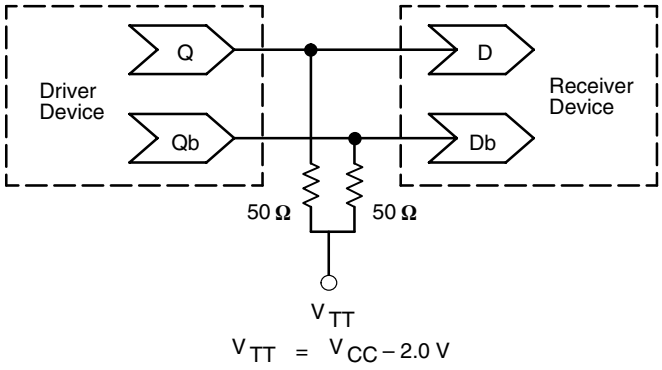


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC100LVEL32

3.3V ECL ÷2 Divider

The MC100LVEL32 is an integrated ÷2 divider. The LVEL32 is functionally identical to the EL32, but operates from a 3.3 V supply.

The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flop will attain a random state; the reset allows for the synchronization of multiple LVEL32's in a system.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- 510 ps Propagation Delay
- 2.6 GHz Typical Maximum Frequency
- ESD Protection: >4 KV HBM, >200 V MM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 3.0 V to 3.8 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE} = –3.0 V to –3.8 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8",
  Oxygen Index 28 to 34
- Transistor Count = 111 devices

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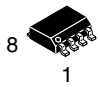
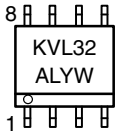
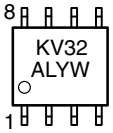
MARKING DIAGRAMS*



SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



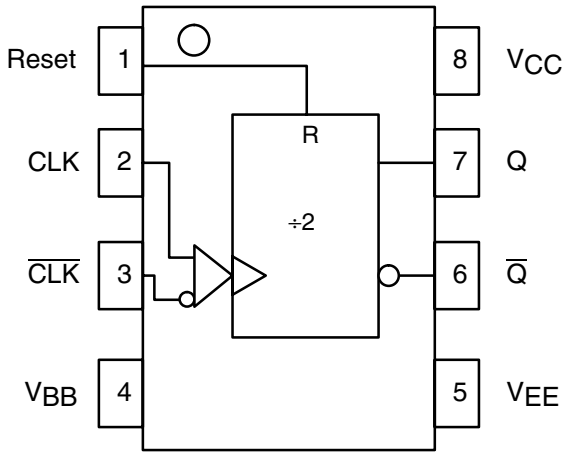
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL32D	SO–8	98 Units / Rail
MC100LVEL32DR2	SO–8	2500 / Reel
MC100LVEL32DT	TSSOP–8	98 Units / Rail
MC100LVEL32DTR2	TSSOP–8	2500 / Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
CLK, $\overline{CLK}$	ECL Differential Clock Inputs
Q, $\overline{Q}$	ECL Differential Data ÷2 Outputs
Reset	ECL Asynch Reset
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44 ± 5%	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V (Note 1)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		29	35		29	35		31	36	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1490		1825	1490		1825	1490		1825	mV
V_{BB}	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.) Vpp < 500 mV Vpp ≧ 500 mV	 1.2 1.4		 3.1 3.1	 1.1 1.3		 3.1 3.1	 1.1 1.3		 3.1 3.1	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK $\overline{CLK}$	0.5 –600			0.5 –600			0.5 –600			μA μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

LVNECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		29	35		29	35		31	36	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.) Vpp < 500 mV Vpp ≧ 500 mV	 2.1 1.9		 –0.2 –0.2	 2.2 2.0		 –0.2 –0.2	 2.2 2.0		 –0.2 –0.2	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLK $\overline{CLK}$	0.5 –600			0.5 –600			0.5 –600			μA μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency	2.2	2.5		2.4	2.6		2.6	2.8		GHz
t_{PLH} t_{PHL}	Propagation Delay CLK to Q (Diff) CLK to Q (S.E.) Reset to Q	 350 300 340	 500 500 540	 530 580 540	 370 320 350	 510 510 540	 550 600 550	 410 360 380	 540 540 550	 590 640 580	 ps
t_{RR}	Reset Recovery	175	50		175	50		175	50		ps
t_{PW}	Minimum Pulse Width Reset	500	300		500	300		500	300		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 2.)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	120	225	320	120	225	320	120	225	320	ps

1. V_{EE} can vary ±0.3 V.
2. V_{PP}(min) is minimum input swing for which AC parameters are guaranteed.

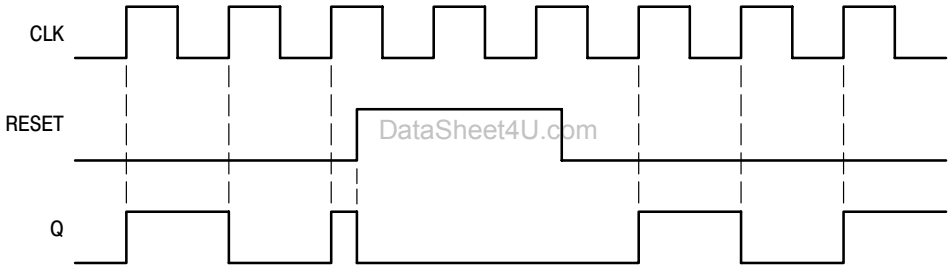


Figure 1. Timing Diagram

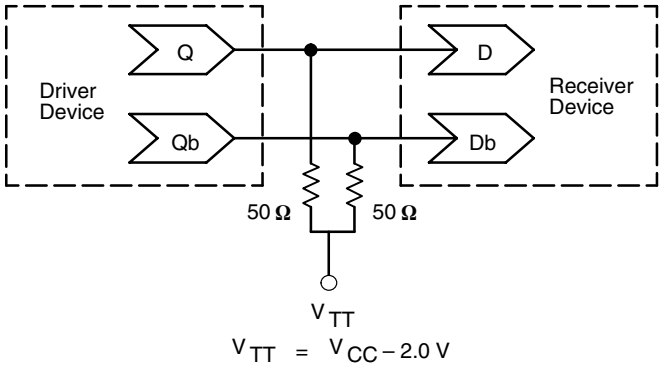


Figure 2. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC100LVEL33

3.3V ECL ÷4 Divider

The MC100LVEL33 is an integrated ÷4 divider. The LVEL is functionally equivalent to the EL33 and works from a 3.3 V supply.

The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flops will attain a random state; the reset allows for the synchronization of multiple LVEL33's in a system.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- 630 ps Typical Propagation Delay
- 4.0 GHz Typical Maximum Frequency
- ESD Protection: >4 KV HBM, >200 V MM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 3.0 V to 3.8 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –3.0 V to –3.8 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8",
  Oxygen Index 28 to 34
- Transistor Count = 130 devices

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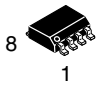
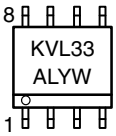
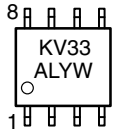
MARKING DIAGRAMS*



SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



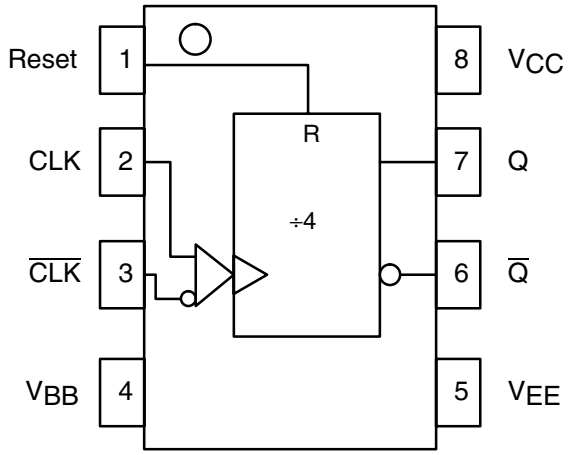
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL33D	SO–8	98 Units / Rail
MC100LVEL33DR2	SO–8	2500 / Reel
MC100LVEL33DT	TSSOP–8	98 Units / Rail
MC100LVEL33DTR2	TSSOP–8	2500 / Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
CLK, $\overline{CLK}$	ECL Differential Clock Inputs
Q, $\overline{Q}$	ECL Differential Data ÷4 Outputs
Reset	ECL Asynch Reset
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44 ± 5%	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V (Note 1)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		33	37		33	37		35	39	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1490		1825	1490		1825	1490		1825	mV
V_{BB}	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.) Vpp < 500 mV Vpp ≧ 500 mV	 1.2 1.4		 2.9 2.9	 1.1 1.3		 2.9 2.9	 1.1 1.3		 2.9 2.9	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current Other $\overline{CLK}$	0.5 –600			0.5 –600			0.5 –600			μA μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

LVNECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		33	37		33	37		35	39	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.) Vpp < 500 mV Vpp ≧ 500 mV	 –2.1 –1.9		 –0.4 –0.4	 –2.2 –2.0		 –0.4 –0.4	 –2.2 –2.0		 –0.4 –0.4	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current Other $\overline{CLK}$	0.5 –600			0.5 –600			0.5 –600			μA μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency	3.4			3.8	4.0		3.8			GHz
t_{PLH} t_{PHL}	Propagation Delay CLK to Q (Diff) CLK to Q (SE) Reset to Q	 510 460 500		 690 740 700	 540 490 520	 630	 720 770 720	 600 550 580		 780 830 780	 ps
t_{RR}	Reset Recovery	300			300			300			ps
t_{skew}	Duty Cycle Skew (Note 2.)			20			20			20	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 3.)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	120		320	120		320	120		320	ps

1. V_{EE} can vary ±0.3 V.
2. Duty cycle skew is the difference between T_{PLH} and T_{PHL}.
3. V_{PP} (min) is minimum input swing for which AC parameters are guaranteed.

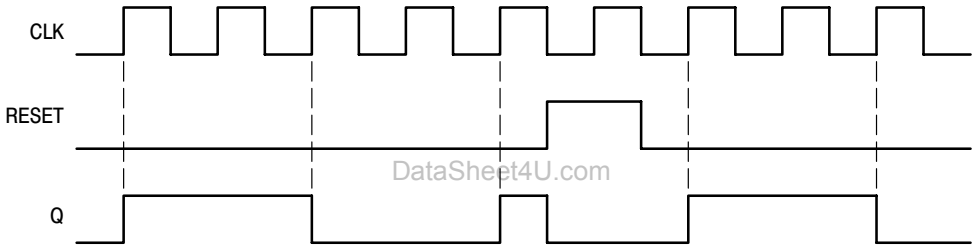


Figure 1. Timing Diagram

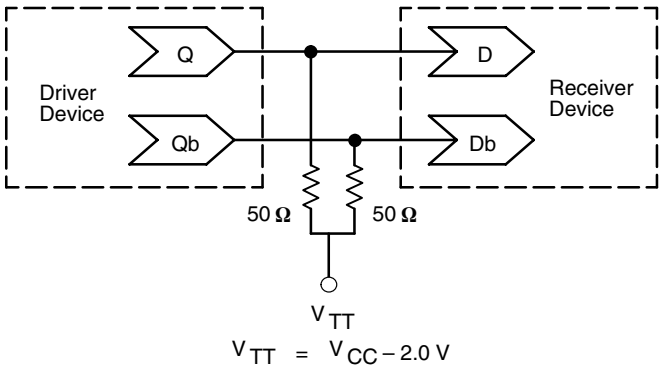


Figure 2. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC100LVEL37

3.3V ECL 1:4 ÷1/÷2 Clock Fanout Buffer

The MC100LVEL37 is a fully differential 1:4 fanout buffer. The device offers two outputs at ÷1 of the input frequency, and two outputs at ÷2 of the input frequency. The Low Output–Output Skew of the device makes it ideal for distributing 1x and 1/2x frequency synchronous signals.

The differential inputs have special circuitry which ensures device stability under open input conditions. When both differential inputs are left open the CLKn input will pull down to V_{EE}, The $\overline{CLKn}$ input will bias around $V_{CC}/2$ and the Qn output will go LOW.

- 700 ps Typical Propagation Delays
- 50 ps Maximum Output–Output Skews
- ESD Protection: >2 KV HBM, >200 V MM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 3.0 V to 3.8 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –3.0 V to –3.8 V
- Internal Input Pulldown Resistors
- Qn Output will Default LOW with Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 256 devices

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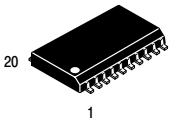
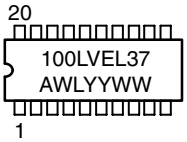
MARKING DIAGRAM*



SO–20
DW SUFFIX
CASE 751D



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL37DW	SO–20	38 Units/Rail
MC100LVEL37DWR2	SO–20	1000 Units/Reel

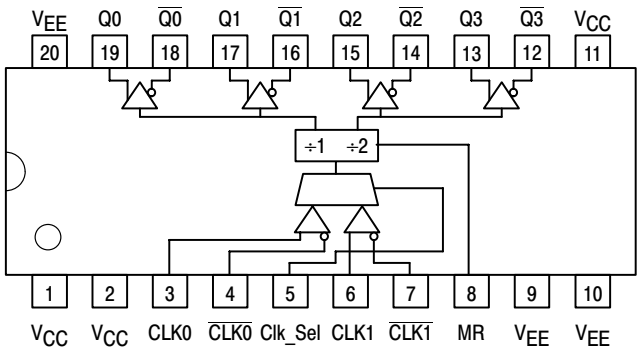


Figure 3. 20–Lead Pinout (Top View)

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

TRUTH TABLE

Clk_Sel	MR	Q0, 1	Q2, 3
L	L	CLK0/÷1	CLK0/÷2
H	L	CLK1/÷1	CLK1/÷2
X	H	L	L

X = Don't Care

PIN DESCRIPTION

PIN	FUNCTION
Q0, $\overline{Q0}$; Q1, $\overline{Q1}$	ECL Differential Clock ÷1 Outputs
Q2, $\overline{Q2}$; Q3, $\overline{Q3}$	ECL Differential Clock ÷2 Outputs
CLKn, $\overline{CLKn}$	ECL Differential Clock Inputs
Clk_Sel	ECL Input Clock Selection
MR	ECL Asynchronous Master Reset
V_{CC}	Positive Supply
V_{EE}	Negative Supply

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V (Note 1)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		38	50		38	55		38	55	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1490		1825	1490		1825	1490		1825	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.) Vpp < 500 mV Vpp ≧ 500 mV	 1.3 1.5		 2.9 2.9	 1.2 1.4		 2.9 2.9	 1.2 1.4		 2.9 2.9	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLKn $\overline{CLKn}$	0.5 –300			0.5 –300			0.5 –300			μA μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

LVNECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		38	50		38	55		38	55	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.) Vpp < 500 mV Vpp ≧ 500 mV	 –2.0 –1.8		 –0.4 –0.4	 –2.1 –1.9		 –0.4 –0.4	 –2.1 –1.9		 –0.4 –0.4	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current CLKn $\overline{CLKn}$	0.5 –300			0.5 –300			0.5 –300			μA μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay										ps
	CLK to Q/$\overline{Q}$ (Diff)	640		940	680	700	920	720		980	
	CLK to Q/$\overline{Q}$	620		920	680	700	940	720		970	
	MR to Q	640		920	680	700	920	720		980	
t_{SKEW}	Within-Device Skew (Note 2.) Duty Cycle Skew (Diff) (Note 3.)			50 50			50 50			50 50	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 4.)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	280		550	280		550	280		550	ps

1. V_{EE} can vary ±0.3 V.
2. Within-device skew defined as identical transitions on similar paths through a device.
3. Duty cycle skew is the difference between a TPLH and TPHL propagation delay through a device.
4. V_{PP}(min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

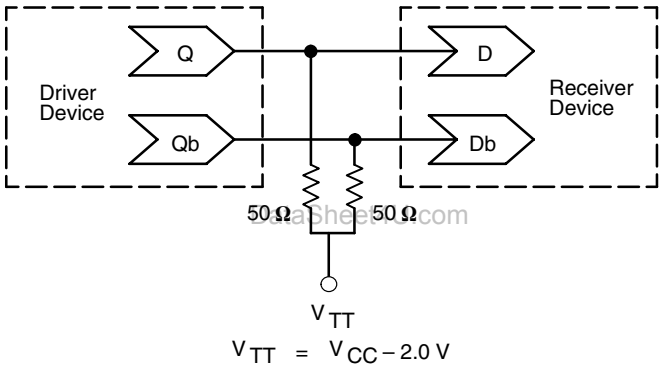


Figure 1. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405 – ECL Clock Distribution Techniques
AN1406 – Designing with PECL (ECL at +5.0 V)
AN1503 – ECLinPS I/O SPICE Modeling Kit
AN1504 – Metastability and the ECLinPS Family
AN1560 – Low Voltage ECLinPS SPICE Modeling Kit
AN1568 – Interfacing Between LVDS and ECL
AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650 – Using Wire–OR Ties in ECLinPS Designs
AN1672 – The ECL Translator Guide
AND8001 – Odd Number Counters Design
AND8002 – Marking and Date Codes
AND8020 – Termination of ECL Logic Devices

MC100LVEL38

3.3V ECL ÷2, ÷4/6 Clock Generation Chip

The MC100LVEL38 is a low skew ÷2, ÷4/6 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended input signal.

The common enable ($\overline{EN}$) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

The Phase_Out output will go HIGH for one clock cycle whenever the ÷2 and the ÷4/6 outputs are both transitioning from a LOW to a HIGH. This output allows for clock synchronization within the system.

Upon startup, the internal flip-flops will attain a random state; therefore, for systems which utilize multiple LVEL38s, the master reset (MR) input must be asserted to ensure synchronization. For systems which only use one LVEL38, the MR pin need not be exercised as the internal divider design ensures synchronization between the ÷2 and the ÷4/6 outputs of a single device.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- 50 ps Maximum Output-to-Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- ESD Protection: >2 KV HBM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 3.0 V to 3.8 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –3.0 V to –3.8 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 388 devices

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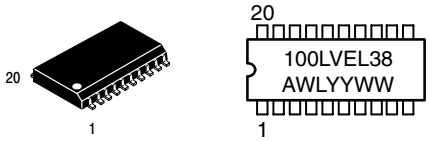
MARKING DIAGRAM



SO–20
DW SUFFIX
CASE 751D

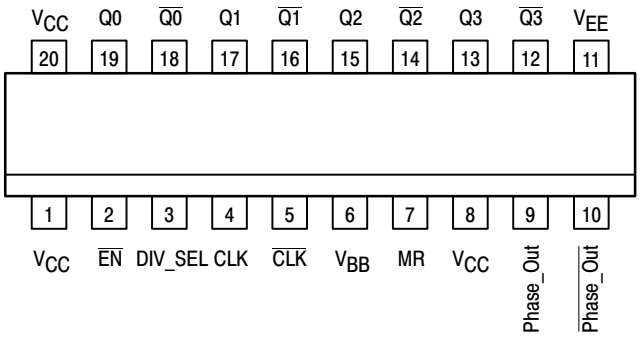
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL38DW	SOIC–20	38 Units/Rail
MC100LVEL38DWR2	SOIC–20	1000 Units/Reel

MC100LVEL38

Pinout: 20-Lead SOIC (Top View)



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

FUNCTION TABLE

CLK	$\overline{EN}$	MR	FUNCTION
Z	L	L	Divide
ZZ	H	L	Hold Q_{0-3}
X	X	H	Reset Q_{0-3}

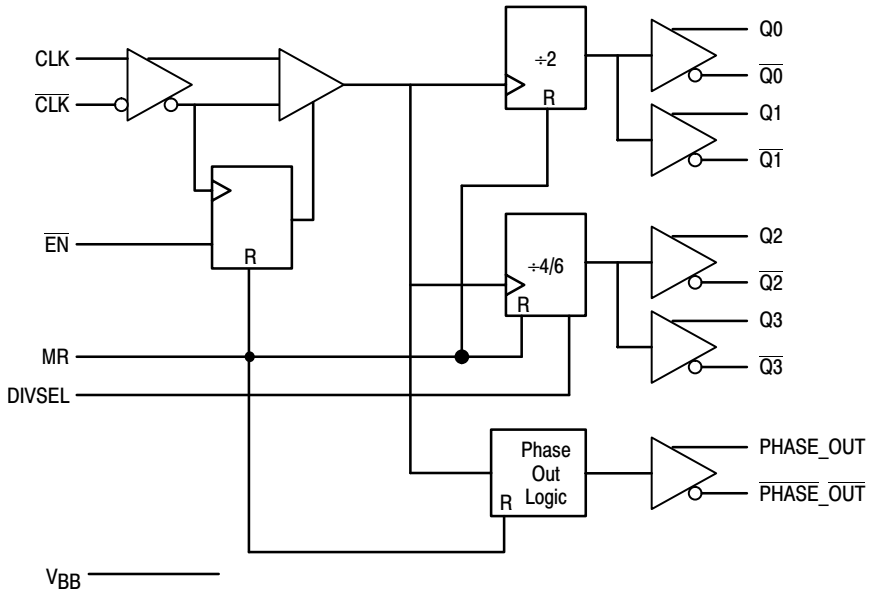
Z = Low-to-High Transition
ZZ = High-to-Low Transition
X = Don't Care

DIVSEL	Q_2, Q_3 OUTPUTS
L	Divide by 4
H	Divide by 6

PIN DESCRIPTION

PIN	FUNCTION
CLK, $\overline{CLK}$	ECL Diff Clock Inputs
Q_0, Q_1; $\overline{Q_0}$, $\overline{Q_1}$	ECL Diff ÷2 Outputs
Q_2, Q_3; $\overline{Q_2}$, $\overline{Q_3}$	ECL Diff ÷4/6 Outputs
$\overline{EN}$	ECL Sync Enable Input
MR	ECL Master Reset Input
DIVSEL	ECL Frequency Select Input
Phase_Out, $\overline{Phase\_Out}$	ECL Phase Sync Diff. Signal Output
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

LOGIC DIAGRAM



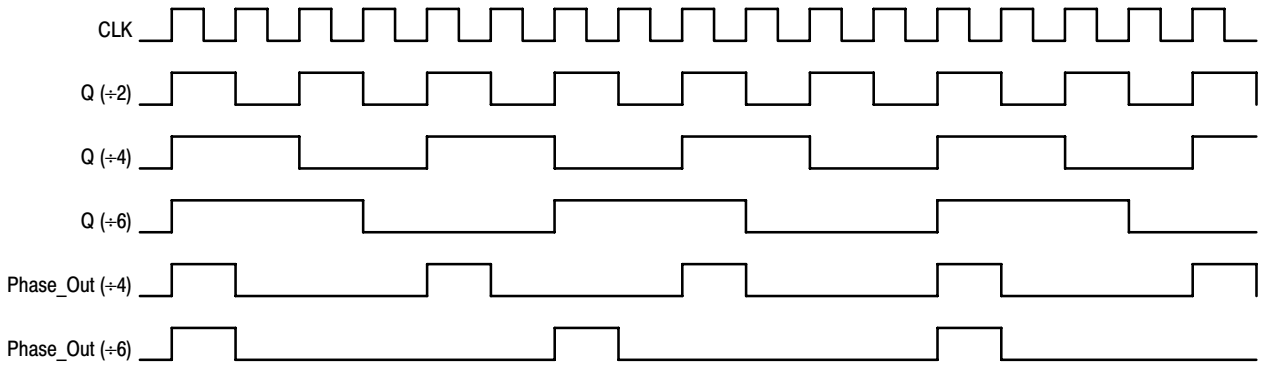


Figure 1. Timing Diagrams

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V (Note 1)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		50	60		50	60		54	65	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1490		1825	1490		1825	1490		1825	mV
V_{BB}	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	1.65		2.75	1.65		2.75	1.65		2.75	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between $V_{PP\ Min}$ and 1.0 V.

LVNECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		50	60		50	60		54	65	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	–1.65		–0.55	–1.65		–0.55	–1.65		–0.55	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between $V_{PP\ Min}$ and 1.0 V.

AC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay CLK to Q (Diff) to Output CLK to Q (S.E.) CLK to Phase_Out (Diff) CLK to Phase_Out (S.E.) MR to.Q	760 710 800 750 510		960 1010 1000 1050 810	800 750 840 790 540		1000 1050 1040 1090 840	850 800 890 840 570		1050 1100 1090 1140 870	ps
t_{SKEW}	Within-Device Skew (Note 2.) $Q_0 - Q_3$ All			50 75			50 75			50 75	ps
	Part-to-Part $Q_0 - Q_3$ (Diff) All			200 240			200 240			200 240	
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_S	Setup Time $\overline{EN}$ to $\overline{CLK}$ DIVSEL to CLK		150			150			150		ps
t_H	Hold Time $\overline{CLK}$ to $\overline{EN}$ CLK to Div_Sel		150 200			150 200			150 200		ps
V_{PP}	Input Swing (Note 3.) CLK	250		1000	250		1000	250		1000	mV
t_{RR}	Reset Recovery Time			100			100			100	ps
t_{PW}	Minimum Pulse Width CLK MR	800 700			800 700			800 700			ps
t_r, t_f	Output Rise/Fall Times Q (20% – 80%)	280		550	280		550	280		550	ps

1. V_{EE} can vary ±0.3 V.
2. Skew is measured between outputs under identical transitions.
3. V_{PP}(min) is minimum input swing for which AC parameters are guaranteed. The device will function reliably with differential inputs down to 100 mV.

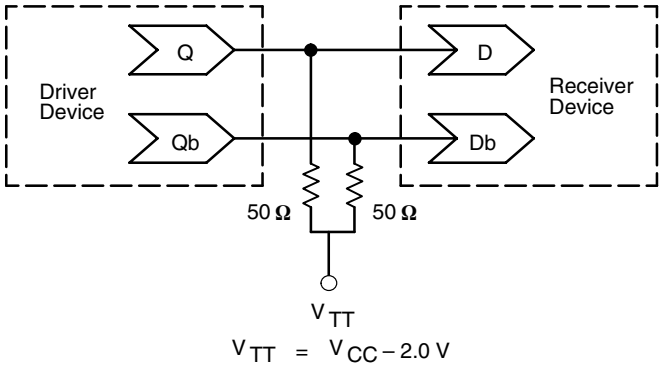


Figure 2. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC100LVEL39

3.3V ECL ÷2/4, ÷4/6 Clock Generation Chip

The MC100LVEL39 is a low skew ÷2/4, ÷4/6 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended input signal. In addition, by using the V_{BB} output, a sinusoidal source can be AC coupled into the device.

The common enable ($\overline{EN}$) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon startup, the internal flip-flops will attain a random state; therefore, for systems which utilize multiple LVEL39s, the master reset (MR) input must be asserted to ensure synchronization. For systems which only use one LVEL39, the MR pin need not be exercised as the internal divider design ensures synchronization between the ÷2/4 and the ÷4/6 outputs of a single device.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- 50 ps Maximum Output-to-Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- ESD Protection: >2 KV HBM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 3.0 V to 3.8 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –3.0 V to –3.8 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 419 devices

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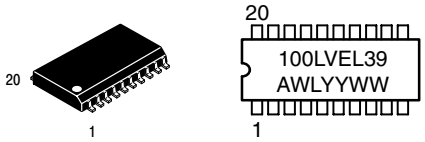
MARKING DIAGRAM*



SOIC–20
DW SUFFIX
CASE 751D

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

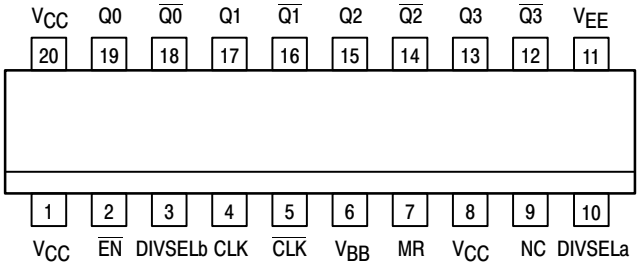
*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL39DW	SOIC–20	38 Units/Rail
MC100LVEL39DWR2	SOIC–20	1000 Units/Reel

MC100LVEL39

Pinout: 20-Lead SOIC (Top View)



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

FUNCTION TABLE

CLK	$\overline{EN}$	MR	FUNCTION
Z	L	L	Divide
ZZ	H	L	Hold $Q_{0–3}$
X	X	H	Reset $Q_{0–3}$

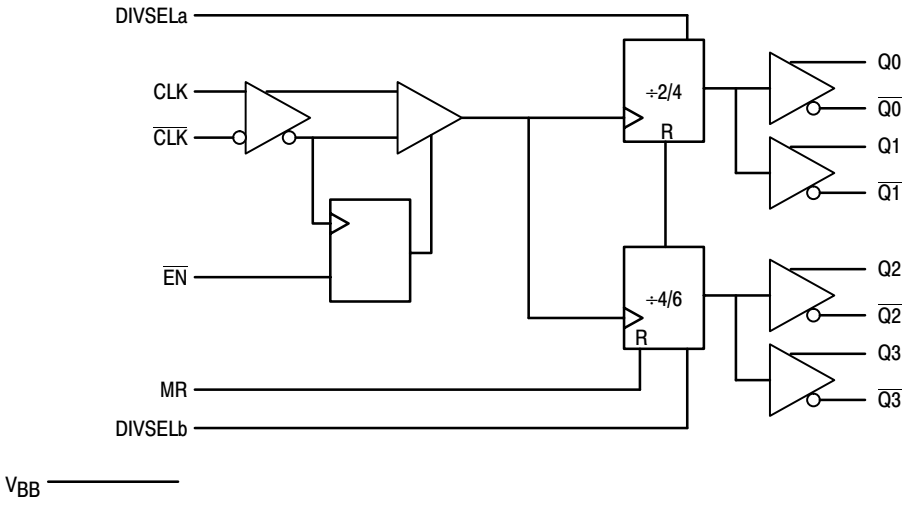
Z = Low-to-High Transition
ZZ = High-to-Low Transition
X = Don't Care

PIN DESCRIPTION

PIN	FUNCTION
CLK, $\overline{CLK}$	ECL Diff Clock Inputs
Q_0, Q_1; $\overline{Q_0}$, $\overline{Q_1}$	ECL Diff ÷2/4 Outputs
Q_2, Q_3; $\overline{Q_2}$, $\overline{Q_3}$	ECL Diff ÷4/6 Outputs
DIVSELa, DIVSELb	ECL Frequency Select Inputs
$\overline{EN}$	ECL Sync Enable
MR	ECL Master Reset
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

DIVSELa	Q_0, Q_1 OUTPUTS
L	Divide by 2
H	Divide by 4
DIVSELb	**Q_2, Q_3 OUTPUTS**
L	Divide by 4
H	Divide by 6

LOGIC DIAGRAM



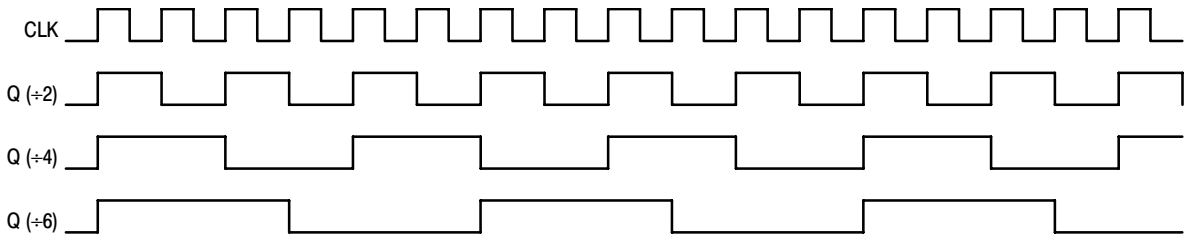


Figure 1. Timing Diagrams

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V (Note 1)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		50	59		50	59		54	61	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1490		1825	1490		1825	1490		1825	mV
V_{BB}	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.) Vpp < 500 mV Vpp ≧ 500 mV	 1.3 1.5		 2.9 2.9	 1.2 1.4		 2.9 2.9	 1.2 1.4		 2.9 2.9	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

LVNECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		50	59		50	59		54	61	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.) Vpp < 500 mV Vpp ≧ 500 mV	 –2.0 –1.8		 –0.4 –0.4	 –2.1 –1.9		 –0.4 –0.4	 –2.1 –1.9		 –0.4 –0.4	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency	1000			1000			1000			MHz
t_{PLH} t_{PHL}	Propagation Delay CLK to Q (Diff) to Output CLK to Q (S.E.) MR to Q	760 710 600		960 1010 900	800 750 610		1000 1050 910	850 800 630		1050 1100 930	ps
t_{SKEW}	Within-Device Skew (Note 2.) $Q_0 - Q_3$			50			50			50	ps
	Part-to-Part $Q_0 - Q_3$ (Diff)			200			200			200	
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_S	Setup Time $\overline{EN}$ to $\overline{CLK}$ DIVSEL to CLK	250 400			250 400			250 400			ps
t_H	Hold Time $\overline{CLK}$ to $\overline{EN}$ CLK to Div_Sel	100 150			100 150			100 150			ps
V_{PP}	Input Swing (Note 3.) CLK	250		1000	250		1000	250		1000	mV
t_{RR}	Reset Recovery Time			100			100			100	ps
t_{PW}	Minimum Pulse Width CLK MR	500 700			500 700			500 700			ps
t_r, t_f	Output Rise/Fall Times Q (20% – 80%)	280		550	280		550	280		550	ps

1. V_{EE} can vary ±0.3 V.
2. Skew is measured between outputs under identical transitions.
3. V_{PP}(min) is minimum input swing for which AC parameters are guaranteed. The device will function reliably with differential inputs down to 100 mV.

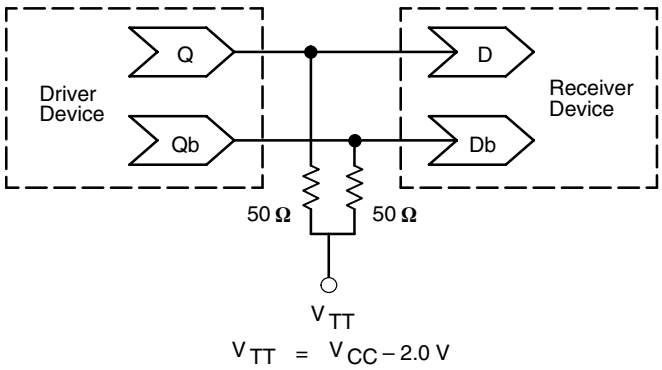


Figure 2. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC100LVEL40

3.3/5V ECL Differential Phase-Frequency Detector

The MC100LVEL40 is a three state phase frequency–detector intended for phase–locked loop applications which require a minimum amount of phase and frequency difference at lock. Advanced design significantly reduces the dead zone of the detector. For proper operation, the input edge rate of the R and V inputs should be less than 5 ns. The device is designed to work with a 3.3 V power supply.

When the reference (R) and the feedback (FB) inputs are unequal in frequency and/or phase the differential up (U) and down (D) outputs will provide pulse streams which when subtracted and integrated provide an error voltage for control of a VCO.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

For application information, see AND8040/D, “Phase Lock Loop Operation.”

The 100 Series Contains Temperature Compensation

- 250 MHz Typical Bandwidth
- ESD Protection: >2 KV HBM
- PECL Mode Operating Range: V_{CC}= 3.0 V to 5.5 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –3.0 V to –5.5 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 356 devices

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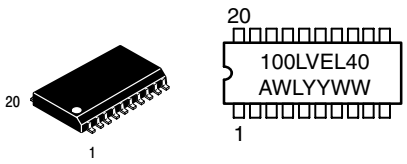
MARKING DIAGRAM



SO–20
DW SUFFIX
CASE 751D

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL40DW	SO–20	38 Units/Rail
MC100LVEL40DWR2	SO–20	1000 Units/Reel

January, 2001 – Rev. 4
Publication Order Number:
MC100LVEL40/D

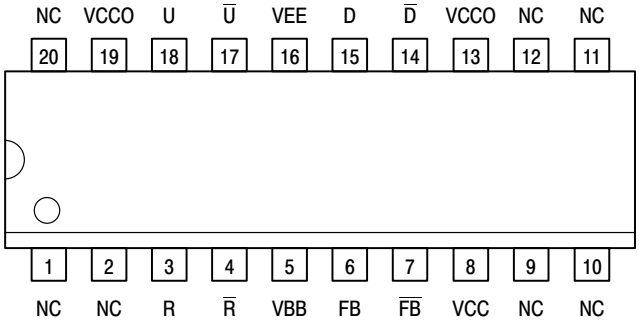


Figure 1. 20–Lead Pinout (Top View)

Warning: All V_{CC}, V_{CC}, and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

PIN	FUNCTION
U, $\overline{U}$	ECL Up Differential Outputs
D, $\overline{D}$	ECL Down Differential Outputs
FB, $\overline{FB}$	ECL Feedback Differential Inputs
R, $\overline{R}$	ECL Reference Differential Inputs
V_{BB}	Reference Voltage Output
V_{CC}, V_{CCO}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

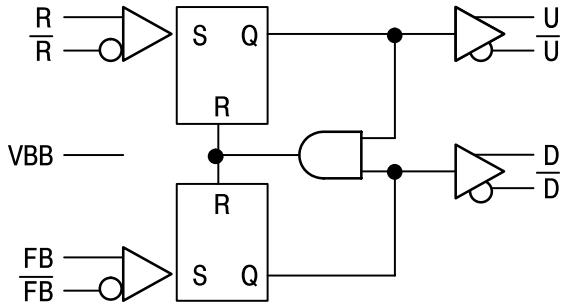


Figure 2. Logic Diagram

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V (Note 1)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current			45		45	47		45	47	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1380	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1490		1825	1490		1825	1490		1825	mV
V_{BB}	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.) Vpp < 500 mV Vpp ≧ 500 mV	 1.3 1.5		 3.3 3.3	 1.2 1.4		 3.3 3.3	 1.2 1.4		 3.3 3.3	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current Others $\overline{R}$, $\overline{FB}$	0.5 –300			0.5 –300			0.5 –300			μA μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

LVNECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current			45		45	47		45	47	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.43		–1.30	–1.35		–1.30	–1.31		–1.20	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 3.) Vpp < 500 mV Vpp ≧ 500 mV	 –2.0 –1.8		 –0.4 –0.4	 –2.1 –1.9		 –0.4 –0.4	 –2.1 –1.9		 –0.4 –0.4	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current Others $\overline{R}$, $\overline{FB}$	0.5 –300			0.5 –300			0.5 –300			μA μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. All loading with 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay R to U, FB to D	430 1200		630 1400	450 1250		650 1450	480 1370		680 1590	ps
V_{PP}	Input Swing (Note 2.)	150		1000	150		1000	150		1000	mV
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r, t_f	Output Rise/Fall Times	175		475	175		475	175		475	ps

1. V_{EE} can vary ±0.3 V.
2. $V_{PP(min)}$ is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

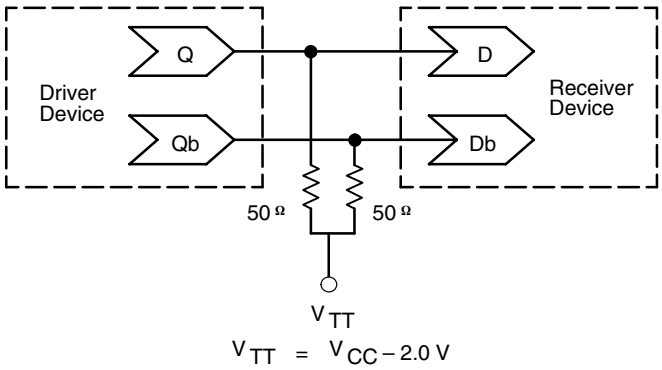


Figure 3. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 – ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405 – ECL Clock Distribution Techniques
AN1406 – Designing with PECL (ECL at +5.0 V)
AN1503 – ECLinPS I/O SPICE Modeling Kit
AN1504 – Metastability and the ECLinPS Family
AN1560 – Low Voltage ECLinPS SPICE Modeling Kit
AN1568 – Interfacing Between LVDS and ECL
AN1596 – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650 – Using Wire–OR Ties in ECLinPS Designs
AN1672 – The ECL Translator Guide
AND8001 – Odd Number Counters Design
AND8002 – Marking and Date Codes
AND8020 – Termination of ECL Logic Devices

MC100LVEL51

3.3V ECL Differential Clock D Flip-Flop

The MC100LVEL51 is a differential clock D flip-flop with reset. The device is functionally equivalent to the EL51 device, but operates from a 3.3 V supply. With propagation delays and output transition times essentially equal to the EL51, the LVEL51 is ideally suited for those applications which require the ultimate in AC performance at 3.3 V V_{CC}.

The reset input is an asynchronous, level triggered signal. Data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The differential clock inputs of the LVEL51 allow the device to be used as a negative edge triggered flip-flop.

The differential input employs clamp circuitry to maintain stability under open input conditions. When left open, the CLK input will be pulled down to V_{EE} and the $\overline{CLK}$ input will be biased at $V_{CC}/2$.

- 475 ps Propagation Delay
- 2.8 GHz Toggle Frequency
- ESD Protection: >4 KV HBM, >200 V MM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 3.0 V to 3.8 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –3.0 V to –3.8 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 114 devices

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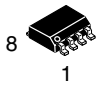
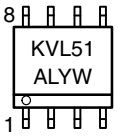
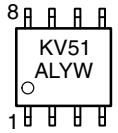
MARKING DIAGRAMS*



SO–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



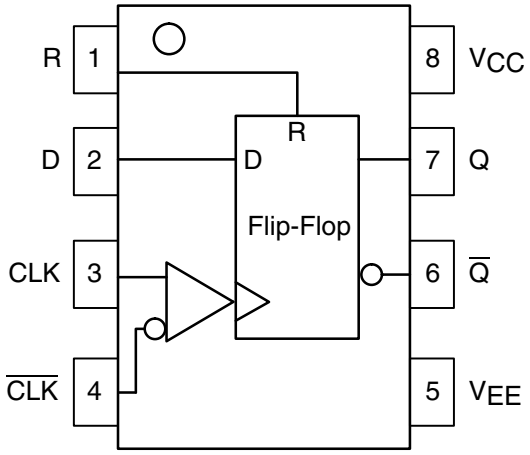
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL51D	SO–8	98 Units / Rail
MC100LVEL51DR2	SO–8	2500 / Reel
MC100LVEL51DT	TSSOP–8	98 Units / Rail
MC100LVEL51DTR2	TSSOP–8	2500 / Reel

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
CLK, $\overline{CLK}$	ECL Differential Clock Input
Q, $\overline{Q}$	ECL Differential Output
D	ECL D Input
R	ECL Reset Input
V_{CC}	Positive Supp;y
V_{EE}	Negative Supply

TRUTH TABLE

D	R	CLK	Q
L	L	Z	L
H	L	Z	H
X	H	X	L

Z = LOW to HIGH Transition
X = Don't Care

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44 ± 5%	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V (Note 1)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		30	35		30	35		32	37	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1490		1825	1490		1825	1490		1825	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.) Vpp < 500 mV Vpp ≧ 500 mV	 1.2 1.4		 3.0 3.0	 1.1 1.3		 3.0 3.0	 1.1 1.3		 3.0 3.0	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current Others $\overline{CLK}$	0.5 –600			0.5 –600			0.5 –600			μA μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

LVNECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		30	35		30	35		32	37	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.) Vpp < 500 mV Vpp ≧ 500 mV	 –2.1 –1.9		 –0.3 –0.3	 –2.2 –2.0		 –0.3 –0.3	 –2.2 –2.0		 –0.3 –0.3	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current Others $\overline{CLK}$	0.5 –600			0.5 –600			0.5 –600			μA μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency	2.7			2.8			2.9			GHz
t_{PLH} t_{PHL}	Propagation Delay to Output CLK R	330 340	465 455	510 540	340 350	475 765	520 550	370 390	530 510	550 590	ps
t_S	Setup Time	150	0		150	0		150	0		ps
t_H	Hold Time	200	100		200	100		200	100		ps
t_{RR}	Reset Recovery	350	200		350	200		350	200		ps
t_{PW}	Minimum Pulse Width CLK Reset	400 500			400 500			400 500			ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 2.)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	120		320	120		320	120		320	ps

1. V_{EE} can vary ±0.3 V.
2. V_{PP}(min) is minimum input swing for which AC parameters are guaranteed.

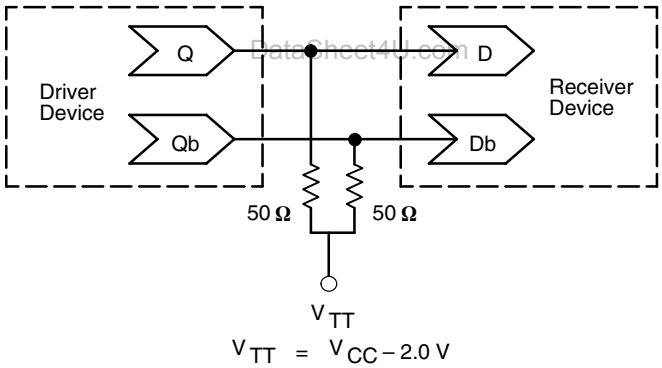


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC100LVEL56

3.3V ECL Dual Differential 2:1 Multiplexer

The MC100LVEL56 is a dual, fully differential 2:1 multiplexer. The differential data path makes the device ideal for multiplexing low skew clock or other skew sensitive signals.

The device features both individual and common select inputs to address both data path and random logic applications.

The differential inputs have special circuitry which ensures device stability under open input conditions. When both differential inputs are left open the D input will pull down to V_{EE}, The $\overline{D}$ input will bias around $V_{CC}/2$ forcing the Q output LOW.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- 440 ps Typical Propagation Delays
- Separate and Common Select
- ESD Protection: >2 KV HBM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 3.0 V to 3.8 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –3.0 V to –3.8 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 147 devices

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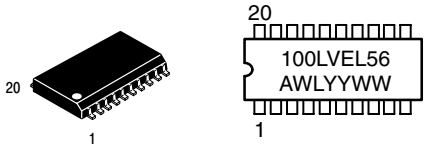
MARKING DIAGRAM



SOIC–20
DW SUFFIX
CASE 751D

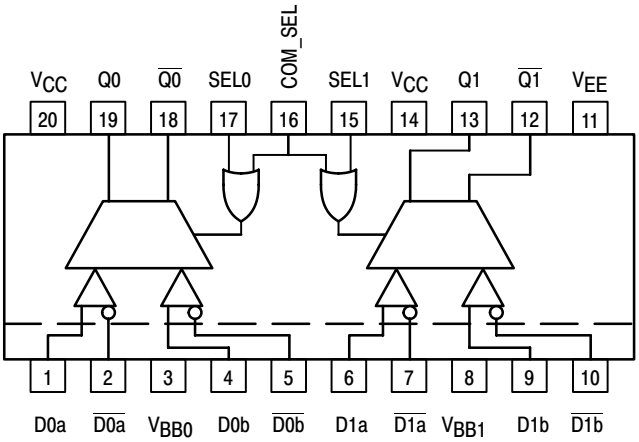
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL56DW	SOIC–20	38 Units/Rail
MC100LVEL56DWR2	SOIC–20	1000 Units/Reel

MC100LVEL56

Logic Diagram and Pinout: 20-Lead SOIC (Top View)



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

PIN	FUNCTION
D0a–D1a, $\overline{D0a–D1a}$	ECL Differential Input Data a
D0b–D1b, $\overline{D0b–D1b}$	ECL Differential Input Data b
SEL0–SEL1	ECL Individual Select Input
COM_SEL	ECL Common Select Input
Q0–Q1, $\overline{Q0–Q1}$	ECL Differential Outputs
V_{BB0}, V_{BB1}	Reference Voltage Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

TRUTH TABLE

SEL	Data
H	a
L	b

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V (Note 1)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		20	24		20	24		20	24	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1490		1825	1490		1825	1490		1825	mV
V_{BB}	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.) Vpp < 500 mV Vpp ≧ 500 mV	 1.3 1.5		 2.9 2.9	 1.2 1.4		 2.9 2.9	 1.2 1.4		 2.9 2.9	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current Dn $\overline{Dn}$	0.5 –600			0.5 –600			0.5 –600			μA μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

LVNECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		20	24		20	24		20	24	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3.) Vpp < 500 mV Vpp ≧ 500 mV	 –2.0 –1.8		 –0.4 –0.4	 –2.1 –1.9		 –0.4 –0.4	 –2.1 –1.9		 –0.4 –0.4	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current Dn $\overline{Dn}$	0.5 –600			0.5 –600			0.5 –600			μA μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

AC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay to Output D (Diff) D (SE) SEL COMSEL	340 290 430 430		540 590 730 730	360 310 440 440	440	560 610 740 740	380 330 450 450		580 630 750 750	ps
t_{SKEW}	Within–Device Skew (Note 2.)		40	80		40	80		40	80	ps
t_{SKEW}	Duty Cycle Skew (Note 3.)			100			100			100	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 4.)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	200		540	200		540	200		540	ps

1. V_{EE} can vary ±0.3 V.
2. Within-device skew is defined as identical transitions on similar paths through a device.
3. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.
4. V_{PP}(min) is minimum input swing for which AC parameters are guaranteed.

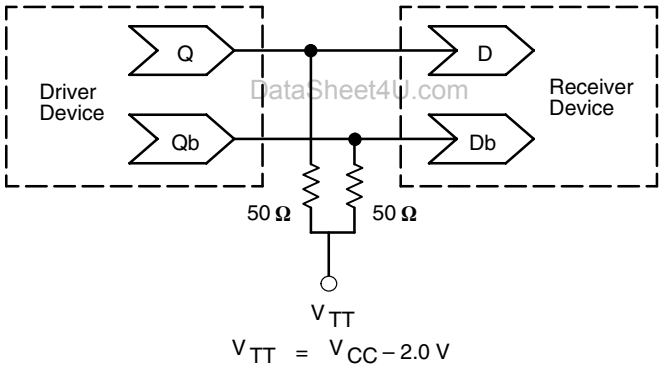


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC100LVEL58

3.3V ECL 2:1 Multiplexer

The MC100LVEL58 is a 2:1 multiplexer. The device is pin and functionally equivalent to the EL58 and works from a 3.3 V supply. With AC performance similar to the EL58 device, the LVEL58 is ideal for low voltage applications which require the ultimate in AC performance.

- 440 ps Typical Propagation Delays
- ESD Protection: >4 KV HBM, >200 V MM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 3.0 V to 3.8 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –3.0 V to –3.8 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 93 devices

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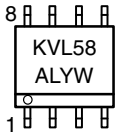
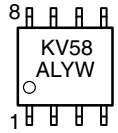
MARKING DIAGRAM*

SOIC–8
D SUFFIX
CASE 751



TSSOP–8
DT SUFFIX
CASE 948R



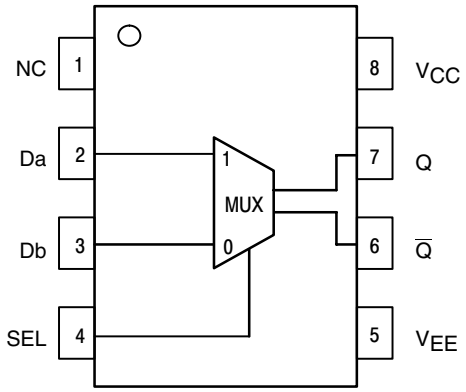
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL58D	SOIC–8	98 Units / Rail
MC100LVEL58DR2	SOIC–8	2500 / Reel
MC100LVEL58DT	TSSOP–8	98 Units / Rail
MC100LVEL58DTR2	TSSOP–8	2500 / Reel

LOGIC DIAGRAM AND PINOUT: ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
Da, Db	ECL Data Inputs
Q, $\overline{Q}$	ECL Differential Data Outputs
SEL	ECL Select Input
V_{CC}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

TRUTH TABLE

SEL	Data
H	a
L	b

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44 ± 5%	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V (Note 1)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		21	28		21	28		23	30	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage	1490		1825	1490		1825	1490		1825	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

LVNECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		21	28		21	28		23	30	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage	–1810		–1475	–1810		–1475	–1810		–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.
1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation D to Q Delay SEL to Q	340 350	435 455	560 570	350 360	440 460	570 580	370 380	450 470	590 600	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	100		320	100		320	100		320	ps

1. V_{EE} can vary ±0.3 V.

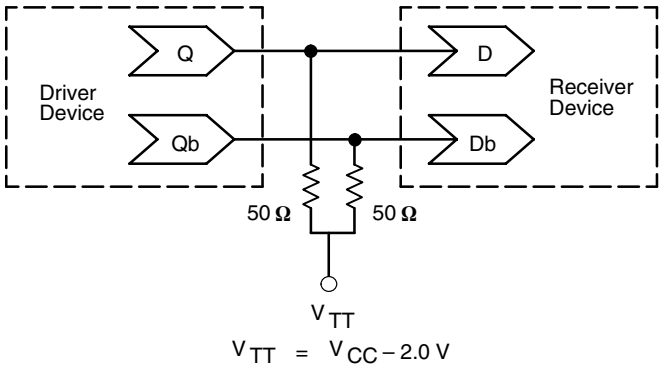


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC100LVEL59

3.3V ECL Triple 2:1 Multiplexer

The MC100LVEL59 is a 3.3 V triple 2:1 multiplexer with differential outputs. The output data of the multiplexers can be controlled individually via the select inputs or as a group via the common select input. The flexible selection scheme makes the device useful for both data path and random logic applications.

- Individual or Common Select Controls
- 500 ps Typical Propagation Delays
- ESD Protection: >2 KV HBM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC}= 3.0 V to 3.8 V with V_{EE}= 0 V
- NECL Mode Operating Range: V_{CC}= 0 V with V_{EE}= –3.0 V to –3.8 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”, Oxygen Index 28 to 34
- Transistor Count = 182 devices

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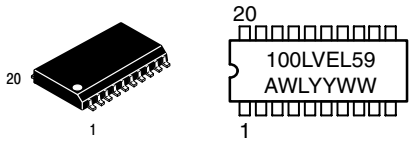
MARKING DIAGRAM*



SO–20
DW SUFFIX
CASE 751D

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

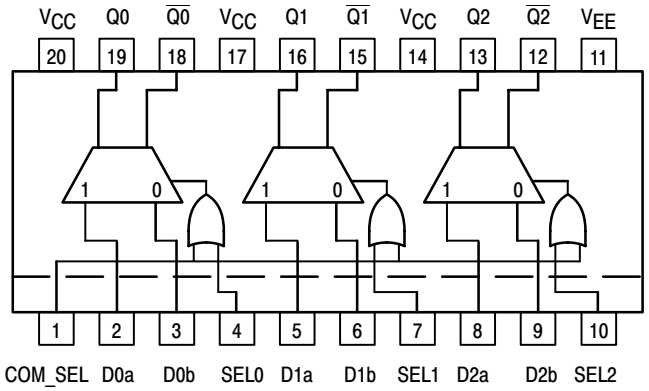
*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL59DW	SO–20	38 Units/Rail
MC100LVEL59DWR2	SO–20	1000 Units/Reel

MC100LVEL59

Logic Diagram and Pinout: 20–Lead SOIC (Top View)



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

Pins	Function
D0a–D2a	ECL Input Data a
D0b–D2b	ECL Input Data b
SEL0–SEL2	ECL Individual Select Input
COM_SEL	ECL Common Select Input
Q0–Q2; $\overline{Q0}$–$\overline{Q2}$	ECL Differential Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

TRUTH TABLE

SEL	Data
H	a
L	b

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		8 to 0	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–8 to 0	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 to 0 –6 to 0	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	140 100	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V (Note 1)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		27	32		27	32		27	32	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage	1490		1825	1490		1825	1490		1825	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

LVNECL DC CHARACTERISTICS V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		27	32		27	32		27	32	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV
V_{IH}	Input HIGH Voltage	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage	–1810		–1475	–1810		–1475	–1810		–1475	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary ±0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= 0.0 V or V_{CC}= 0.0 V; V_{EE}= –3.3 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay DATA to Q/$\overline{Q}$ SEL to Q/$\overline{Q}$ COM_SEL to Q/$\overline{Q}$	340 340 340		690 690 690	340 340 340		690 690 690	340 340 340		690 690 690	ps
t_{skew}	Output–Output Skew Any D_n, D_m to Q			100			100			100	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	200		540	200		540	200		540	ps

1. V_{EE} can vary ±0.3 V.

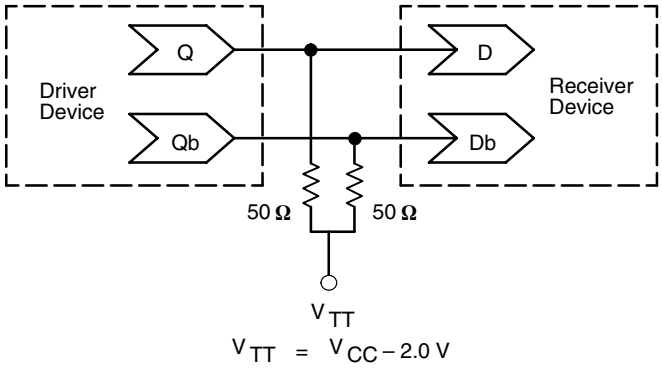


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC100LVEL90

-3.3V / -5V Triple ECL Input to LVPECL Output Translator

The MC100LVEL90 is a triple ECL to LVPECL translator. The device receives either –3.3 V or –5 V differential ECL signals, determined by the V_{EE} supply level, and translates them to +3.3 V differential LVPECL output signals.

To accomplish the level translation, the LVEL90 requires three power rails. The V_{CC} supply should be connected to the positive supply, and the V_{EE} pin should be connected to the negative power supply. The GND pins, as expected, are connected to the system ground plane. Both V_{EE} and V_{CC} should be bypassed to ground via 0.01 μF capacitors.

Under open input conditions, the $\overline{D}$ input will be biased at $V_{EE}/2$ and the D input will be pulled to V_{EE}. This condition will force the Q output to a LOW, ensuring stability.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- 500 ps Propagation Delays
- ESD Protection: >2 KV HBM, >200 V MM
- The 100 Series Contains Temperature Compensation
- Operating Range: V_{CC}= 3.0 V to 3.8 V; V_{EE}= –3.0 V to –5.5 V; GND= 0 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at V_{EE}
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 261 devices

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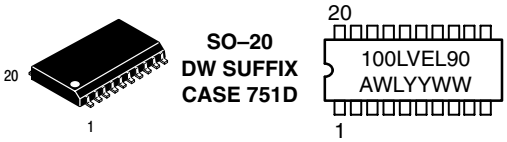
MARKING DIAGRAM*



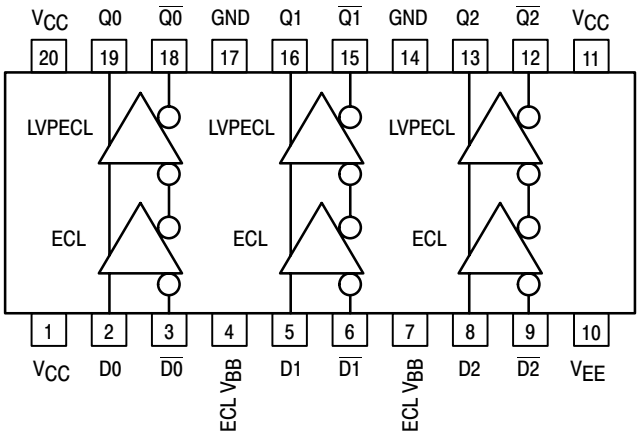
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL90DW	SO–20	38 Units/Rail
MC100LVEL90DWR2	SO–20	1000 Units/Reel

Logic Diagram and Pinout: 20-Lead SOIC (Top View)



* All V_{CC} pins are tied together on the die.

Warning: All V_{CC}, V_{EE}, and GND pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

PIN	FUNCTION
Dn, $\overline{Dn}$	ECL Inputs
Qn, $\overline{Qn}$	LVPECL Outputs
ECL V_{BB}	ECL Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
GND	Ground

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Power Supply	GND = 0 V		8 to 0	V
V_{EE}	NECL Power Supply	GND = 0 V		–8 to 0	V
V_I	NECL Mode Input Voltage	GND = 0 V	$V_I \geq V_{EE}$	–6 to 0	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	ECL V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder			265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

NECL INPUT DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= –3.3 V; GND= 0 V (Note 1)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	V_{EE} Power Supply Current			8.0		6.0	8.0			8.0	mA
V_{IH}	Input HIGH Voltage (Single Ended)	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1810		–1475	–1810		–1475	–1810		–1475	mV
ECL V_{BB}	Output Voltage Reference	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 2.) Vpp < 500 mV Vpp ≧ 500 mV	 V_{EE}+1.3 VEE+1.5		 –0.4 –0.4	 V_{EE}+1.2 VEE+1.4		 –0.4 –0.4	 V_{EE}+1.2 VEE+1.4		 –0.4 –0.4	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –600			0.5 –600			0.5 –600			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input parameters vary 1:1 with GND. V_{EE} can vary –3.0 V to –5.5 V.
2. V_{IHCMR} min varies 1:1 with V_{EE}. V_{IHCMR} max varies 1:1 with GND.

LVPECL OUTPUT DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= –3.3 V; GND= 0 V (Note 1)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{CC}	V_{CC} Power Supply Current			24		20	24			26	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1380	1490	1595	1680	mV

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Output parameters vary 1:1 with V_{CC}. V_{CC} can vary +0.5 V / –0.3 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}–2 volts.

AC CHARACTERISTICS V_{CC}= 3.0 V to 3.8 V; V_{EE}= –3.0 V to –5.5 V; GND= 0 V

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		560			650			700		MHz
t_{PLH} t_{PHL}	Propagation Delay Diff D to Q S.E.	390 340		590 640	420 370		620 670	460 410		660 710	ps
t_{SKEW}	Skew Output–to–Output (Note 1) Part–to–Part (Diff) (Note 1) Duty Cycle (Diff) (Note 2)		20 25	100 200		20 25	100 200		20 25	100 200	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 3)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	230		500	230		500	230		500	ps

1. Skews are valid across specified voltage range, part–to–part skew is for a given temperature.
2. Duty cycle skew is the difference between a TPLH and TPHL propagation delay through a device.
3. V_{PP}(min) is the minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈40.

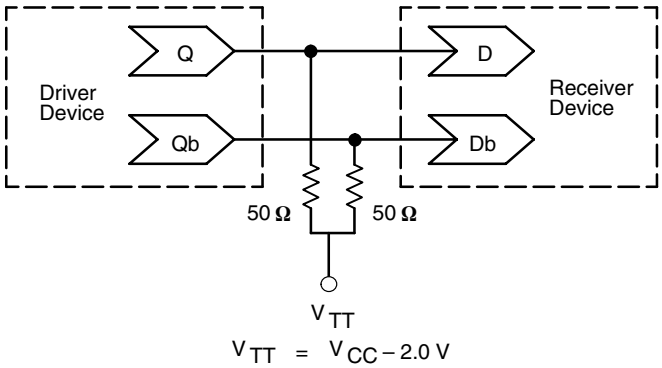


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC100LVEL91

3.3V / 5V Triple LVPECL / PECL Input to -3.3V ECL Output Translator

The MC100LVEL91 is a triple LVPECL / PECL input to ECL output translator. The device receives standard or low voltage differential PECL signals, determined by the V_{CC} supply level, and translates them to differential –3.3 V ECL output signals. (For translation to –5 V ECL output, see MC100EL91.)

To accomplish the level translation the LVEL91 requires three power rails. The V_{CC} supply should be connected to the positive supply, and the V_{EE} pin should be connected to the negative power supply. The GND pins are connected to the system ground plane. Both V_{EE} and V_{CC} should be bypassed to ground via 0.01μF capacitors.

Under open input conditions, the $\overline{D}$ input will be biased at $V_{CC}/2$ and the D input will be pulled to GND. This condition will force the Q output to a low, ensuring stability.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- 620 ps Typical Propagation Delay
- ESD Protection: >2 KV HBM
- The 100 Series Contains Temperature Compensation
- Operating Range: V_{CC}= 3.0 V to 5.25 V; V_{EE}= –3.0 V to –3.8 V; GND= 0 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at GND
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 282 devices

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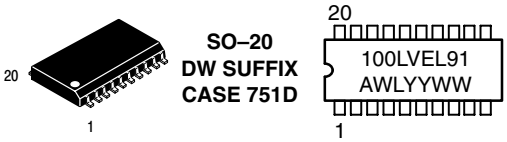
MARKING DIAGRAM*



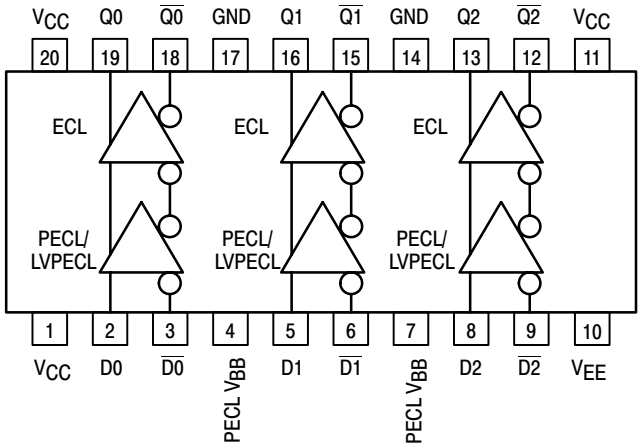
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL91DW	SO–20	38 Units/Rail
MC100LVEL91DWR2	SO–20	1000 Units/Reel

20–Lead Pinout (Top View) **and Logic Diagram**



* All V_{CC} pins are tied together on the die.

Warning: All V_{CC}, V_{EE}, and GND pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

PIN	FUNCTION
Dn, $\overline{Dn}$	PECL/LVPECL Inputs
Qn, $\overline{Qn}$	ECL Outputs
PECL V_{BB}	PECL Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
GND	Ground

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Power Supply	GND = 0 V		8 to 0	V
V_{EE}	NECL Power Supply	GND = 0 V		–8 to 0	V
V_I	PECL Input Voltage	GND = 0 V	$V_I \leq V_{CC}$	6 to 0	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	PECL V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

LVPECL INPUT DC CHARACTERISTICS V_{CC}= 3.3 V; V_{EE}= –3.3 V; GND= 0 V (Note 1)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{CC}	V_{CC} Power Supply Current			11		6	11			11	mA
V_{IH}	Input HIGH Voltage (Single Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1490		1825	1490		1825	1490		1825	mV
LVPECL V_{BB}	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 2.) Vpp < 500 mV Vpp ≧ 500 mV	 1.0 1.2		 2.9 2.9	 0.9 1.1		 2.9 2.9	 0.9 1.1		 2.9 2.9	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –600			0.5 –600			0.5 –600			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input parameters vary 1:1 with V_{CC}. V_{CC} can vary +0.5 / –0.3 V.
2. V_{IHCMR} min varies 1:1 with GND. V_{IHCMR} max varies 1:1 with V_{CC}.

PECL INPUT DC CHARACTERISTICS V_{CC}= 5.0 V; V_{EE}= –3.3 V; GND= 0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{CC}	V_{CC} Power Supply Current			11		6	11			11	mA
V_{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
PECL V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 2.) Vpp < 500 mV Vpp ≧ 500 mV	 1.0 1.2		 4.6 4.6	 0.9 1.1		 4.6 4.6	 0.9 1.1		 4.6 4.6	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –600			0.5 –600			0.5 –600			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input parameters vary 1:1 with V_{CC}. V_{CC} can vary ± 0.25 V.
2. V_{IHCMR} min varies 1:1 with GND. V_{IHCMR} max varies 1:1 with V_{CC}.

NECL OUTPUT DC CHARACTERISTICS V_{CC}= 3.3 V to 5.0 V; V_{EE}= –3.3 V; GND= 0 V (Note 1.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	V_{EE} Power Supply Current			27		21	27			29	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1085	–1005	–880	–1025	–955	–880	–1025	–955	–880	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1830	–1695	–1555	–1810	–1705	–1620	–1810	–1705	–1620	mV

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Output parameters vary 1:1 with GND. V_{EE} can vary +0.3 V / –0.5 V.
2. All loading with 50 ohm resistor to GND–2 volts.

AC CHARACTERISTICS V_{CC}= 3.0 V to 5.5 V; V_{EE}= –3.0 V to –3.8 V; GND = 0 V

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		200			600			600		MHz
t_{PLH} t_{PHL}	Propagation Delay Diff D to Q S.E.	490 440	590 590	690 740	520 470	620 620	720 770	560 510	660 660	760 810	ps
t_{SKEW}	Skew Output–to–Output (Note 4.) Part–to–Part (Diff) (Note 4.) Duty Cycle (Diff) (Note 5.)		40 25	100 200		40 25	100 200		40 25	100 200	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 6.)	200		1000	200		1000	200		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	320	400	580	320	400	580	320	400	580	ps

4. Skews are valid across specified voltage range, part–to–part skew is for a given temperature.
5. Duty cycle skew is the difference between a TPLH and TPHL propagation delay through a device.
6. V_{PP}(min) is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈40.

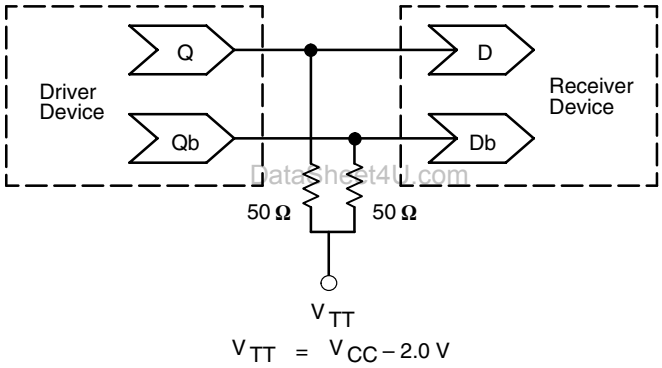


Figure 1. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

MC100LVEL92

5V Triple PECL Input to LVPECL Output Translator

The MC100LVEL92 is a triple PECL input to LVPECL output translator. The device receives standard PECL signals and translates them to differential LVPECL output signals.

To accomplish the PECL to LVPECL level translation, the MC100LVEL92 requires three power rails. The V_{CC} supply is to be connected to the standard 5 V PECL supply, the LVCC supply is to be connected to the 3.3 V LVPECL supply, and Ground is connected to the system ground plane. Both the V_{CC} and LVCC should be bypassed to ground with 0.01 μf capacitors.

The PECL V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- 500 ps Propagation Delays
- 5 V and 3.3 V Supplies Required
- ESD Protection: >2 KV HBM, >200 V MM
- The 100 Series Contains Temperature Compensation
- LVPECL Operating Range: LV_{CC}= 3.0 V to 3.8 V
- PECL Operating Range: V_{CC}= 4.5 V to 5.5 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or < GND+1.3 V
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
  For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8”,
  Oxygen Index 28 to 34
- Transistor Count = 247 devices

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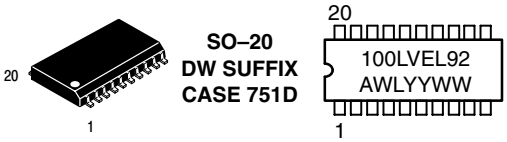
MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

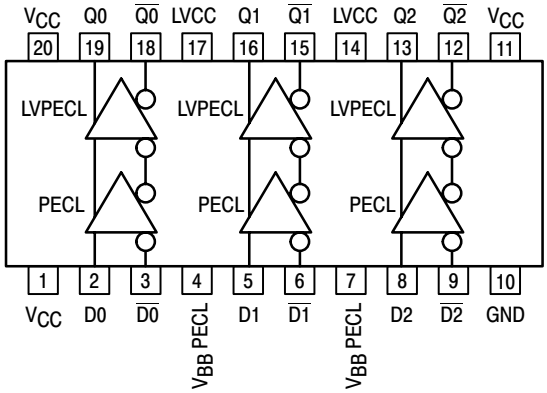
*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEL92DW	SO–20	38 Units/Rail
MC100LVEL92DWR2	SO–20	1000 Units/Reel

January, 2001 – Rev. 5
Publication Order Number:
MC100LVEL92/D

Logic Diagram and Pinout: 20-Lead SOIC (Top View)



Warning: All V_{CC}, LV_{CC}, and GND pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

PIN	FUNCTION
Dn, $\overline{Dn}$	PECL Inputs
Qn, $\overline{Qn}$	LVPECL Outputs
PECL V_{BB}	PECL Reference Voltage Output
LVCC	LVPECL Power Supply
V_{CC}	PECL Power Supply
GND	Common Ground Rail

MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Power Supply	GND = 0 V		8 to 0	V
LV_{CC}	LVPECL Power Supply	GND = 0 V		–8 to 0	V
V_I	PECL Input Voltage	GND = 0 V	$V_I \leq V_{CC}$	6 to 0	V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	PECL V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

PECL INPUT DC CHARACTERISTICS V_{CC}= 5.0 V; LV_{CC}= 3.3 V; GND= 0 V Note 1)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IV_{CC}	PECL Power Supply Current			12			12			12	mA
V_{IH}	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3190		3515	3190		3525	3190		3525	mV
PECL V_{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (DIfferential) (Note 2.) Vpp < 500 mV Vpp ≧ 500 mV	 1.3 1.5		 4.8 4.8	 1.2 1.4		 4.8 4.8	 1.2 1.4		 4.8 4.8	 V V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	0.5 –600			0.5 –600			0.5 –600			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input parameters vary 1:1 with V_{CC}. V_{CC} can vary 4.5 V to 5.5 V.
2. V_{IHCMR} min varies 1:1 with GND. V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1 V.

LVPECL OUTPUT DC CHARACTERISTICS V_{CC}= 5.0 V; LV_{CC}= 3.3 V; GND= 0 V (Note 1)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
ILV_{CC}	LVPECL Power Supply Current			20			20			21	mA
V_{OH}	Output HIGH Voltage (Note 2.)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage (Note 2.)	1470	1605	1745	1490	1595	1380	1490	1595	1680	mV

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Output parameters vary 1:1 with LV_{CC}. V_{CC} can vary 3.0 V to 3.8 V.
2. Outputs are terminated through a 50 ohm resistor to GND–2 volts.

AC CHARACTERISTICS V_{CC}= 5.0 V; LV_{CC}= 3.3 V; GND= 0 V (Note 7.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t_{PLH} t_{PHL}	Propagation Delay Diff D to Q S.E.	490 440	590 590	690 740	510 460	610 610	710 760	530 480	630 630	730 780	ps
t_{SKEW}	Skew Output–to–Output (Note 8.) Part–to–Part (Diff) (Note 8.) Duty Cycle (Diff) (Note 9.)		20 20 25	100 200		20 20 25	100 200		20 20 25	100 200	ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Input Swing (Note 10.)	150		1000	150		1000	150		1000	mV
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	320		580	320		580	320		580	ps

7. LV_{CC} can vary 3.0 V to 3.8 V; V_{CC} can vary 4.5 V to 5.5 V.
8. Skews are valid across specified voltage range, part–to–part skew is for a given temperature.
9. Duty cycle skew is the difference between a TPLH and TPHL propagation delay through a device.
10. V_{PP}(min) is the minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈40.

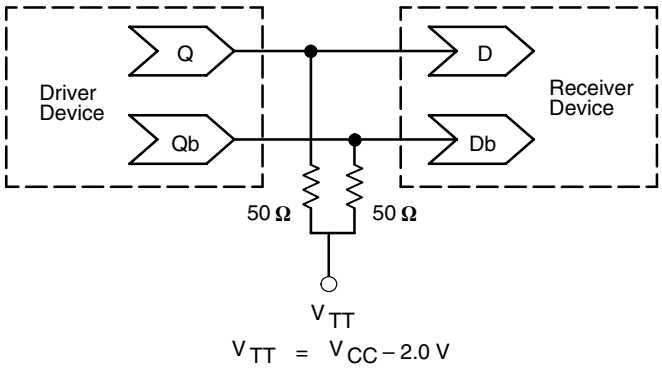


Figure 1. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1503	–	ECLinPS I/O SPICE Modeling Kit
AN1504	–	Metastability and the ECLinPS Family
AN1560	–	Low Voltage ECLinPS SPICE Modeling Kit
AN1568	–	Interfacing Between LVDS and ECL
AN1596	–	ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8020	–	Termination of ECL Logic Devices

CHAPTER 4
Case Outlines and Package Dimensions

Device Nomenclatures

ECLinPS, ECLinPS Lite, ECLinPS Plus

MC WWW XXX YYY ZZ

Circuit Identifier
- MC = Fully Qualified Circuit
- XC = Non Reliability Qualified

Compatibility Identifier
- 10 = 10H Compatible (0 to +85°C)
- 100 = 100K Compatible (0 to +85°C)

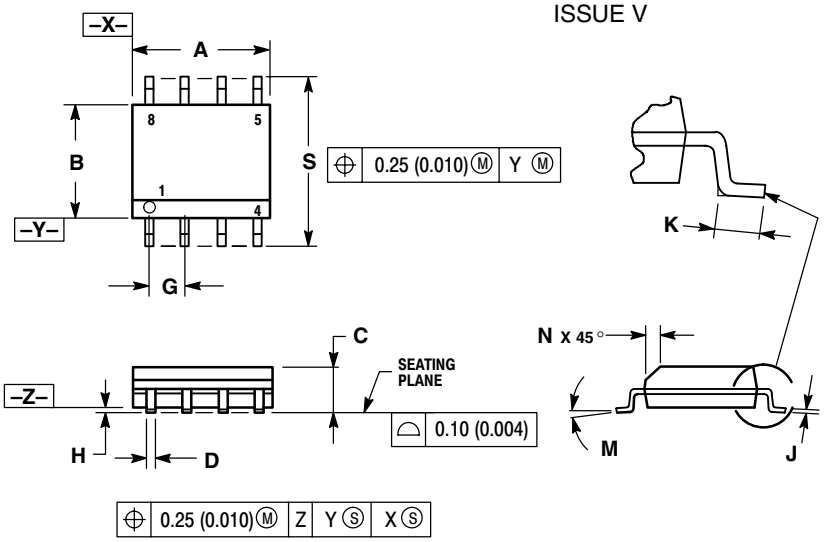
ECLinPS Family Identifier
- E = ECLinPS
- EL = ECLinPS Lite
- ELT = ECLinPS Lite Translator
- EP = ECLinPS Plus
- EPT = ECLinPS Plus Translator
- LVEP = Low Voltage ECLinPS Plus
- LVE = Low Voltage ECLinPS
- LVEL = Low Voltage ECLinPS Lite
- LVELT = Low Voltage ECLinPS Lite Translator

Function Type
- YYY = 3–Digits for ECLinPS
- YY= 2–Digits for ECLinPS Lite

Package Type
- FN = PLCC
- D = Plastic SOIC
- L = Ceramic DIP
- P = Plastic DIP

CASE OUTLINES AND PACKAGE DIMENSIONS

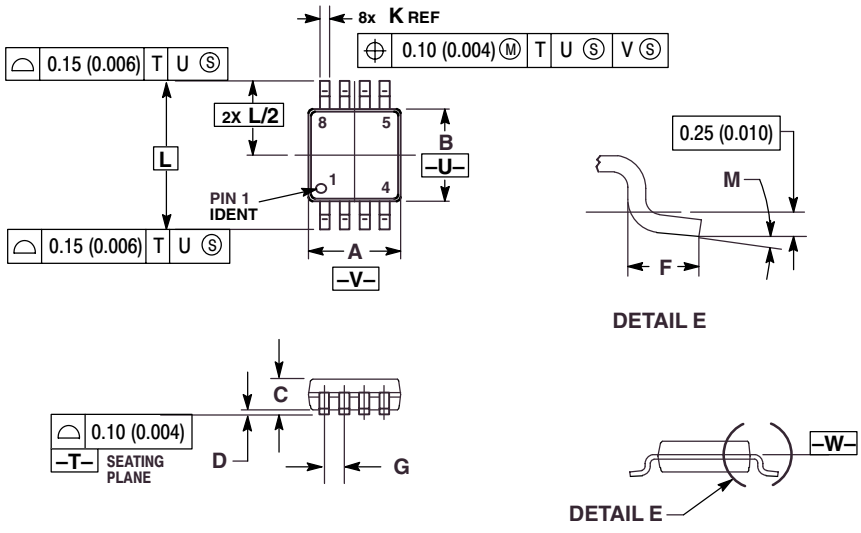
SO–8
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751–07
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

TSSOP–8
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948R–02
ISSUE A

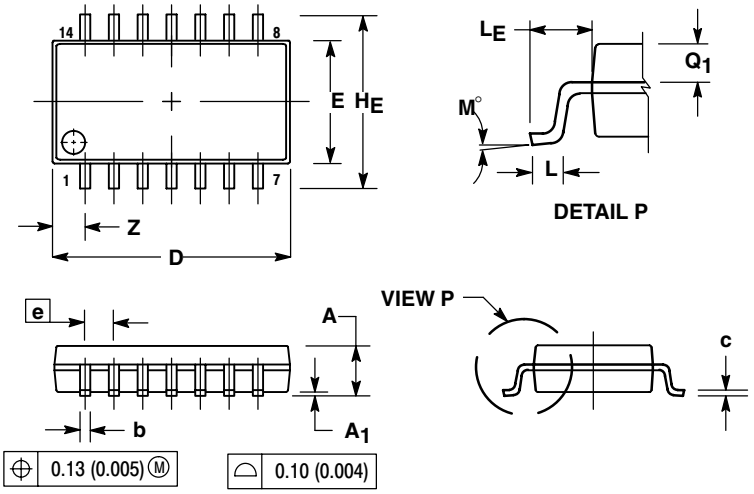


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0 °	6 °	0 °	6 °

CASE OUTLINES AND PACKAGE DIMENSIONS

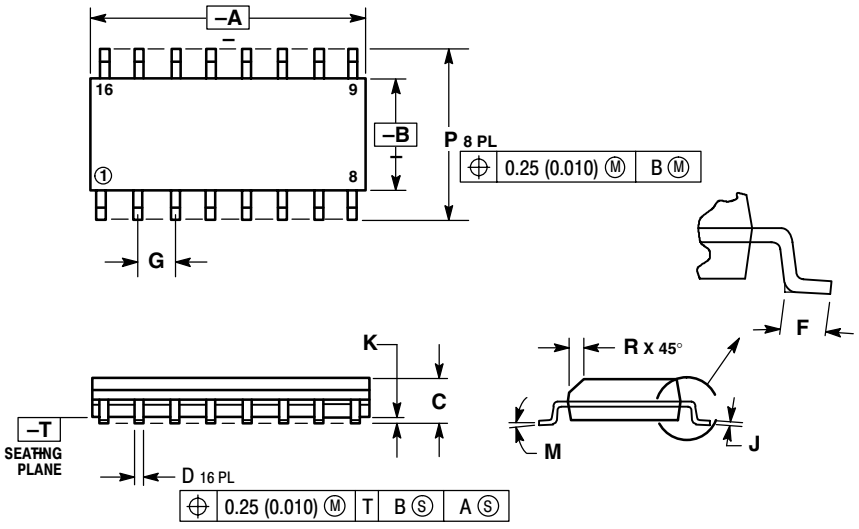
SOIC EIAJ–14
M SUFFIX
CASE 965–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

SO–16
D SUFFIX
CASE 751B–05
ISSUE J

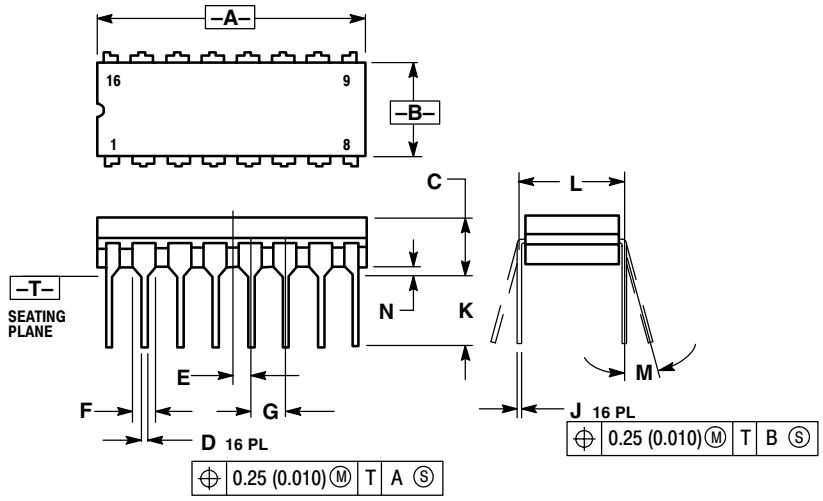


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

CASE OUTLINES AND PACKAGE DIMENSIONS

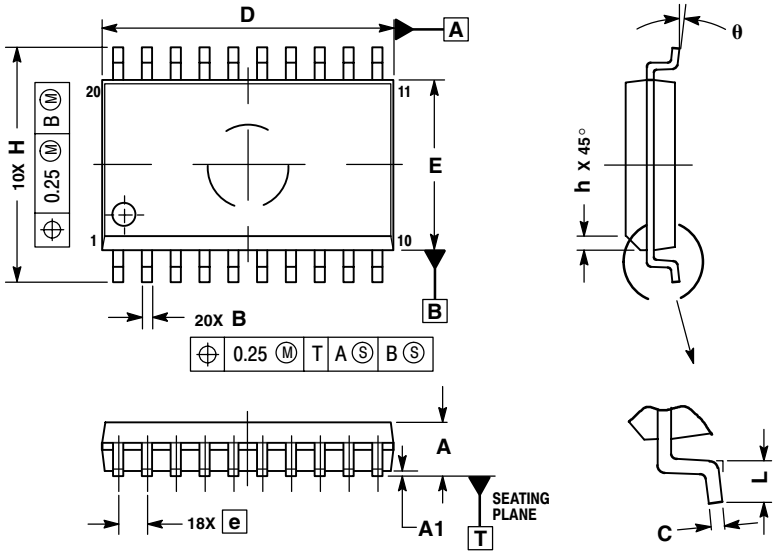
CDIP–16
L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	---	0.200	---	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.01

SO–20
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D–05
ISSUE F

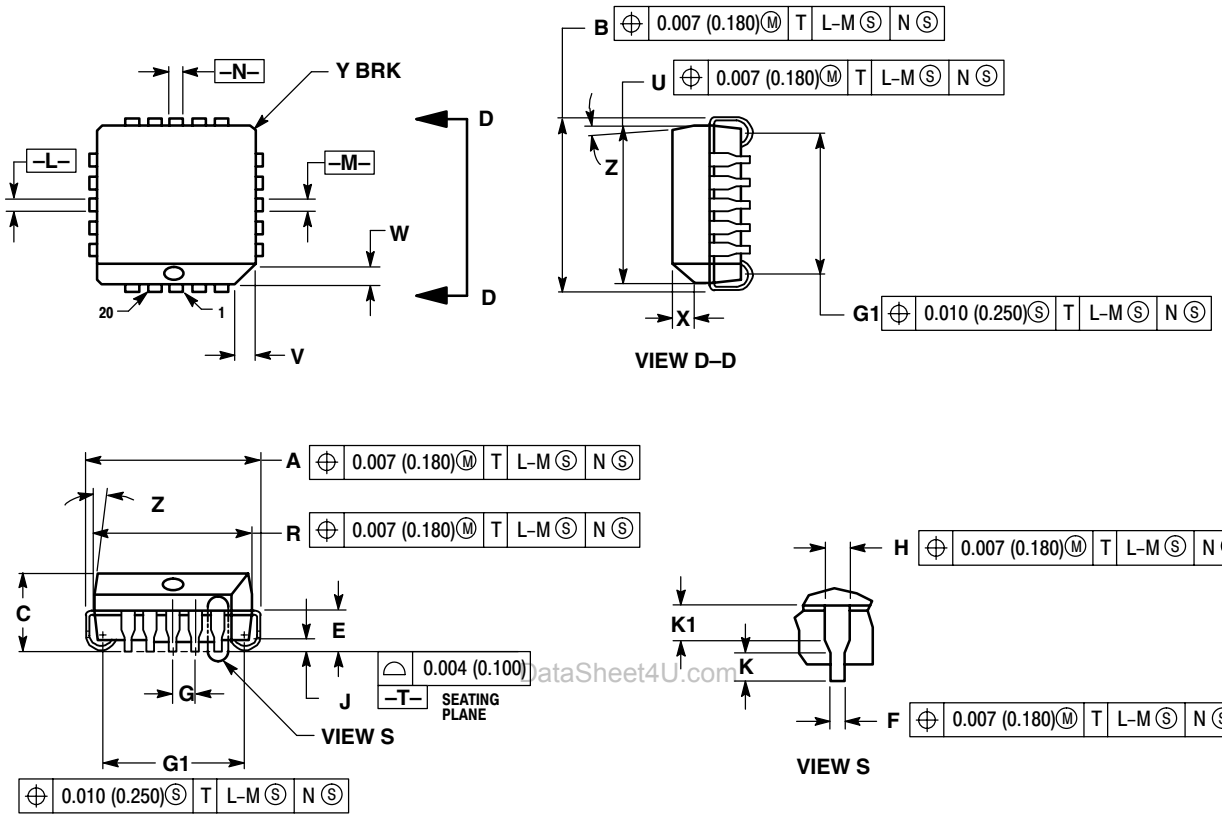


NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

CASE OUTLINE AND PACKAGE DIMENSIONS

PLCC–20
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775–02
ISSUE D

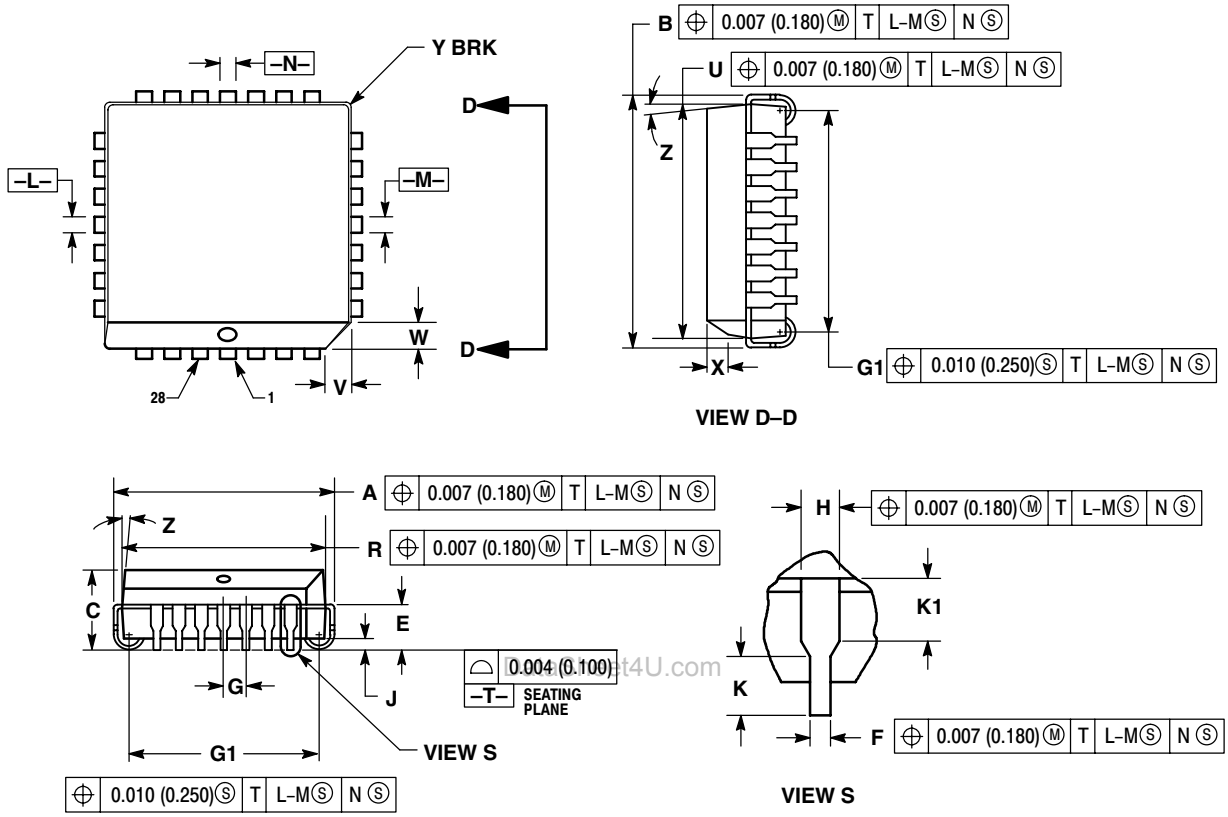


NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.310	0.330	7.88	8.38
K1	0.040	---	1.02	---

CASE OUTLINE AND PACKAGE DIMENSIONS

PLCC–28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776–02
ISSUE E

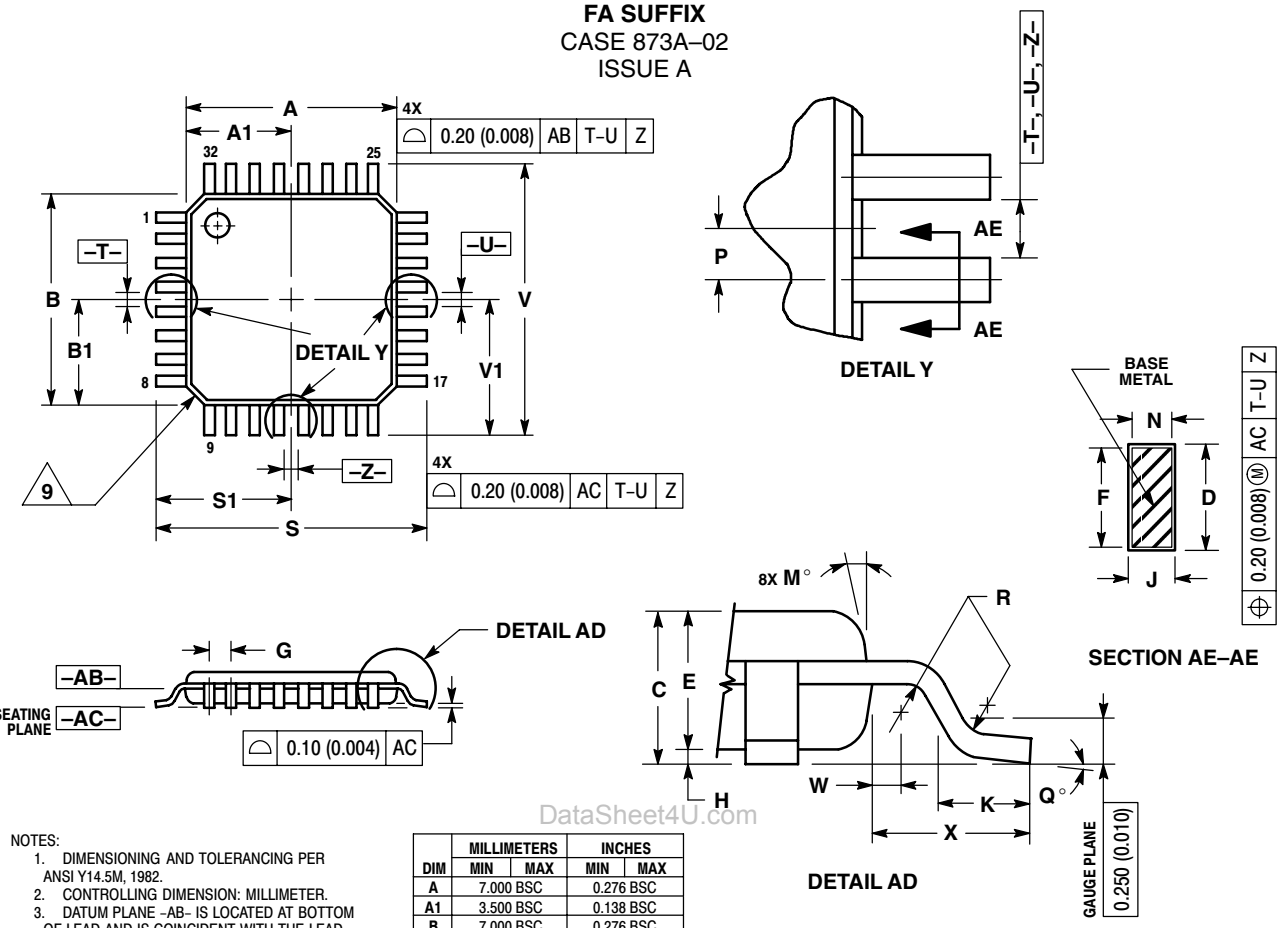


NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2 °	10 °	2 °	10 °
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

CASE OUTLINE AND PACKAGE DIMENSIONS

TQFP–32
FA SUFFIX
CASE 873A–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

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PRODUCT PREVIEW

A Product Preview is a summary document for a product/device under consideration or in the early stages of development. The Product Preview exists only until an "Advance Information" document is published that replaces it. The Product Preview is often used as the first section or chapter in a corresponding reference manual. The Product Preview displays the following disclaimer at the bottom of the first page: "This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice."

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A Handbook is a publication that contains a collection of information on almost any give subject which does not fall into the Reference Manual definition. The subject matter can consist of information ranging from a device specific design information, to system design, to quality and reliability information.

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