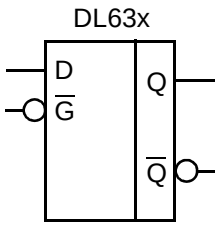
Description

DL63x is a family of transparent, buffered D latches with active low gate transparency and without SET or RESET.

Logic Symbol



Truth Table

D	GN	Q	QN
L	L	L	H
H	L	H	L
X	H	NC	NC

NC = No Change

HDL Syntax

Verilog ..... DL63x *inst_name* (Q, QN, D, GN);

VHDL..... *inst_name*: DL63x port map (Q, QN, D, GN);

Pin Loading

Pin Name	Equivalent Loads			
	DL631	DL632	DL634	DL636
D	1.1	1.0	1.0	1.0
GN	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DL631	5.0	TBD	12.0
DL632	6.0	TBD	15.3
DL634	9.0	TBD	23.7
DL636	12.0	TBD	33.5

a. See page 2-15 for power equation.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
DL631	From: D To: Q	t_{PLH} t_{PHL}	0.66 0.71	0.76 0.81	0.87 0.93	1.00 1.07	1.09 1.18
	From: D To: QN	t_{PLH} t_{PHL}	0.61 0.58	0.71 0.70	0.83 0.83	0.96 0.98	1.06 1.09
	From: GN To: Q	t_{PLH} t_{PHL}	0.77 0.90	0.87 1.00	0.98 1.12	1.11 1.26	1.21 1.37
	From: GN To: QN	t_{PLH} t_{PHL}	0.78 0.68	0.88 0.79	1.00 0.92	1.13 1.08	1.24 1.20
	Number of Equivalent Loads		**1**	**8**	**15**	**22**	**30 (max)**
DL632	From: D To: Q	t_{PLH} t_{PHL}	0.76 0.80	0.86 0.92	0.95 1.03	1.05 1.13	1.16 1.23
	From: D To: QN	t_{PLH} t_{PHL}	0.62 0.58	0.74 0.74	0.84 0.86	0.95 0.97	1.06 1.08
	From: GN To: Q	t_{PLH} t_{PHL}	0.87 0.99	0.97 1.11	1.06 1.21	1.14 1.30	1.24 1.40
	From: GN To: QN	t_{PLH} t_{PHL}	0.80 0.70	0.91 0.86	1.01 0.96	1.10 1.06	1.21 1.17
	Number of Equivalent Loads		**1**	**14**	**28**	**42**	**56 (max)**
DL634	From: D To: Q	t_{PLH} t_{PHL}	0.82 0.93	0.93 1.01	1.02 1.12	1.11 1.23	1.18 1.36
	From: D To: QN	t_{PLH} t_{PHL}	0.67 0.58	0.74 0.73	0.83 0.84	0.94 0.94	1.05 1.03
	From: GN To: Q	t_{PLH} t_{PHL}	0.96 1.12	1.01 1.24	1.10 1.34	1.20 1.43	1.31 1.51
	From: GN To: QN	t_{PLH} t_{PHL}	0.85 0.69	0.90 0.79	0.99 0.91	1.10 1.04	1.22 1.17

	Number of Equivalent Loads		1	21	42	62	83 (max)
DL636	From: D To: Q	t_{PLH} t_{PHL}	0.87 0.97	0.94 1.07	1.02 1.18	1.11 1.29	1.22 1.40
	From: D To: QN	t_{PLH} t_{PHL}	0.74 0.65	0.86 0.74	0.94 0.85	1.01 0.96	1.08 1.08
	From: GN To: Q	t_{PLH} t_{PHL}	0.99 1.18	1.07 1.31	1.15 1.39	1.23 1.47	1.34 1.56
	From: GN To: QN	t_{PLH} t_{PHL}	0.93 0.77	1.04 0.90	1.12 1.01	1.19 1.09	1.26 1.17

Delay will vary with input conditions. See page 2-Reference for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DL631	DL632	DL634	DL636
Min GN Width	Low	t_w	0.66	0.69	0.73	0.83
Min D Setup		t_{su}	0.47	0.50	0.54	0.64
Min D Hold		t_h	0.14	0.14	0.14	0.14

Logic Schematic