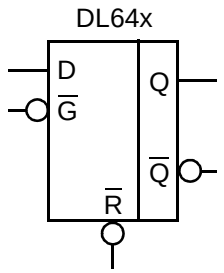
AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

DL64x is a family of transparent, buffered D latches with active low gate transparency. RESET is active low.

Logic Symbol



Truth Table

RN	D	GN	Q	QN
H	L	L	L	H
H	H	L	H	L
H	X	H	NC	NC
L	X	X	L	H

NC = No Change

HDL Syntax

Verilog ..... DL64x *inst_name* (Q, QN, D, GN);

VHDL..... *inst_name*: DL64x port map (Q, QN, D, GN);

Pin Loading

Pin Name	Equivalent Loads			
	DL641	DL642	DL644	DL646
D	1.0	1.0	1.0	1.0
GN	1.0	1.0	1.0	1.0
RN	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DL641	5.0	TBD	11.3
DL642	7.0	TBD	13.4
DL644	11.0	TBD	28.8
DL646	14.0	TBD	35.7

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
DL641	From: D To: Q	t_{PLH} t_{PHL}	0.55 0.53	0.68 0.68	0.81 0.83	0.98 1.00	1.10 1.14
	From: D To: QN	t_{PLH} t_{PHL}	0.69 0.76	0.78 0.86	0.89 0.99	1.02 1.14	1.13 1.27
	From: GN To: Q	t_{PLH} t_{PHL}	0.63 0.69	0.75 0.84	0.89 1.00	1.05 1.16	1.17 1.29
	From: GN To: QN	t_{PLH} t_{PHL}	0.86 0.82	0.95 0.92	1.06 1.06	1.20 1.22	1.30 1.35
	From: RN To: Q	t_{PLH} t_{PHL}	0.55 0.42	0.69 0.56	0.84 0.70	0.99 0.86	1.11 0.99
	From: RN To: QN	t_{PLH} t_{PHL}	0.58 0.78	0.66 0.89	0.77 1.01	0.91 1.17	1.02 1.29
	Number of Equivalent Loads		**1**	**8**	**15**	**22**	**30 (max)**
DL642	From: D To: Q	t_{PLH} t_{PHL}	0.56 0.55	0.71 0.75	0.84 0.88	0.96 1.00	1.09 1.12
	From: D To: QN	t_{PLH} t_{PHL}	0.80 0.85	0.89 0.98	0.98 1.08	1.07 1.18	1.18 1.29
	From: GN To: Q	t_{PLH} t_{PHL}	0.65 0.71	0.81 0.90	0.92 1.03	1.04 1.15	1.18 1.27
	From: GN To: QN	t_{PLH} t_{PHL}	0.97 0.93	1.05 1.07	1.15 1.17	1.24 1.26	1.35 1.36
	From: RN To: Q	t_{PLH} t_{PHL}	0.59 0.41	0.76 0.59	0.88 0.72	0.99 0.83	1.10 0.95
	From: RN To: QN	t_{PLH} t_{PHL}	0.65 0.86	0.74 1.00	0.83 1.11	0.93 1.21	1.04 1.31

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	Number of Equivalent Loads		1	14	28	42	56 (max)
DL644	From: D To: Q	t_{PLH} t_{PHL}	0.88 0.79	1.00 0.89	1.10 1.00	1.18 1.11	1.25 1.21
	From: D To: QN	t_{PLH} t_{PHL}	0.93 1.02	0.98 1.15	1.06 1.25	1.17 1.34	1.29 1.42
	From: GN To: Q	t_{PLH} t_{PHL}	0.97 0.97	1.09 1.12	1.18 1.21	1.26 1.29	1.34 1.36
	From: GN To: QN	t_{PLH} t_{PHL}	1.11 1.16	1.17 1.24	1.26 1.35	1.36 1.45	1.47 1.56
	From: RN To: Q	t_{PLH} t_{PHL}	0.76 0.57	0.85 0.71	0.94 0.82	1.04 0.92	1.14 1.02
	From: RN To: QN	t_{PLH} t_{PHL}	0.72 0.91	0.79 1.03	0.89 1.14	0.99 1.24	1.11 1.34
	Number of Equivalent Loads		**1**	**14**	**28**	**42**	**56 (max)**
DL646	From: D To: Q	t_{PLH} t_{PHL}	0.92 0.77	1.00 0.89	1.06 0.98	1.11 1.05	1.16 1.12
	From: D To: QN	t_{PLH} t_{PHL}	1.00 1.14	1.07 1.22	1.13 1.28	1.19 1.35	1.24 1.42
	From: GN To: Q	t_{PLH} t_{PHL}	1.04 0.99	1.11 1.10	1.17 1.18	1.21 1.24	1.24 1.30
	From: GN To: QN	t_{PLH} t_{PHL}	1.19 1.25	1.27 1.33	1.32 1.39	1.37 1.45	1.42 1.51
	From: RN To: Q	t_{PLH} t_{PHL}	0.79 0.60	0.87 0.70	0.94 0.78	1.00 0.85	1.05 0.93
	From: RN To: QN	t_{PLH} t_{PHL}	0.82 1.03	0.86 1.10	0.92 1.17	0.98 1.23	1.05 1.29

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DL641	DL642	DL644	DL646
Min GN Width	Low	t_w	0.57	0.68	0.65	0.65
Min RN Width	Low	t_w	0.45	0.53	0.51	0.51
Min D Setup		t_{su}	0.57	0.68	0.47	0.47
Min D Hold		t_h	0.14	0.14	0.15	0.15
Min RN Setup		t_{su}	0.38	0.42	0.36	0.36
Min RN Hold		t_h	0.24	0.24	0.29	0.29

Logic Schematic