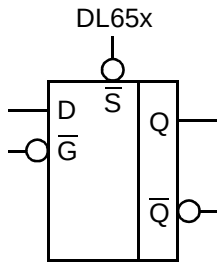
AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

DL65x is a family of transparent, buffered D latches with active low gate transparency. SET is active low.

Logic Symbol



Truth Table

SN	GN	D	Q	QN
L	X	X	H	L
H	H	X	NC	NC
H	L	L	L	H
H	L	H	H	L

NC = No Change

HDL Syntax

Verilog ..... DL65x *inst_name* (Q, QN, D, GN, SN);

VHDL..... *inst_name*: DL65x port map (Q, QN, D, GN, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DL651	DL652	DL654	DL656
D	1.0	1.0	1.0	1.0
GN	1.0	1.0	1.0	1.0
SN	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DL651	6.0	TBD	12.6
DL652	7.0	TBD	15.7
DL654	10.0	TBD	27.2
DL656	12.0	TBD	33.9

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
DL651	From: D To: Q	t_{PLH} t_{PHL}	0.68 0.83	0.75 0.91	0.86 1.04	1.01 1.20	1.13 1.33
	From: D To: QN	t_{PLH} t_{PHL}	0.74 0.60	0.86 0.72	0.98 0.86	1.12 1.02	1.23 1.13
	From: GN To: Q	t_{PLH} t_{PHL}	0.79 1.02	0.87 1.14	0.98 1.25	1.12 1.38	1.23 1.47
	From: GN To: QN	t_{PLH} t_{PHL}	0.88 0.71	0.98 0.82	1.11 0.96	1.28 1.12	1.42 1.24
	From: SN To: Q	t_{PLH} t_{PHL}	0.44 0.53	0.54 0.63	0.65 0.76	0.79 0.91	0.90 1.02
	From: SN To: QN	t_{PLH} t_{PHL}	0.41 0.36	0.52 0.50	0.65 0.64	0.81 0.80	0.93 0.91
	Number of Equivalent Loads		**1**	**8**	**15**	**22**	**30 (max)**
DL652	From: D To: Q	t_{PLH} t_{PHL}	0.75 0.94	0.85 1.06	0.94 1.16	1.03 1.25	1.14 1.36
	From: D To: QN	t_{PLH} t_{PHL}	0.76 0.59	0.89 0.75	1.00 0.87	1.11 0.97	1.22 1.08
	From: GN To: Q	t_{PLH} t_{PHL}	0.87 1.16	0.97 1.26	1.06 1.35	1.14 1.43	1.23 1.52
	From: GN To: QN	t_{PLH} t_{PHL}	0.93 0.72	1.06 0.88	1.17 1.00	1.27 1.11	1.39 1.22
	From: SN To: Q	t_{PLH} t_{PHL}	0.54 0.64	0.61 0.75	0.71 0.85	0.81 0.96	0.94 1.07
	From: SN To: QN	t_{PLH} t_{PHL}	0.44 0.36	0.57 0.53	0.68 0.65	0.79 0.76	0.91 0.87

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	Number of Equivalent Loads		1	14	28	42	56 (max)
DL654	From: D To: Q	t_{PLH} t_{PHL}	0.74 0.90	0.83 1.00	0.93 1.12	1.03 1.24	1.14 1.36
	From: D To: QN	t_{PLH} t_{PHL}	1.08 0.89	1.14 1.01	1.22 1.11	1.32 1.18	1.44 1.26
	From: GN To: Q	t_{PLH} t_{PHL}	0.85 1.08	0.95 1.21	1.05 1.33	1.13 1.44	1.21 1.54
	From: GN To: QN	t_{PLH} t_{PHL}	1.23 1.00	1.30 1.07	1.40 1.17	1.50 1.28	1.61 1.41
	From: SN To: Q	t_{PLH} t_{PHL}	0.50 0.59	0.60 0.75	0.70 0.87	0.80 0.96	0.89 1.05
	From: SN To: QN	t_{PLH} t_{PHL}	0.73 0.65	0.83 0.79	0.93 0.89	1.03 0.97	1.13 1.05
	Number of Equivalent Loads		**1**	**21**	**42**	**62**	**83 (max)**
DL656	From: D To: Q	t_{PLH} t_{PHL}	0.78 0.98	0.88 1.08	0.97 1.19	1.05 1.29	1.14 1.40
	From: D To: QN	t_{PLH} t_{PHL}	1.17 0.99	1.28 1.10	1.35 1.19	1.41 1.29	1.47 1.39
	From: GN To: Q	t_{PLH} t_{PHL}	0.87 1.16	0.96 1.30	1.06 1.40	1.15 1.48	1.25 1.57
	From: GN To: QN	t_{PLH} t_{PHL}	1.35 1.09	1.45 1.22	1.53 1.32	1.59 1.39	1.64 1.47
	From: SN To: Q	t_{PLH} t_{PHL}	0.51 0.62	0.63 0.79	0.73 0.91	0.82 1.00	0.91 1.09
	From: SN To: QN	t_{PLH} t_{PHL}	0.88 0.76	0.95 0.88	1.02 0.98	1.11 1.07	1.22 1.15

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DL651	DL652	DL654	DL656
Min GN Width	Low	t_w	0.74	0.78	0.74	0.74
Min SN Width	Low	t_w	0.45	0.49	0.44	0.44
Min D Setup		t_{su}	0.55	0.59	0.55	0.55
Min D Hold		t_h	0.14	0.14	0.14	0.14
Min SN Setup		t_{su}	0.26	0.30	0.26	0.26
Min SN Hold		t_h	0.41	0.41	0.41	0.41

Logic Schematic