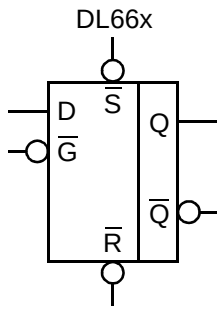
AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

DL66x is a family of transparent, buffered D latches with active low gate transparency. RESET and SET are active low.

Logic Symbol



Truth Table

SN	RN	D	GN	Q	QN
L	L	X	X	IL	IL
L	H	X	X	H	L
H	L	X	X	L	H
H	H	X	H	NC	NC
H	H	L	L	L	H
H	H	H	L	H	L

IL = Illegal NC = No Change

HDL Syntax

Verilog ..... DL66x *inst_name* (Q, QN, D, GN, RN, SN);

VHDL..... *inst_name*: DL66x port map (Q, QN, D, GN, RN, SN);

Pin Loading

Pin Name	Equivalent Loads			
	DL661	DL662	DL664	DL666
D	1.0	1.0	1.0	1.0
GN	1.0	1.0	1.0	1.0
SN	1.0	1.0	2.1	2.1
RN	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
DL661	7.0	TBD	13.4
DL662	8.0	TBD	16.6
DL664	13.0	TBD	34.0
DL666	15.0	TBD	40.5

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
DL661	From: D To: Q	t_{PLH} t_{PHL}	0.81 0.86	0.88 0.96	0.99 1.08	1.13 1.22	1.26 1.34
	From: D To: QN	t_{PLH} t_{PHL}	0.76 0.72	0.86 0.85	0.99 0.98	1.14 1.14	1.25 1.25
	From: GN To: Q	t_{PLH} t_{PHL}	0.89 1.04	0.97 1.12	1.08 1.24	1.22 1.39	1.33 1.53
	From: GN To: QN	t_{PLH} t_{PHL}	0.93 0.80	1.02 0.93	1.15 1.07	1.30 1.22	1.43 1.33
	From: SN To: Q	t_{PLH} t_{PHL}	0.43 0.51	0.52 0.62	0.63 0.74	0.78 0.89	0.89 1.01
	From: SN To: QN	t_{PLH} t_{PHL}	0.40 0.35	0.52 0.49	0.65 0.63	0.79 0.78	0.90 0.90
	From: R To: Q	t_{PLH} t_{PHL}	0.83 0.78	0.91 0.89	1.02 1.01	1.16 1.15	1.27 1.25
	From: RN To: QN	t_{PLH} t_{PHL}	0.67 0.74	0.78 0.87	0.90 1.01	1.05 1.16	1.16 1.27
	Number of Equivalent Loads		**1**	**8**	**15**	**22**	**30 (max)**
DL662	From: D To: Q	t_{PLH} t_{PHL}	0.88 0.98	0.99 1.09	1.08 1.19	1.16 1.29	1.25 1.39
	From: D To: QN	t_{PLH} t_{PHL}	0.79 0.74	0.93 0.89	1.03 1.00	1.13 1.10	1.23 1.21
	From: GN To: Q	t_{PLH} t_{PHL}	0.96 1.14	1.05 1.25	1.15 1.36	1.24 1.46	1.35 1.57
	From: GN To: QN	t_{PLH} t_{PHL}	0.94 0.81	1.08 0.95	1.18 1.07	1.28 1.18	1.38 1.29
	From: SN To: Q	t_{PLH} t_{PHL}	0.52 0.61	0.61 0.74	0.70 0.85	0.79 0.94	0.90 1.05
	From: SN To: QN	t_{PLH} t_{PHL}	0.41 0.35	0.54 0.52	0.66 0.64	0.77 0.74	0.89 0.85
	From: RN To: Q	t_{PLH} t_{PHL}	0.91 0.87	1.00 0.99	1.10 1.10	1.19 1.21	1.29 1.32
	From: RN To: QN	t_{PLH} t_{PHL}	0.70 0.75	0.84 0.92	0.95 1.03	1.05 1.13	1.15 1.23

AMI5HG 0.5 micron CMOS Gate Array

	Number of Equivalent Loads		1	14	28	42	56 (max)
DL664	From: D To: Q	t_{PLH} t_{PHL}	0.81 0.87	0.88 1.02	0.98 1.13	1.09 1.22	1.21 1.30
	From: D To: QN	t_{PLH} t_{PHL}	1.01 1.00	1.08 1.11	1.17 1.20	1.27 1.29	1.38 1.37
	From: GN To: Q	t_{PLH} t_{PHL}	0.93 1.04	1.03 1.20	1.11 1.31	1.19 1.39	1.27 1.46
	From: GN To: QN	t_{PLH} t_{PHL}	1.21 1.10	1.25 1.19	1.33 1.28	1.44 1.38	1.58 1.47
	From: SN To: Q	t_{PLH} t_{PHL}	0.42 0.51	0.53 0.62	0.63 0.74	0.72 0.85	0.81 0.96
	From: SN To: QN	t_{PLH} t_{PHL}	0.67 0.60	0.72 0.68	0.81 0.78	0.92 0.89	1.03 1.01
	From: RN To: Q	t_{PLH} t_{PHL}	0.69 0.64	0.77 0.79	0.86 0.89	0.97 0.99	1.09 1.10
	From: RN To: QN	t_{PLH} t_{PHL}	0.85 0.87	0.91 0.98	0.98 1.07	1.07 1.15	1.18 1.22
	Number of Equivalent Loads		**1**	**21**	**42**	**62**	**83 (max)**
DL666	From: D To: Q	t_{PLH} t_{PHL}	0.87 0.89	0.96 1.03	1.05 1.15	1.14 1.26	1.24 1.38
	From: D To: QN	t_{PLH} t_{PHL}	1.12 1.08	1.24 1.20	1.32 1.29	1.38 1.38	1.43 1.45
	From: GN To: Q	t_{PLH} t_{PHL}	0.97 1.07	1.06 1.23	1.14 1.35	1.22 1.44	1.31 1.53
	From: GN To: QN	t_{PLH} t_{PHL}	1.30 1.17	1.35 1.31	1.43 1.41	1.51 1.49	1.61 1.57
	From: SN To: Q	t_{PLH} t_{PHL}	0.48 0.59	0.58 0.72	0.66 0.79	0.76 0.87	0.86 1.00
	From: SN To: QN	t_{PLH} t_{PHL}	0.76 0.68	0.84 0.79	0.93 0.89	1.03 0.98	1.14 1.08
	From: RN To: Q	t_{PLH} t_{PHL}	0.72 0.72	0.81 0.85	0.91 0.95	1.01 1.04	1.12 1.13
	From: RN To: QN	t_{PLH} t_{PHL}	0.90 0.95	1.01 1.08	1.09 1.17	1.16 1.25	1.23 1.33

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Timing Constraints

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			DL661	DL662	DL664	DL666
Min GN Width	Low	t_w	0.76	0.80	0.73	0.73
Min RN Width	Low	t_w	0.52	0.56	0.34	0.34
Min SN Width	Low	t_w	0.53	0.58	0.43	0.43
Min D Setup		t_{su}	0.59	0.63	0.55	0.55
Min D Hold		t_h	0.14	0.14	0.14	0.14
Min SN Setup		t_{su}	0.25	0.29	0.21	0.21
Min SN Hold		t_h	0.46	0.46	0.43	0.43
Min RN Setup		t_{su}	0.54	0.57	0.35	0.35
Min RN Hold		t_h	0.24	0.24	0.31	0.31

Logic Schematic