DLIS-2K XTREMEPIX

Ultra-Configurable Monochrome Linear Sensor

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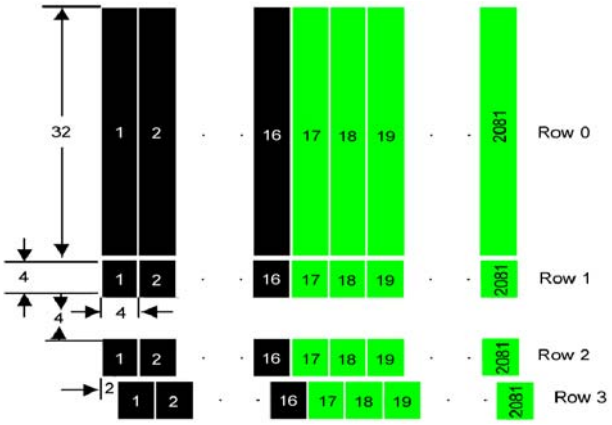
DLIS-2K IMAGER – Quad Line Scan Sensor with 11 bit A/D, High Dynamic Range (HDR), and Correlated Multi-Sampling (CMS) for Enhanced Sensitivity is designed for a wide variety of applications, including:

- **Barcode**
- **Machine Vision**
- **Edge Detection**
- **Contact Imaging**
- **Finger Printing**
- **Encoding and Positioning**



Pixel Orientation
Pixel Layout Dimension in microns.
Readout starts at Pixel 1, selected row.

Key Features

- Four Rows: 1 row of tall pixels (4x32 micron) and 3 rows of square pixels (4x4 micron)
- Integrated 11 bit Distributed A/D with parallel 10 bit digital output
- Output speeds to 120 MHz
- Sensitivity ≤ 160 V/lux.s
- Automatic Dynamic Thresholding™ with binary output
- Integrated CDS
- Multiple Readout modes
  - Ambient Light Subtraction
  - High Dynamic Range (HDR)
  - Correlated Multi-Sampling (CMS)
  - Non-Destructive Read mode
  - Binning of different rows
  - 4K pixels – 2 rows of 2K pixels offset 2 microns
  - Readout one to four rows
- Programmable Gain & Offset (2 bit control)
- Onboard Test Mode capabilities, including External Input to A/D
- Tri-State Outputs
- Power Down Mode
- Single Power Supply 3.3 Volts
- Semi-custom options available

Brief Description

The DLIS-2K Linear Image Sensor consists of 4 rows of pixels, each with 2080 optical pixels and 16 dark pixels. Three rows are made up of 4 micron x 4 micron square pixels and the other is an array of rectangular 4 micron wide x 32 micron tall pixels with equivalent sensitivity ≤ 160 V/lux.s by utilizing Correlated Multi-Sampling (CMS). There is a 4 micron space between rows 1 & 2. One to four rows may be selected for readout. Each row has independent control of reset and integration. Additionally the background sample can be selected as the reset value for normal Correlated Double Sampling (CDS) or can be selected to be the ambient light sample with integration time controlled by the user. The sensor is programmable via a 3-wire serial interface and combined with our patented high speed Distributed 8 to 11 bit Analog to Digital Converter (D/AD™), XtremePIX®, and Active Column Sensor™ (ACS®) technologies to enable a powerful imaging combination for the most demanding applications.

Electro-Optical Characteristics

Unless otherwise specified: $T_{Ambient}$ = 25°C, DVDD_I/O = DVDD = AVDD = 3.3 volts,, CLK = 7.5MHz @ 50% duty cycle, LOAD = 1gate, Color temperature = 3000K

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Voltage, Analog	AVDD		3.0	3.3	3.6	V
Supply Voltage, Digital	DVDD		3.0	3.3	3.6	V
Supply Voltage, I/O Bias	DVDD_IO		3.0	3.3	3.6	V
Supply Current, Analog	I_A			24.6		mA
Supply Current, Digital [1]	I_D			30.3		mA
Power Dissipation	P_W	Normal mode		0.18		W
Power Dissipation	P_{WS}	Power-down mode		TBD		mW
Logic Input, High	V_{IH}		Vdd -0.7			V
Logic Input, Low	V_{IL}				0.8	V
Frequency, Master Clock	F_{CLK}		0.1	7.5	120	MHz
Dark Current(equivalent)	e_n			2.8		mV/S
Dynamic Range [2]	DR	Single read		53.2		dB
Average Dark Signal [3]	ADS			0.22		%FS
Fixed Pattern Noise [4]	FPN			0.31		%FS
Linearity, uncorrected [5]	L			0.24		%FS
Sensitivity (equivalent) of 4x32um pixels	Sen			25.5(1x sampling) 50.0(2x sampling) 102.0 (4x sampling)		V/lux.s
Sensitivity (equivalent) of 4x4um pixels	Sen			20(1x sampling) 40(2x sampling) 80 (4x sampling)		V/lux.s
Full Well Capacity	FW	High as possible		18 k (4x32 um pixel) 14 k (4x4 um pixel)		e
Quantum Efficiency	QE	λ = 600nm High as possible		TBD		%
Image Lag[6]	IL			0,1	3.0	%FS
Spectral Response			350		1100	nm

Table 1. Electro-Optical Specifications

Notes:

1. Lower clock speeds will result in lower DVDD power dissipation.
2. DR ≡ V_{FS} / e_n =D_{FS}/D_n , measured at dark in counts, FS ≡ Full Scale, D_{FS} is FS in digital counts .
3. ADS measured over an integration period of 10ms. Defined as a percentage of Full Scale.
4. Fixed pattern noise measured as V_O – N_O in the dark
5. Pixel average measured from 5% to 70% of saturation, linearity error reported as RMS deviation of response to 'best fit' straight line.
6. Lag can be completely eliminated with adjusted timing; default timing can have up to 3%.

Absolute Maximum and Environmental Specifications

Table 2. Absolute Maximum Specifications

Supply voltage range, V_{DD}[1]	0 V to 5.0 V
Digital input current range, I_{IN}	–16 mA to 16 mA
Digital output current range, I_{OUT}	–16 mA to 16 mA

† Exceeding the ranges specified under "absolute maximum ratings" can damage the device. The values given are for stress ratings only. Operation of the device at conditions other than those indicated above, is not implied. Exposing the device to absolute maximum rated conditions for extended periods may affect device reliability and performance.

Notes:

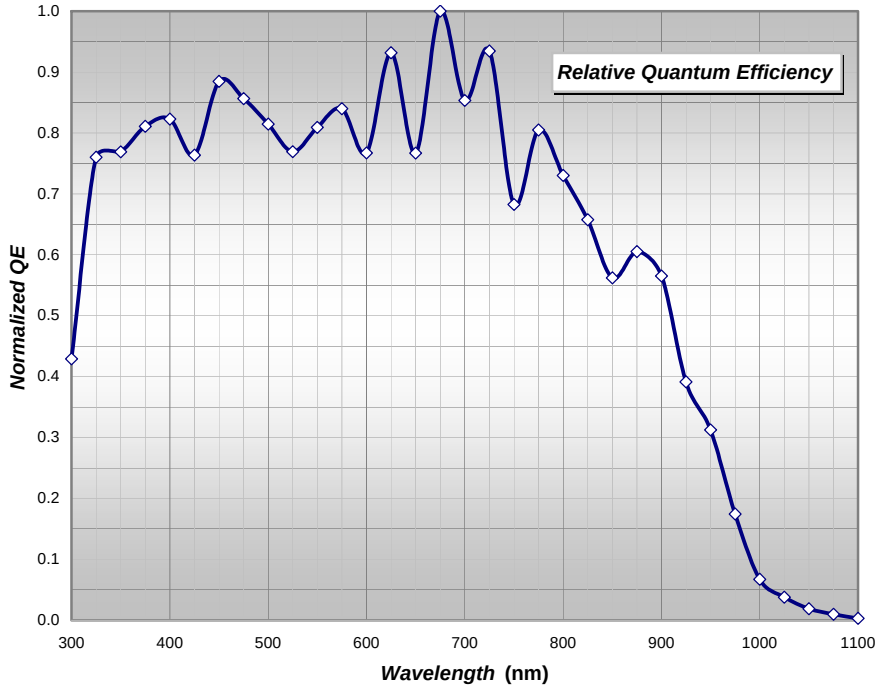
1. Voltage values are with respect to the device GND terminal.

Environment Specifications

Operating case temperature range, T_C (see Note 2)	0°C to 70°C
Operating free-air temperature range, T_A	0°C to 50°C
Storage temperature range	–20°C to 85°C
Humidity range, RH	0-100%, non-condensing
Lead temperature 1.5 mm (0.06 inch) from case for 45 seconds	240°C

Notes:
Case temperature is defined as the surface temperature of the package measured directly over the integrated circuit.

Relative Quantum Efficiency (Estimated)



Note: Representative data not actual from sensor. Data below 350nm not measured, but device is sensitive to 200nm. The QE peaks at 675nm. Shown for un-encapsulated device.

DLIS-2K Device Architecture and Operation

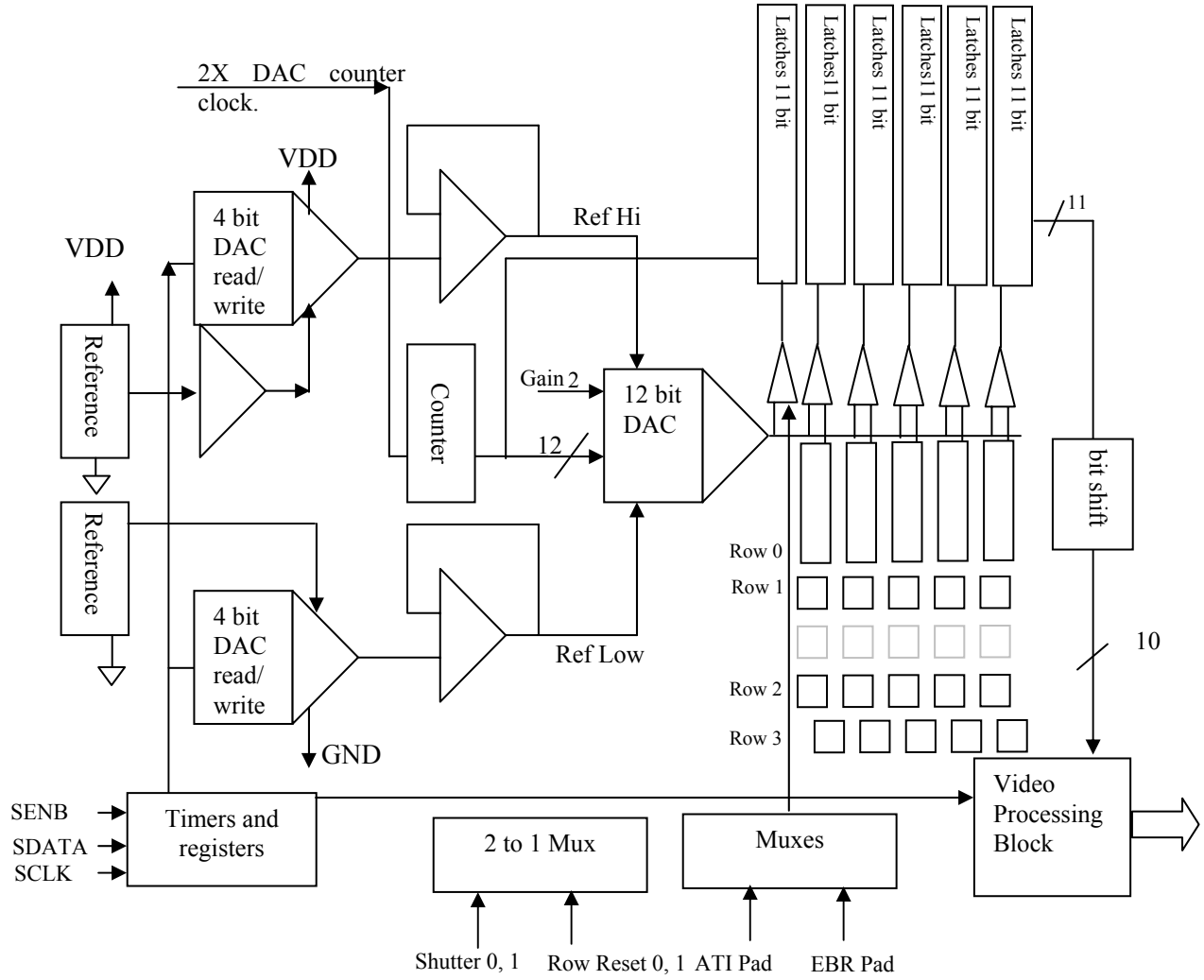


Figure #1**: Top level block diagram**

Overview:

A simplified functional block diagram of the DLIS-2K imager is shown in Fig. 1. The device consists of an imaging core, timing engine, mode select block, video processing engine, and a serial interface for user programming & setup of the device.

Imaging Core

The Imaging core consists of a pixel array configured: 4 rows by 2096 columns (16 dark pixels, 2080 active pixels). Each column of pixels is processed by our patented ACS® technology (described further in this section). The pixel array is followed by an on-chip CDS circuit that is used to subtract out a background signal. This background signal is typically sampled and stored as the value of the pixel after it has been reset and prior to integration of light. Then once the pixel has integrated and sampled again, the corresponding background sample is subtracted and the resultant video is output.

This sensor allows the user to select if the background sample is the normal reset value or the user can allow the sensor to integrate for some period of time after reset and capture an 'ambient light sample' as the background sample. This is very useful for applications where an artificial light source such as an LED or laser is used to illuminate the target. For example, if the laser pulse is 1 ms the user can first sample a 1ms ambient background without the laser and then again for 1ms with the laser. The on chip circuit then automatically subtracts the two outputting only the desired laser signal. The Binary Counter and Digital Latches, that follow the CDS form integral parts of the Distributed Analog-to-Digital Converter or D/AD™ that enable the XtremePIX™ architecture (described further in this section).

The Binary Counter generates up to a 12-bit count that is used by the DAC for the D/AD™ for converting the sampled raw analog video and raw analog background up to 11-bit raw digital video and 11-bit raw digital background respectively, using the DAC Ramp as the analog reference. The Binary Counter is equipped with a Preload feature to initialize the start count. The user may also utilize an external ramp via RAMP input pin, and select the appropriate programming features. An external differential DAC (of at least 11-bit precision) should be used to generate the Ramp input into the D/AD™ via a precision amplifier with appropriate filter to cancel out any external noise.

The DATA_VALID signals specifies the period of active pixel data Data-synched Output clock called PIX_CLK is provided for further external video processing.

Active Column Sensor™/ ACS®

The Panavision Imaging's -exclusive Active Column Sensor™ technology (ACS®) provides video signals that are inherently free of fixed pattern noise (FPN) caused by gain and offset of pixel amplifiers. Rather than using an independent, open loop source follower amplifier per pixel like APS imagers do, the ACS® technique uses a single, closed loop unity gain amplifier (UGA) that is shared among all of the pixels in a column. Thus, each pixel has a virtual closed-loop amplifier, that is, each pixel in a column behaves as if it has its own closed-loop UGA but having identically the same gain and offset. Since all of the columns employ closed-loop UGAs, the gain uniformity from column to column is also exceedingly high. The correlated double-sampling circuit that follows each UGA removes any UGA offset. In the DLIS-2K/4K devices the ACS® amplifier was modified into a comparator and traditional sample-and-hold capacitors were eliminated in order to achieve true Correlated Double-Sampling (CDS) and true Correlated Multi-Sampling (CMS). For more details of the ACS® technology see references [1- 3].

XtremePIX™ Sensor Technology

The XtremePIX™ sensor technology is a revolution in image sensor architecture, enabling CCD image quality with the benefits of CMOS: excellent image quality, high sensitivity for low-light imaging, low power, highly integrated, small form factor, and low cost. The XtremePIX™ sensor technology is the next generation of ACS® and enables true Correlated Double Sampling (CDS), not pseudo CDS as provided by most APS designs. Additionally, it allows our Distributed 11-bit Analog-to-Digital Converter or D/AD™, in-pixel binning mode for increased sensitivity for low-light / night-time video capture and enables High Dynamic Range (HDR) capture by the camera.

Timing Engine

The onboard timing engine provides all necessary signals to drive the imaging core, on board DAC's (ramp & references), and video processing. This simplifies the user interface, and reduces the I/O count required to operate the device. The user may also alter the default timing edges via programmable registers & serial interface (detailed in Device Operation & Timing, and programming section) for special applications requiring alternative operational characteristics.

Video Processing Engine & Mode Select Block

The on board video processing engine & mode select block provides required processing of raw video & video configuration modes as selected by the user. This simplifies the user interface, and reduces off chip resources to operate the device in the any of the available video modes as required by the user. The user may select video processing options and video modes via programmable registers & serial interface. Further details are described in Device Operation & Timing, and programming section.

Serial Programming interface

The device is programmable via a simple 3 wire serial interface. The use can create custom setups that include changing video modes, test modes, on-chip data path characterizing, and modify imager core timing. The result is a compact high performance imaging system, rivaling that of systems costing much more. Further details are described in Device Operation & Timing, and programming section.

Device Operation and Timing:

Power Up

When power is applied to the digital DVDD the timing controller must initiate the default settings and then bring up the internal power down signals. All power down signals are active low, meaning when driven low the circuit is powered off. The Power Down Pad has an internal pull up so the sensor will normally be powered on.

Imager Core Operation

The DLIS-2K is configured for ease of use and provide an easy to use interface to provide wide flexibility to be adaptable to many applications. There are four rows of 2080 pixels that the user can have direct control of integration, sample and reset. One row is 4 X 32 micron pixels (a.k.a. row 0) and the other rows are 4 X 4 micron pixels (a.k.a. row 1, 2, 3). The decoded outputs from the pads (Shutter 0,1 and Row Reset 0,1) are combined with the internal registers except for Row 3 pad decode.

The user can select to output the first row (rectangular pixels), or the three other rows (square pixels). Note that there is only one readout structure that is multiplexed between the four available (out of 5) rows, therefore the second and other rows are readout after the first selected row is readout.

The decoded outputs from the pads (Shutter 0, 1 and Row Reset 0, 1) are combined with the internal registers except for Row 3 pad decode as shown below.

Row selected	Shutter 0	Shutter 1	Reset 0	Reset 1
Row 3	-Programmed via internal registers			
Row 2	0	1	0	1
Row 1	1	0	1	0
Row 0	1	1	1	1
None	0	0	0	0

Figure #2**:**. *Two bit decoder for row selection(Shutter 0,1 to transfer pixel signal to sense node) and reset*

Each column Opamp is configured as a comparator for direct comparison the pixel value to a default setting of a 10 bit DAC generated ramp. . The DAC has a programmable range of 8 to 12 bits. When the DAC output matches the value of the pixel value the comparator will latch the DAC count. This process is done a minimum of twice per readout to sample the background and the video value. The difference is the signal value. The pixel background (reset level) and the video sample can be re-sampled to reduce noise or add gain. Additionally an offset (Preload) can be added in terms of A/D counts and the default value of the offset is 128 counts.

The first sample is called the background sample using the Row Reset 0, 1 signal and the second sample is called the video sample using the Shutter 0, 1. The first sample occurs just after the pixel sample (a.k.a. sense node) node is reset via either Reset 0 for the 4 X 32 micron pixel or Reset 1 for the 4 X 4 micron pixel. The background is digitized according to the DAC ramp resolution setting. The pixel values are sampled after issuing the Select 0 or 1 signal.

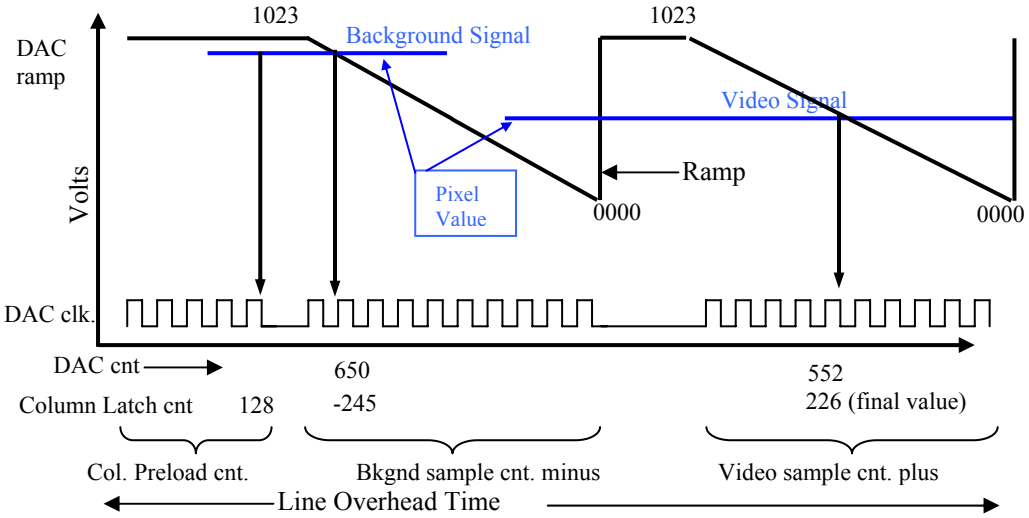


Figure #3**: Video Ramp**

Fig. # 3 shows DAC ramp, background sample and video sample signals for a 10 bit ramp, and corresponding column count (default ramp is 10 bits).

The 2X clock input (MCLK) is used for the BIN_CNT_CLK that drives the binary counter that drives the DAC and the 2X clock is used for the COUNTER_CLK that drives the count to the pixel latches. As the input clock is a 2X of the pixel clock the DAC utilizes the 2X clock as the actual clock rate of the lsb for the DAC counter. In this manner the user can select the readout speed as an even divider from MCLK and give flexibility on the timing needed for pixel depth when digitizing and allow for more oversampling. MCLK_DIVIDE is used to generate all other pixel timing edges. The digital designer will determine which clock is used for ADT, and Digital Comparator. The actual 2X clock used for the DAC counter is MCLK.

Full Scale DAC offset control:

User can control DAC full scale offset by two ways.

1) By providing bias to EBR (External black reference) pin.
2) By programming full scale offset register thru serial interface

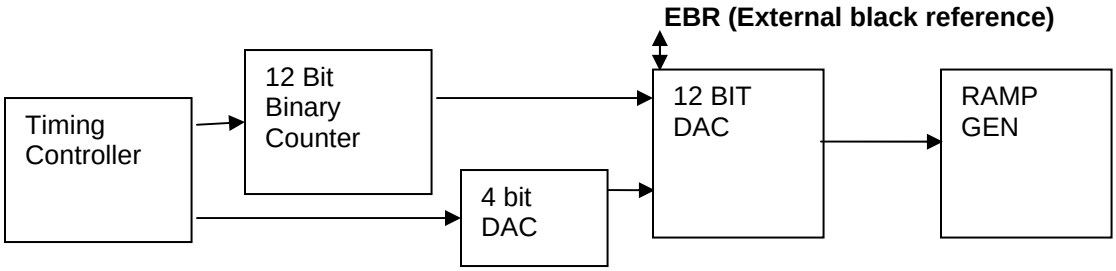


Figure #4: **DAC Full Scale Offset**

The user can control DAC full scale offset by providing bias to EBR pin or by programming full scale offset register. External bias or internal offset register can be selected via a control bit. In default mode DAC full scale offset is controlled by the programmable register

Zero Scale offset control or secondary gain control

The user can control DAC Zero scale offset by two ways:

1) By providing bias to ATI (Analog Test Input) pin.
2) By programming Zero scale offset register thru serial interface

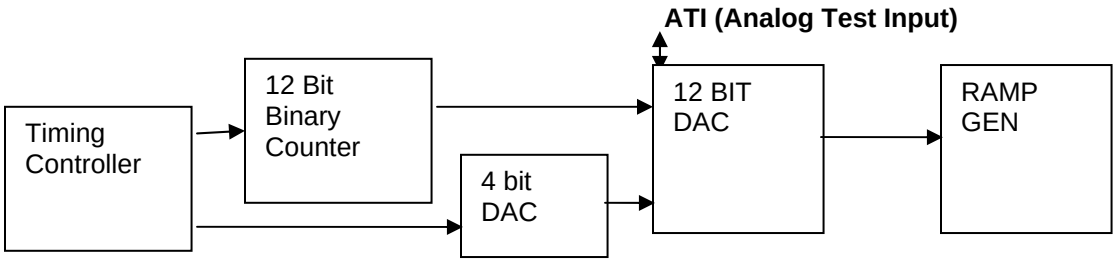


Figure #5: **DAC Zero Scale Offset**

The user can control DAC Zero scale offset by providing bias to ATI pin or by programming Zero scale offset register. Either external bias or internal offset register can be selected via control bits. In default mode DAC Zero scale offset is controlled by the programmable register.

Preload

Every pixel has 11 bit latches associated with it. The DAC counter at the beginning of every line can have a preload to the pixel latches applied. The preload count is set to a default of 128 counts. The preload is effectively an offset being applied to the resulting video value. The preload value is accomplished by the COUNTER_CLK and PLUS_CNT or MINUS_CNT signals being issued. The EXTRA_CLK AND TOGGLE signal it then issued to change from a positive latched value (PLUS_CNT) to a negative latched value (MINUS_CNT) without corrupting held values in the latches.

Background Sample

The DAC is set to maximum value by the PULL_UP_DAC signal at the same time the BIN_CNT RST signal is issued. Row_Reset0 or Row_Reset1 signal can issue after BIN_CNT_RST for background sample. Row_Reset0 or Row_Reset1 signal reset the sense node at around 2.5V and than this value is digitized according to DAC ramp resolution setting. Background sample is preprogrammed to be before the video sample. When digitizing the background the digitized value is the positive value for the latch and the video sample is considered the negative value for the pixel latch. The net sum of the two values is the correlated double sampling. Hence, the background sample is first and the PLUS_CNT signal is issued to coincide with the background ramp and MINUS_CNT is associated with the video ramp.

In the above Fig. #3, the preload count is 128 and the example value of the background value captured by the latch is 650 The DAC can reset to its maximum count while issuing BIN_CNT_RST and PULL_UP_DAC. PULL_UP_DAC is used to reset the ramp signal back to its maximum value on the Opamp buffer. The background level is typically 2.5Volts analog internally.

This sensor allows the user to select if the background sample is the normal reset value or the user can allow the sensor to integrate for some period of time after reset and capture an 'ambient light sample' as the background sample. This is very useful for applications where an artificial light source such as an LED or laser is used to illuminate the target.

Video Sample

Between the background sample and the video sample an Extra_Clk and Toggle signal must be issued. Any time the value to be digitized needs to change sign, an EXTRA_CLK AND TOGGLE signal needs to be issued. After Shutter 0,1 addressing has issued the DAC begins to decrement again via the PLUS_CNT signal. In the example above the column in the Fig. #4 example above at count 1306 for the lower 10 bits of the 11 bit counter. The count 1306 is the final count as the offset value is added to the video value and the background value is subtracted out. During readout, the user can select the resulting video value to be the upper 10 or lower 10 bits.

Video Output Modes:

Standard or Conventional CDS

User can control exposure time, select and reset row externally thru "Reset" and "Shutter" pins. User can charge pixel senses node to background level by turning on High external "Reset" signal. Once the sense node is charged up to background level the sense FET, which the gate is attached to the sense node is then automatically turned on and connects the sense node to comparator. After "Reset" signal goes low, immediately background ramp will start counting from 1023-count and comparator compares background value with ramp and trigger the counter to store background value. Once background value is sampled and background ramp is done user can transfer photo-diode value onto sense node by turning on High "Shutter" signal. After "Shutter" signal goes low video ramp will start counting from 1023-count and comparator compares video value with video ramp and trigger latches to store the DAC count that is the video value. See figure #6 for timing.

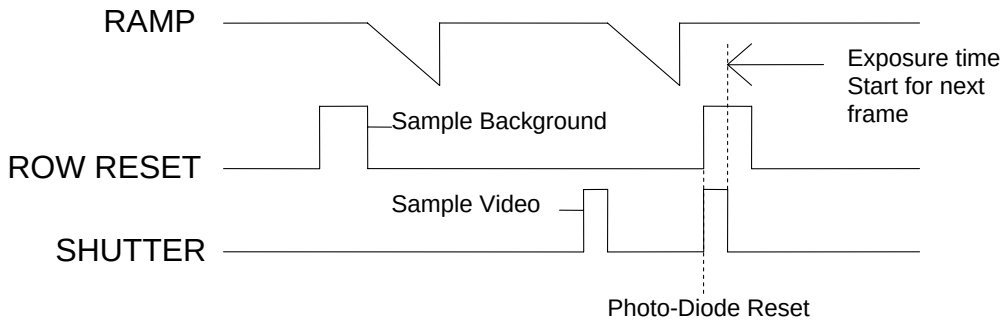


Figure #6: **Standard CDS Sample Timing**

Ambient Light Subtraction (Double Sampling):

In this mode, the user can sample different ambient light levels to get correct offset. First the user has to put imager sensor in this mode thru programming the serial-interface. The user can charge pixel sense node to background level by turning on High external "Reset" signal. Once the sense node is charged up to background level, the 'Shutter" signal is turned on to transfer photo-diode value onto to sense node for ambient light level. After "Shutter" signal goes low immediately background ramp will start counting from 1023-count and comparator compares background value with ambient light to ramp and trigger the latches to store background value with ambient light level.

Once background value with ambient light is sampled, user can turn on "Reset" signal again to charge sense to background level. Once sense charge is charged up to background level, 'Shutter" signal is turned on to transfer photo-diode value with flash into sense node. Once "Shutter" signal goes low video ramp will start counting from 1023-count and comparator compares background value with flashlight to ramp and trigger the latches to store value. User will have selectable feedback based upon the Sync signal selected to be output by the TM pin. See figure #7 for timing.

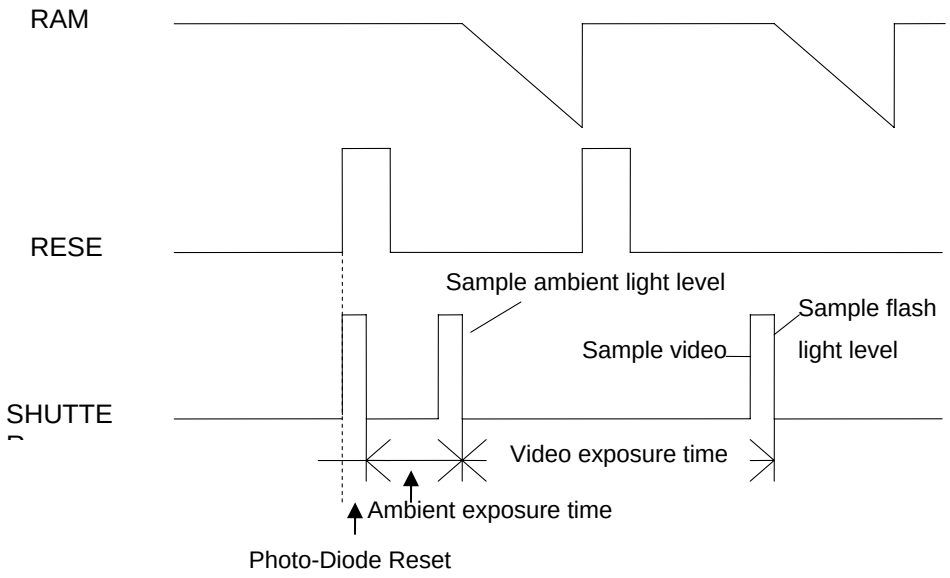


Figure #7: **Double Sample Timing**

Auto Dynamic Thresholding (ADT)

ADT resides in the video processor block and is a form of video signal processing that detects a varying video signal that is superimposed on a non-uniform DC level. Localized signal processing is performed within a window of pixels to determine whether or not the video level is above or below the average of all pixels within the window. This calculated "look ahead moving average" becomes the dynamic threshold. The ADT when enabled calculates either a 4 pixel average or an 8 pixel average. The "average" can either be a calculated average of the previous 4 or 8 pixels or a running weighted average where the last pixel is 50% of the calculated value. The ADT calculates the average on the 10 bits of data only.

Bit Select:

Bit 0: 4-pixel average (figure #8)
Bit 1: 8-pixel average (figure #9)

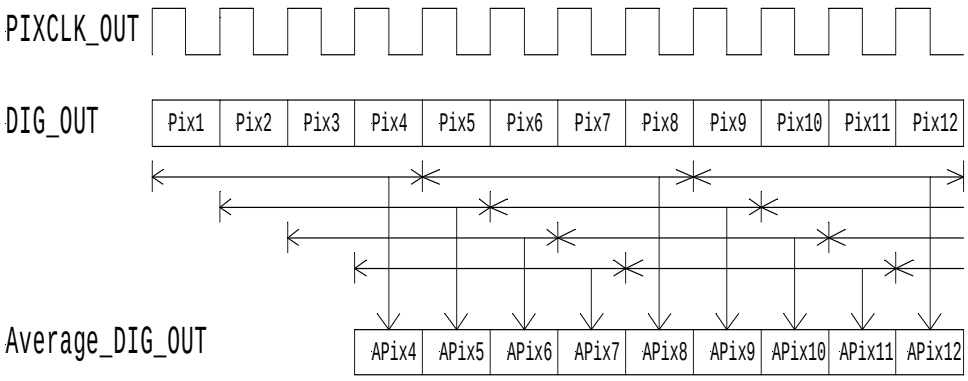


Figure #8: **4 Pixel average**

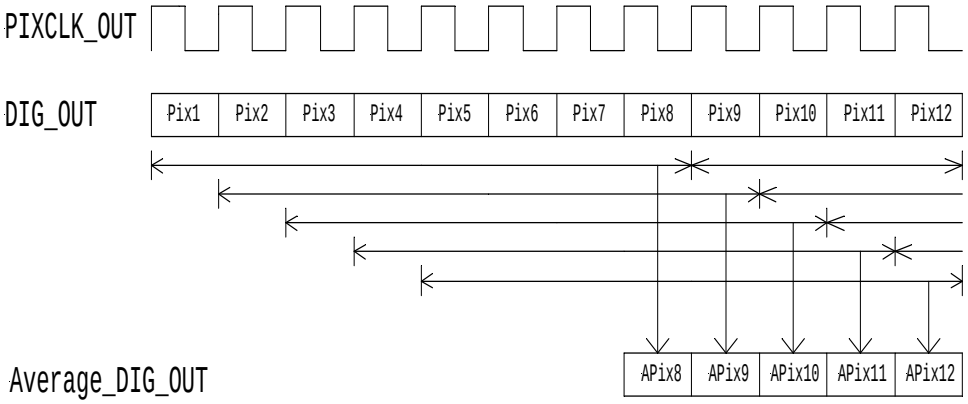


Figure #9: **8 Pixel average**

Weighted Average 4 or 8 Pixel Mode

In this mode the device takes either 4 or 8 pixels and will create a value based on decreasing weights of the previously read pixels as follows:

4 Pixel Mode

NewPixel = (Pixel[t-0] + Pixel[t-1] /2 + Pixel[t-2] /4 + Pixel[t-3] /8) /2

8 Pixel Mode

NewPixel = (Pixel[t-0] + Pixel[t-1] /2 + Pixel[t-2] /4 + Pixel[t-3] /8 +
Pixel[t-4] /16 + Pixel[t-5] /32 + Pixel[t-6] /64 + Pixel[t-7] /128)/2

Digital Comparator

Digital comparator is compare of digital out from the pixels and digital out from ADT Processor and provides result to "BOUT" pad. Here ADT output works as a threshold and user can select 4 or 8 pixel window for threshold value. If digital output from Imager core is higher than threshold value than comparator flags "High" and if digital output from Imager core is lower than threshold value than comparator flags "Low". Use can select different Hysteresis settings for noise immunity. Default Hysteresis setting is +/-32 but can be increased to +/- 256 counts.

The digital comparator compares the previous 4 or 8 pixel average to the current pixel value and compares if the current pixel value is above or below the average plus or minus a hysteresis value.. If the current pixel is above the

average plus a user programmed hysteresis value then a "one" is output. If the pixel value is below the average minus the hysteresis value than a "zero" is output to the BOUT (Binary OUT) pad. This calculated 'average' becomes the digital threshold and can be output to the digital output pads in the upper 10 bits.

For example straight 4 pixel average:
Initial conditions at beginning of line time BOUT = "0" (note: first 4 or 8 pixels are "0")
IF (n-4 + n-3 + n-2 + n-1)/4 + hysteresis > n then = 1
IF (n-4 + n-3 + n-2 + n-1)/4 - hysteresis > n then = 0
IF pixel n not outside hysteresis window then previous value of BOUT is maintained.
.

Mode0 (*default programming*)

Default 10-bit Digital outputs (this also means 10 bit ramp) are connected on DOUT pads. In this mode ADT processor is disabled. In all modes the Start pulse ("STRT") will begin the readout overhead timing without further input from the user. The user can overdrive the Reset 0,1 or Shutter 0,1 signals as they are or'ed with the internal Shutter 0,1 or Reset 0,1 timing registers.

The 2x input Clock signal ("CLK") is a free-running 50% duty-cycle clock. The start pulse ("STRT") goes high before a rising "CLK" edge to commence line initialization sequence followed by turning on external "RESET' and "Shutter" signal high for the black pixel and video pixel readout. The "DATA_VALID" signal goes high when first active pixel has been readout and stays high up to last pixel readout. The initialization always takes 8 clock cycles to complete and followed by 4 to 8 clock wide "RESET" signal and 2 to 8 clock wide "Shutter" signal to read out background and video value from pixel.

Pixel Reset: The pixels are reset while the RESET and Shutter inputs are both held high for at least 4-pixel clock cycle. This way user can charge the photo-diode to background value. Once Shutter signal goes low, user can hold RESET signal high for another 4-pixel clock cycle to get proper background value from sense node.

Pixel Integration: Once Shutter 0 or 1 goes low while RESET is high, the pixels begin to integrate. Integration continues until Shutter signal goes high again.

Readout: Background readout begins on the first rising edge of clock after RESET signal goes low and Video readout begins on the first rising edge of clock after SHUTTER signal goes low

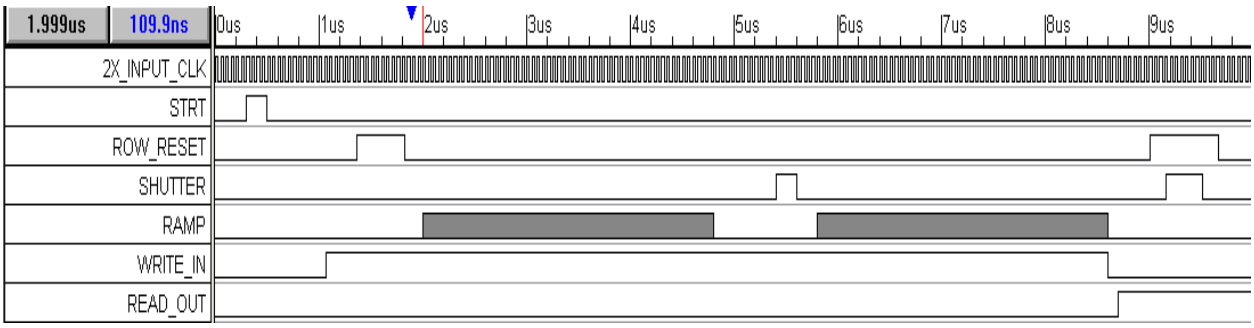


Figure #10: **Line Initialization Timing**

Mode 1

10-bit Digital output on DOUT pads. In this mode ADT processes video on DOUT pins.

In this mode Line initialization timing is same as mode0 but user can enable ADT processor thru serial interface. In this mode digital comparator compares upper 10 bit of digital video to output of ADT processor. Here output of ADT processor is works as a digital threshold. User can get 10-bit Digital output on DOUT pads and digital out of Digital comparator is on "BOUT" pad. User can also select 4 or 8-pixel window for digital threshold value depend on target and application. Use can read threshold value from register thru serial interface. Please see ADT processor description more details. When ADT is enabled ADT should control Line Valid (DATA_VALID) so it is in sync with actual data.

Mode Options

Correlated Multi-Sampling (CMS)

The 10-bit Digital output on DOUT pads and ADT processor is disabled. User can put image sensor in this mode thru serial interface.

The user can oversample the pixel data such that each row is read twice or 4 times by issuing twice or four times ramp in same line time to reduce temporal noise, and/or increase sensitivity and to extend dynamic range. Example files are sent with each demo kit.

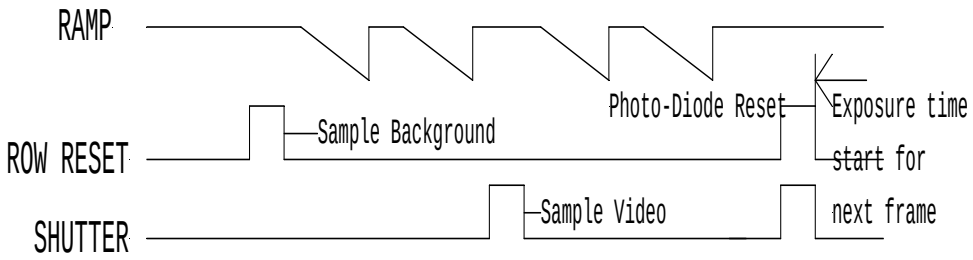


Figure #11: **Correlated Multi-Sampling (CMS) Timing Example**

High Dynamic Range (HDR)

The user can sample the pixel data with short and long exposure time to extend dynamic range. A detailed High Dynamic Range timing sequence for row operation is as follows. The sense node is charged to the background level by turning on "High" the "Row Reset0" signal briefly. Once the sense node is charged up to the background level the sense FET, which the gate is attached to the sense node is then automatically turned on and completes the ACS amplifier. The Background Ramp signal is operated to sample the background level. Shutter0 is operated to transfer the charge on to the sense node from photo-diode and Video Ramp is operated to sample the video level. In this cycle background and video value is stored in storage latch because user is not reading out this value. The previous cycle is repeated for "Row_Reset1" and "Shutter1" signals without issuing "Reset_Latch" signal followed by issuing "READOUT_CLK" and 'READ_OUT" signal. Adding two rows with different exposure times in storage together can extend dynamic rage of the image.

Figure #12: **High Dynamic Range (HDR) with 2x CMS Sample Timing**

Power Standby Mode

The user can put image sensor in this mode thru serial interface. In this mode all internal bias generators, RAMP DAC and digital blocks are disabled. This mode maintains the minimum logic required to preserve the existing set-up. User can hold RESET and SHUTTER signals high to put photo-diode in reset mode. This is different than driving the "PD" pin low which causes the device to go into "Power Down" mode.

Output Bus Control

The user can cause all output pins to be placed in tri-state mode via TM pin. Note: TM in default mode (0) serves as an input (Tri State active high) and drives Data Outputs Tri-State mode. See "Programming Control Register Map" for further details

Programming & Setup

In this section, the timing edge registers, and user programmable registers are defined. Default timing and default register settings are also defined in this section

Serial Communication Interface

Communication of setup and control information to the internal registers of the device is via a 3 wire serial interface. The serial enable pin, SENB, is used to enable the serial interface. Serial data (SDATA) is clocked into or out of the device with the serial clock pin, SCLK. SENB must be high during the entire read or write operation of a register. Asserting SENB to low will terminate the serial frame.

Parameter	Min	Typ	Max	Units
SCLK Frequency			20	MHz
SDATA set-up time	10			nS
SDATA hold time		0		nS

A typical write sequence consists of:

1. Driving the enable line high to initiate communication.
2. Sending a 15-bit address MSB first, followed by a "0" to indicate a write operation.
3. The last 16-bits of serial data will be the write/read data.
4. Sending the 16 bit data value.
5. Driving the enable line low to terminate the cycle.

Please note that the registers are updated 4 MCLK clock cycles after SENB goes low.

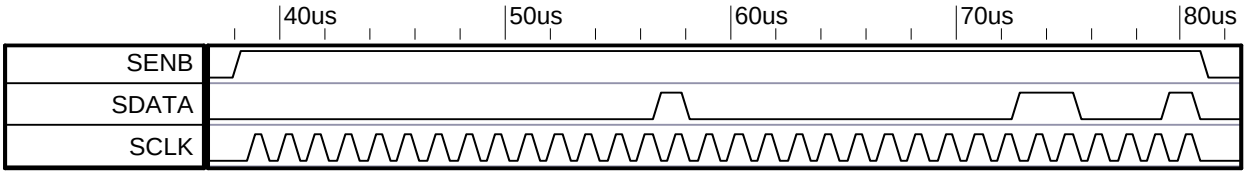


Figure #13: **Write Cycle Timing**

During a write cycle and always during the first 16-bits of input data (15-bit address and 1-bit r/w flag), data is latched into the serial interface on the rising edge of the SCLK signal.

A read operation consists of:

1. Driving the enable line high to initiate communication.
2. Sending a fifteen bit address MSB first, followed by a "1" to indicate a read operation.
3. The last 16-bits of serial data will be the write/read data.
4. Receive the 16-bit data value.
5. Driving the enable line low to terminate the cycle.

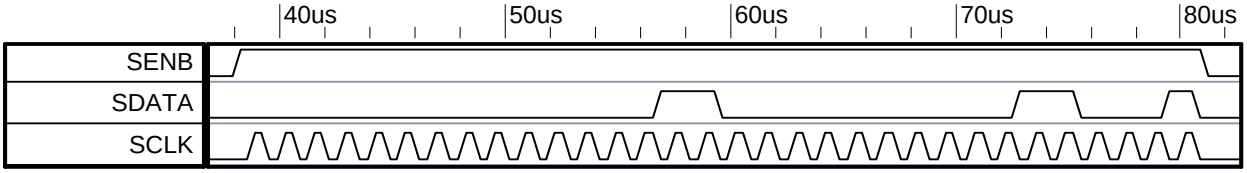


Figure #14: **Read Cycle Timing**

During the Read cycle (last 16-bits of data); new bit data is presented to the user on rising edge of SCLK. Therefore the user should latch the presented data on the falling edge of the SCLK signal.

Default Programmable Internal Timing Signals:

Internal timings are from timing engine to imaging core. All edges have default values. See figures #14 & #16 for default timing waveforms. All defaults enabled upon power up.

Signal Name	Signal	# of Edges	Initial Value	Signal Polarity	EDGES																	
					1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	11th	12th	13th	14th	15th	16th	17th	18th
BIN_CNT_CLK	Clock	18	0		1232	2256	2750	3774	0	0	0	0	0	0	0	0	0	0	0	0	0	0
COUNTER_CLK	Clock	18	0		200	264	1250	2256	2768	3774	0	0	0	0	0	0	0	0	0	0	0	0
BIN_CNT_RST	Prog.	4	0	Act. High	1200	1254	0	0														
PULL_UP_DAC	Prog.	18	0	Act.High	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
AMP_ACTIVATE	Prog.	4	1	Act.Low	3900	4200	0	0														
ZERO_RESET	Prog.	4	0	Act.High	0	0	0	0														
FORCE_RESET	Prog.	4	1	Act.Low	0	0	0	0														
PLUS_CNT	Prog.	10	1	Act.High	800	2768	0	0	0	0	0	0	0	0								
MINUS_CNT	Prog.	10	0	Act.High	1250	2256	0	0	0	0	0	0	0	0								
TOGGLE	Prog.	12	0	Act.High	1098	1110	2518	2530	0	0	0	0	0	0	0	0						
READOUT	Prog.	4	0	Act.High	3790	12032	0	0														
WRITE_IN	Prog.	16	1	Act.High	3786	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
EXTRA_CLK	Prog.	12	0	Act.High	1102	1106	2522	2526	0	0	0	0	0	0	0	0						
PRELOAD	Prog.	2	0	Act.High	200	328																
RESET_LATCH	Prog.	4	1	Act.Low	50	100	0	0														
SHUTTER0	Prog.	8	0	Act.High	2768	2772	3940	4160	0	0	0	0										
SHUTTER1	Prog.	8	0	Act.High	0	0	0	0	0	0	0	0										
SHUTTER2	Prog.	8	0	Act.High	0	0	0	0	0	0	0	0										
SHUTTER3	Prog.	8	0	Act.High	0	0	0	0	0	0	0	0										
ROW_RESET0	Prog.	8	0	Act.High	1250	1254	3920	4180	0	0	0	0										
ROW_RESET1	Prog.	8	0	Act.High	0	0	0	0	0	0	0	0										
ROW_RESET2	Prog.	8	0	Act.High	0	0	0	0	0	0	0	0										
ROW_RESET3	Prog.	8	0	Act.High	0	0	0	0	0	0	0	0										
VALID_A (DATA_VALID)	Prog.	2	0	Act.High	3790	12032																

Figure #15: **Default Timing Edges**

Note: All other register contents not specified in the above table or in the **Programmable Control Register Map** have default values of "0".

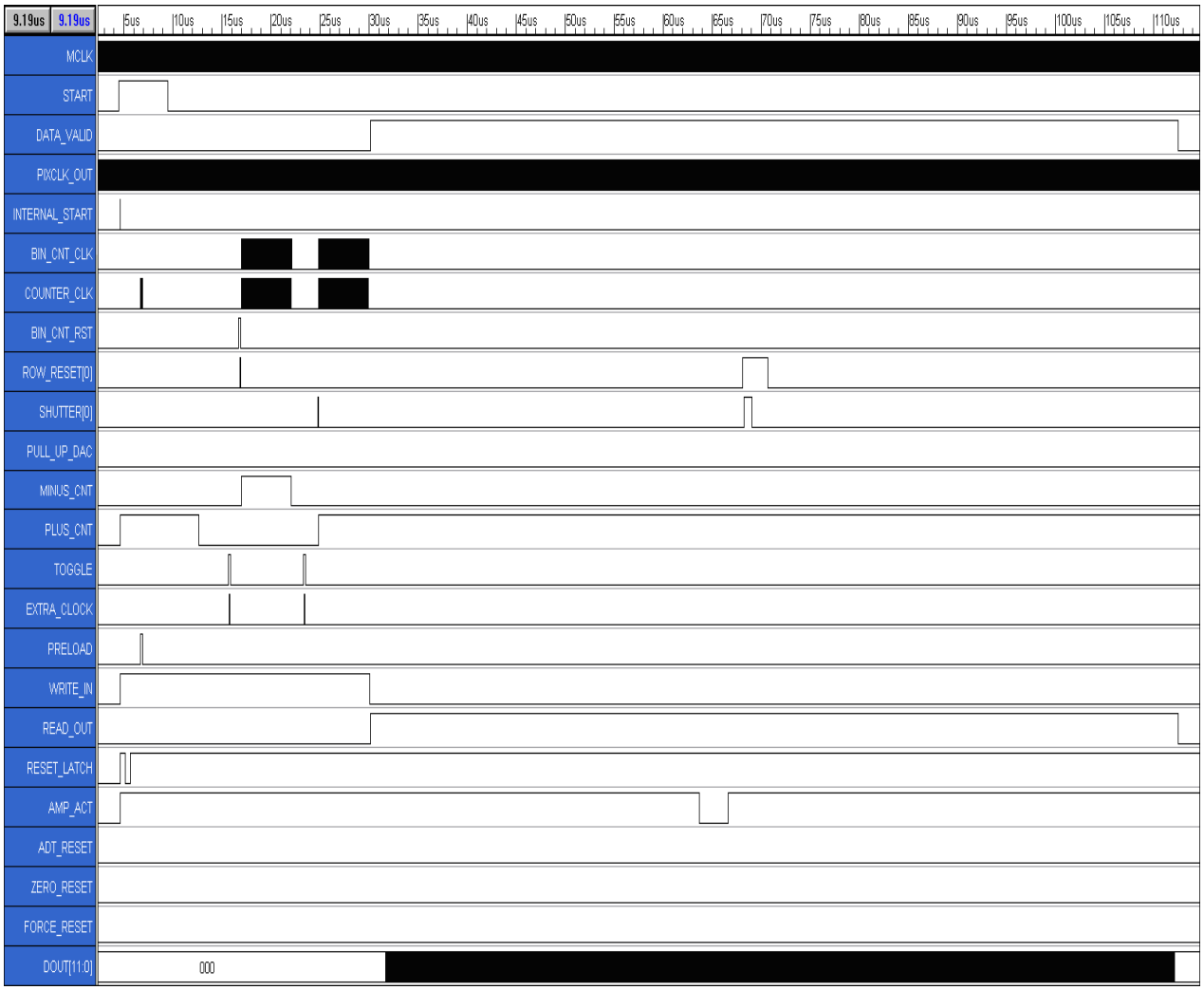


Figure #16: **Default Timing Diagram**

Programmable Control Register Map:

Address	Name	Description/Bits
0x001	START_CON	Two 4-bit timers that control the timing of the internal start pulse after the assertion of the user's external START pin Bits [7:4] = Clock Cycle of falling edge of START Bits [3:0] = Clock Cycle of rising edge of START **Default at Reset = 0x0085**
0x002	PWR_CON	Bit 15 = DAC LOW POWER MODE bit (low enables PD) Bit 14 = BIAS LOW POWER MODE bit (low enables PD) Bits [13:8] = RESERVED Bits [7:4] = DAC_NBIAS Control bits* Bits [3:0] = DAC_PBIAS Control Bits* **Default at Reset = 0xC0F0** * Please contact Panavision Imaging if using values other than default
0x003	DAC_CON	Bit [15] = RESERVED Bits [14:12] = DAC Counter Clock Shift Control 000: 12 bit ramp 001: 11 bit ramp 010: 10 bit ramp **(default)** 011: 9 bit ramp 100: 8 bit ramp 101: RESERVED 110: RESERVED 111:RESERVED Bits [11:8] == VREF High Offset for 12-bit RAMP DAC* Bits [7:4] == VREF Low Offset for 12-bit RAMP DAC* Bits [3:0] == Black Reference VREF Offset* **Default at Reset = 0x298C** * Please contact Panavision Imaging if using values other than default

Address	Name	Description/Bits
0x004	SYS_CON	Bit [15] = VID_OR_THR Select 0: Raw Pixel Data output on DOUT pins (**default**) 1: ADT processed output on DOUT pins Bit [14]= 0: TM pin logic state drives Digital Data Outputs Tri-States **(default)** 1: Digital Outputs are always driven Bit [13] = 0: Enable TM as input **(default)** 1: Enable TM as an output driver Bit [12] = ADT_Enable (**Default = '0' to disable ADT**) Bit [11] = ADT Power Down Mode **(Default ='0')** Bit [10] = RESERVED Bit [9] = Digital Comparator Enable (**Default='0' for disabled**) Bit [8] = Digital Comparator Reset **(Default='0' to release from reset)** Bit [7] = Digital Comparator Power Down **(Default= '0')** Bit [6] = Zero Control (Default ='0' for OUT1 '1' for Out0) Bit [5:4] = Dac Gain for Ramp DAC. (**Default = '00')** Bit [3] = RESERVED Bits [2:0] = Digital Comparator Hysteresis **(Default = '100' for +/-32)** 000: 0 count 001: 4 count 010: 8 count 011: 16 count 100: 32 count **(Default)** 101: 64 count 110: 128 count 111: 256 count **Default at Reset = 0x4004**
0x005	RESERVED	
0x006	RESERVED	

Address	Name	Description/Bits
0x007	OPMODE	Bit [15] = BIN_CNT_MINUS **(Default='1')** for DAC RAMP 1: DAC counts from 4095 > 0 0: DAC counts up from 0 > 4095 Bit [14] = UPPER/LOWER Bit Select **(Default = '0')** 1: Selects bits[12:1] from the imager array 0: Selects bits [11:0] from the imager array Bit [13:12]:= Select the ADT Processor Mode **(Default = '00')** 00: Weighted 4 Pixel Mode 01: Non Weighted 4 Pixel Mode 10: Weighted 8 Pixel Mode 11: Non Weighted 8 Pixel Mode Bit [11] = RESERVED Bits[10:8] = RCLK_DIV: Divide down MCLK for Readout Frequency 000: Divided by 2 **(default)** 001: Divided by 4* 010: Divided by 8* 111: Divide by 1* Bit [7] = RESERVED Bit [6:4] = MCLK_DIV: Divide down MCLK for Timer Stepping 000: Divided by 2 001: Divided by 4 010: Divided by 8 111: Divide by 1 **(default)** Bits [3:2] = RESERVED Bit [1:0] = Mode Setting bits 00: Mode 0 (ADT disabled) 01: Mode 1 (ADT enabled) **Default at Reset = 0x8070** * Please contact Panavision Imaging if using values other than default
0x008	RESERVED	
0x009	RESERVED	

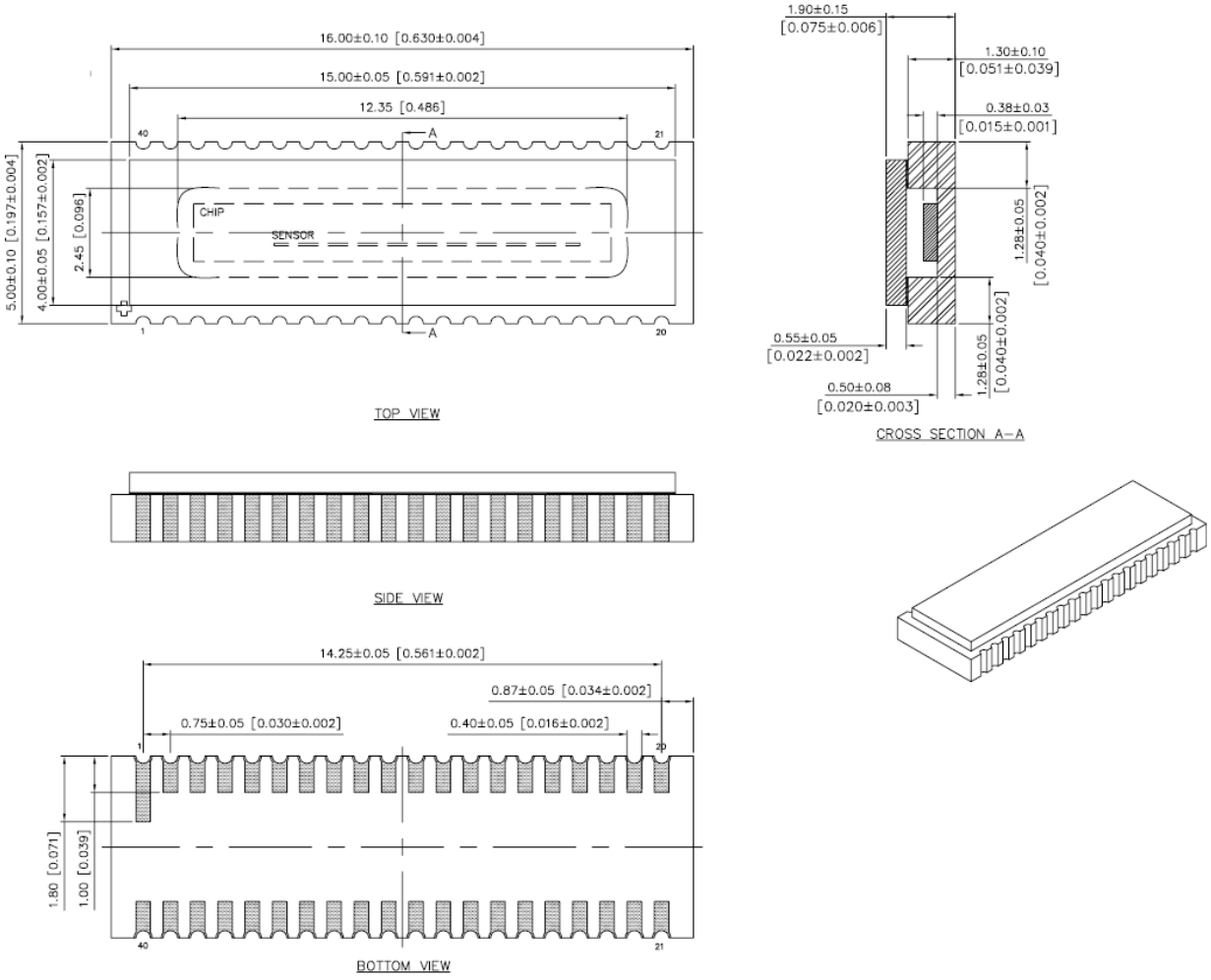
Address	Name	Description/Bits
0x00A	RESERVED	
0x00B	RESERVED	
0X00C	RESERVED	
0x00D	ADT_DISCARD	This 8-bit register is used to holdoff the ADT module until the black pixels have been read out of the pixel array. This register prevents the ADT module from considering the black pixels during the averaging process. Bit [7] = '1' to enable 4 or 8 pixel auto-adjust mode. This holds the ADT core off for proper alignment in both 4 and 8 pixel mode Bits [6:0] = Specify clock cycle when the black pixel read out is complete **Default at Reset = 0x0091**
0x00E	RESERVED	
0x00F	RESERVED	
0x200	SYS_CONB	15-bit register with the following allocations Bit [15] = RAMP_SELECT Bit [14] = SND Bit [13]= LPM Bit [12] = VREF_CNT Bit [11] = RESERVED Bit [10] = RESERVED Bit [9] = RAMPMAXSEL/EBR Bit [8] = RAMPMINSEL/ATI Bits [7:5] = RESERVED Bit [4] = '1' to invert BOUT signal Bit [3] = '1' invert pixel output clock polarity Bit [2] = '1' to center the pixel output clock on the DOUT data = '0' to align the edges of the pixel output clock with DOUT data Bit [1] = '1' > PixelClock output at the imager pads into free-running-mode = '0' > PixelClock active only during readout Bit [0] = '1' to invert the PixelClock output **Default at Reset = 0x8002**

Address	Name	Description/Bits
0x010- 0x013	BIN_CNT_RST	These address ranges represent a total of four 15-bit timer compare points that can be used to trigger the BIN_CNT_RST pulse.
0x030 – 0x041	PULL_UP_DAC	These address ranges represent a total of eighteen 15-bit timer compare points that can be used to trigger PULL_UP_DAC pulse.
0x048 – 0x04B	AMP_ACT	These address ranges correspond to four 15-bit trigger points to produce the AMP_ACT pulse.
0x050 – 0x053	ZERO_RESET	These address ranges correspond to four 15-bit trigger points to produce the ZERO_RESET pulse.
0x060 – 0x063	FORCE_RESET	These address ranges correspond to four 15-bit trigger points to produce the FORCE_RESET pulse.
0x070 – 0x073	ADT_RESET	These address ranges correspond to four 15-bit trigger points to produce the ADT_RESET pulse.
0x090 – 0x093	RESET_LATCH	These address ranges correspond to four 15-bit trigger points to produce the RESET_LATCH pulse. Note this pulse is ACTIVE LOW.
0x0A0- 0x0A2	PRELOAD	These address ranges correspond to two 15-bit trigger points to produce the PRELOAD pulse.
0x0B0- 0x0B7	SHUTTER0	These address ranges represent a total of eight 15-bit timer compare points that can be used to trigger the SHUTTER 0 pulse.
0x0C0- 0x0C7	SHUTTER1	These address ranges represent a total of eight 15-bit timer compare points that can be used to trigger the SHUTTER 1 pulse.
0x0D0- 0x0D7	ROW_RESET0	These address ranges represent a total of eight 15-bit timer compare points that can be used to trigger the ROW_RESET 0 pulse.
0x0E0- 0x0E7	ROW_RESET1	These address ranges represent a total of eight 15-bit timer compare points that can be used to trigger the ROW_RESET 1 pulse.
0x100 – 0x109	MINUS_CNT	These address ranges represent a total of ten 15-bit timer compare points that can be used to trigger the MINUS CNT pulse.
0x110 – 0x119	PLUS_CNT	These address ranges represent a total of ten 15-bit timer compare points that can be used to trigger the PLUS CNT pulse.

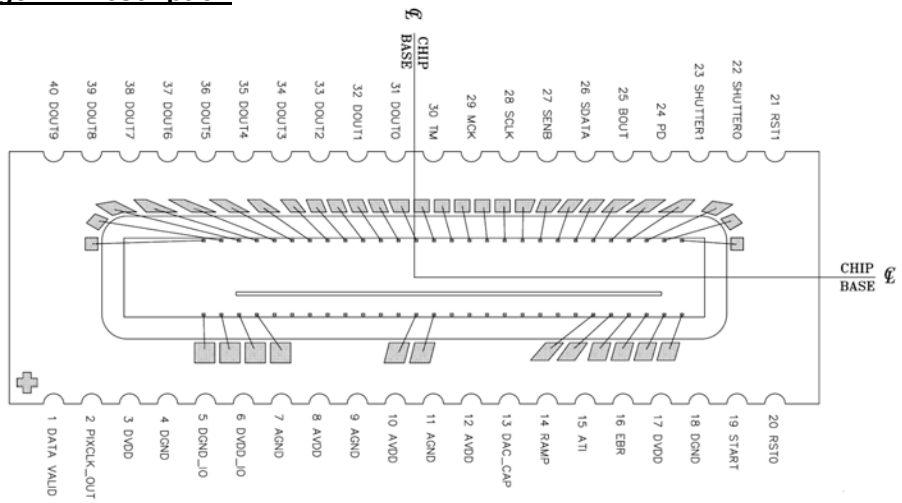
Address	Name	Description/Bits
0x120 – 0x12F	WRITE_IN	These address ranges represent a total of sixteen 15-bit timer compare points that can be used to trigger the WRITE IN pulse.
0x130 – 0x13B	TOGGLE_COUNTER	These address ranges represent a total of twelve 15-bit timer points that can be used to trigger the TOGGLE pulse.
0x140- 0x141	DATA_VALID	These addresses implement two 15-bit timer compare points that can be used to trigger the DATA_VALID signal to indicate valid pixel data on the output of the imager.
0x160- 0x163	READOUT_TIMER	These addresses implement four 15-bit timer compare points that can be used to start/stop the read-out period and corresponding read-out clocks
0x170- 0x182	BIN_CLK_TIMER	These addresses implement eighteen 15-bit timer compare points that can be used to start/stop the BINClock pulses.
0x210- 0x221	COUNTER_CLK	These registers implement eighteen 15-bit timers compare points that are used to start/stop the COUNTERClock pulses..
0x280 – 0x28B	EXTRA_CLOCK_COUNTER	These address ranges represent a total of twelve 15-bit timer compare points that can be used to trigger the EXTRA CLOCK pulse.
0x2B0- 0x2B7	SHUTTER2	These address ranges represent a total of eight 15-bit timer compare points that can be used to trigger the SHUTTER 2 pulse..
0x2C0- 0x2C7	SHUTTER3	These address ranges represent a total of eight 15-bit timer compare points that can be used to trigger the SHUTTER 3 pulse.
0x2D0- 0x2D7	ROW_RESET2	These address ranges represent a total of eight 15-bit timer compare points that can be used to trigger the ROW_RESET 2 pulse.
0x2E0- 0x2E7	ROW_RESET3	These address ranges represent a total of eight 15-bit timer compare points that can be used to trigger the ROW_RESET 3 pulse.
0x2F0 – 0x2F1	END_OF_LINE	These address ranges correspond to two 15-bit trigger points to produce the END_OF_LINE pulse. This will help to reset the pixels of the unused rows, so that all pixels start at the same value for the next frame.

Package and Pin out Information

40LCC Package Mechanical Information, P/N DLIS-2KA-LG

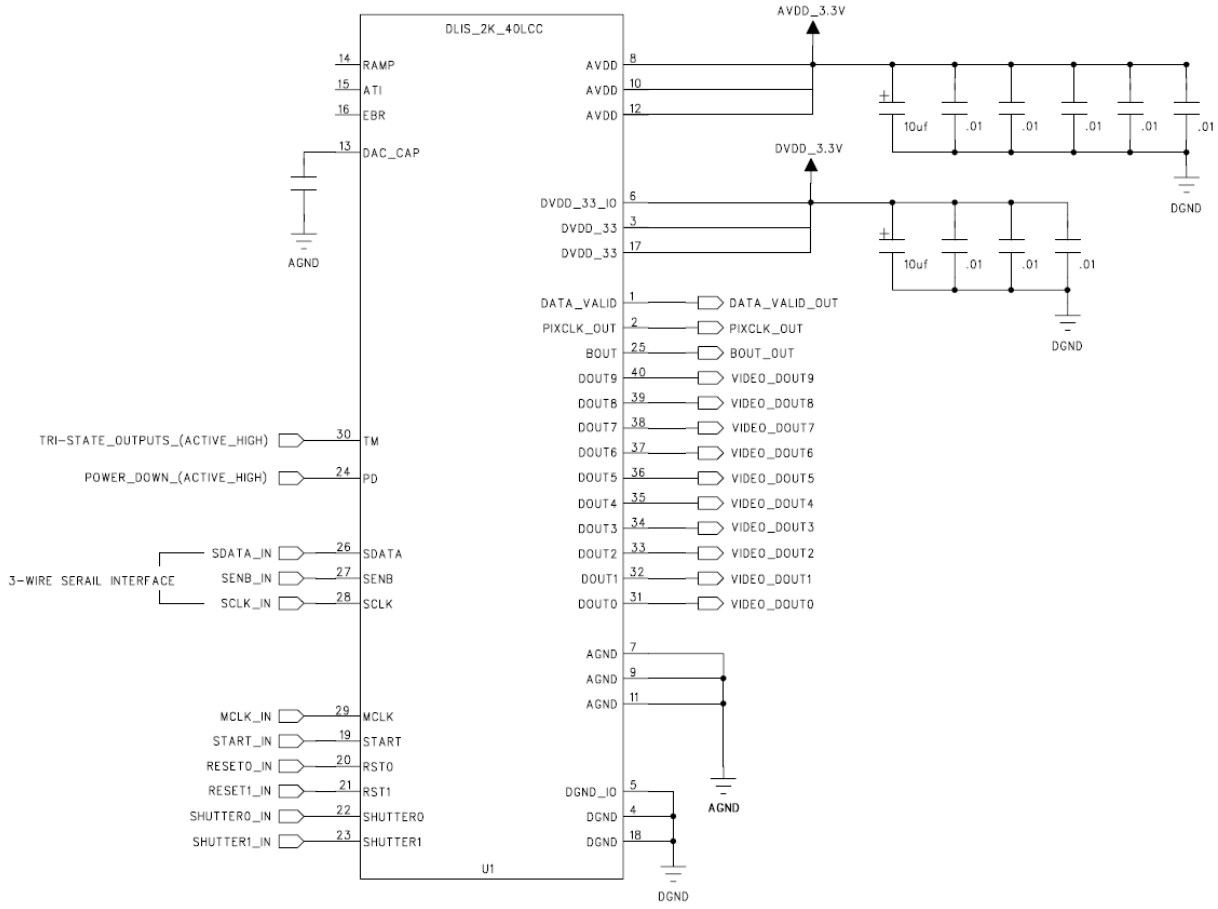


40LCC Package Pin Description



Pin #	Pin Name	PAD Type	Description
1	DATA_VALID	3-state Digital Output	Line valid signal to validate data on data bus
2	PIXCLK_OUT	3-state Digital Output	Pixel clock out for reference
3	DVDD	Bias	Digital 3.3V for digital core
4	DGND	Bias	Digital Ground
5	DGND_I/O	Bias	Ground digital I/O
6	DVDD_I/O	Bias	Digital 3.3V digital I/O
7	AGND	Bias	Analog Ground
8	AVDD	Bias	Analog 3.3V core
9	AGND	Bias	Analog Ground
10	AVDD	Bias	Analog 3.3V core
11	AGND	Bias	Analog Ground
12	AVDD	Bias	Analog 3.3V core
13	DAC_CAP	Analog Input	Cap input to Ramp DAC (normally floating)
14	RAMP	Analog I/O	Internal ramp output
15	ATI	Analog I/O	Analog Test Input for test purpose
16	EBR	Analog I/O	External Black Ref
17	DVDD	Bias	Digital 3.3V core
18	DGND	Bias	Digital Ground
19	START	Digital Pull down Input	Line initialization
20	RESET0	Digital Pull down Input	Row Reset0
21	RESET1	Digital Pull down Input	Row Reset1
22	SHUTTER0	Digital Pull down Input	Photo diode transfer0
23	SHUTTER1	Digital Pull down Input	Photo diode transfer1
24	PD	Digital Pull up Input	Power down mode
25	BOUT	3-state Digital Output pad	Binary output from Digital comparator
26	SDATA	3-state Digital I/O with pull down input.	Serial interface data
27	SENB	Digital Pull down Input	Serial interface enable
28	SCLK	Digital Input	Serial interface clock
29	MCLK	Digital Input	Master clock input at the 2x pixel rate
30	TM	3-state Digital I/O with pull down input	Digital I/O pad to test digital ckt and control 3-state output pad
31	DOUT0	3-state Digital Output	Digital Data out bit
32	DOUT1	3-state Digital Output	Digital Data out bit
33	DOUT2	3-state Digital Output	Digital Data out bit
34	DOUT3	3-state Digital Output	Digital Data out bit
35	DOUT4	3-state Digital Output	Digital Data out bit
36	DOUT5	3-state Digital Output	Digital Data out bit
37	DOUT6	3-state Digital Output	Digital Data out bit
38	DOUT7	3-state Digital Output	Digital Data out bit
39	DOUT8	3-state Digital Output	Digital Data out bit
40	DOUT9	3-state Digital Output	Digital Data out bit

Typical Application Circuit:



Semi-Custom Options

The DLIS-2K can be configured with additional features thru our semi-custom program. Features such as an additional row of pixels, color filters, microlens, and top glass coatings can be made available at a reduced cost. Contact sales@panavisionimaging.com, for more information

Product Errata

See document # PED00001 for DLIS-2K Errata Data

Characterization Criteria

Characterization measurements are guaranteed by design and are not tested for production parts. Unless otherwise specified, the measurements described herein are characterization measurements.

Pixel Clock Frequency

The pixel clock frequency is the frequency at which adjacent pixels can be reliably read. HDTV compatibility requires that the pixel clock frequency be 37.125 MHz for 30 frames/s operation although the imager will operate at considerably higher pixel rates. At higher pixel clock frequencies, the line overhead time is proportionately reduced and this eventually becomes the limiting factor in achieving high quality video.

Full Well

Full well (or Saturation Exposure) is the maximum number of photon-generated and/or dark current-generated electrons a pixel can hold. Full well is based on the capacitance of the pixel at a given bias. Full well is determined by measuring the capacitance of all pixels for the operational bias. In reality, the column circuitry will limit the signal swing on the pixel, so full well is defined as the number of electrons that will bring the output to the specified saturation voltage.

Quantum Efficiency

Quantum Efficiency is a measurement of the pixel ability to capture photon-generated charge as a function of wavelength. This is measured at 10nm increments over the wavelength range of the sensor typically 300 to 1100 nm for monochrome or 380 to 780 nm for color. Measurements are taken using a stable light source that is filtered using a monochromator. The exiting light from the monochromator is collimated to provide a uniform flux that overfills a portion of the sensor area. The flux at a given wavelength is measured using a calibrated radiometer and then the device under test is substituted and its response measured.

Linearity

Linearity is an equal corresponding output signal of the sensor for a given amount of photons incident on the pixel active area. Linearity is measured numerous ways. The most straightforward method is plotting the imager transfer function from dark to saturation and fitting a 'best fit' straight line from 1% to 75% of saturation. The maximum peak-peak deviation of the output voltage from the 'best fit' straight line is computed (E_{pp}) over the fitting range. Linearity (L) is then computed as shown below where V_{FS} is the full-scale voltage swing from dark to saturation measured with sensor gain at 0.0 dB.

$$L = \left(1 - {E_{pp}}/{V_{FS}}\right) \times 100\%$$

Average Dark Offset

The 'dark offset' is the voltage proportional to the accumulated electrons for a given integration period, that were not photon generated i.e. dark current. There are a few sources in CMOS circuits for the dark current and the dark current levels will vary even for a given process. Dark offset is measured for a 33.3 millisecond integration time at T_A = 25°C.

Image Lag

Image lag is the amount of residual signal in terms of percent of full well on the current frame of video after injecting the previous frame of video. Image lag is measured by illuminating an ROI to 50% of saturation for one frame and then rereading those pixels for the next and subsequent frames without light exposure. Any remaining residual signal will be measured and recorded in terms of percent of full well.

Dynamic Range

Dynamic range is determined by dividing the full-scale output voltage swing by the root mean squared (rms) temporal read noise voltage and expressed as a ratio or in decibels.

$$DR = 20\log\left[{V_{FS}}/{e_n}\right] = 20\log\left[{D_{FS}}/{D_n}\right]$$

Modulation Transfer Function (MTF)

MTF is a measure of the imager's ability to sense and reproduce contrast as a function of spatial frequency. The Nyquist limit for the DYNAMAX-35 sensor is TBD lp/mm. MTF is measured by illuminating a sensor with a Davidson Optronics PR-10 squarewave burst pattern having 11 discrete spatial frequencies. Therefore, strictly speaking, we are measuring Contrast Transfer Function (CTF) since squarewave targets are easier to obtain and work with. Images are captured with the input pattern oriented both horizontally and vertically and saved as 8-bit images. The sensor's response is derived from the captured images as shown below where M is the measured modulation and S_{MAX}, S_{MIN} are the digital numbers (DN) associated with the spatial frequency under evaluation.

$$M \equiv \frac{S_{MAX} - S_{MIN}}{S_{MAX} + S_{MIN}}$$

$$MTF \approx CTF \equiv M_{output} \Big/ M_{input}$$

Fixed Pattern Noise (FPN)

FPN, also known as dark signal non-uniformity (DSNU), is a measure of pixel-to-pixel variation when the array is in the dark. It is primarily due to dark current differences, reset noise and synchronous timing effects (at higher clock rates.) It is a signal-independent noise and is additive to the other noise powers. Offset variations within any column are inherently low due to the ACS® technology. Similarly, gain related FPN is almost non-existent due the ACS® technology. FPN is measured as a peak-to-peak variation along a line of video averaged to remove temporal noise.

Photoresponse Nonuniformity (PRNU)

PRNU is a measure of pixel-to-pixel variation in output (responsivity) under uniform illumination (usually illumination sufficient to bring the imager to half-scale output at unity gain i.e. half-well.) PRNU is a signal-dependent noise and is a multiplicative factor of the photoelectron number. Using uniform illumination, PRNU is measured over an ROI of 256H x 128V for each segment with a technique designed to remove temporal noise. The standard deviation of the histogram of all pixels in the ROI is divided by the average value and multiplied by 100%.

$$PRNU = \frac{V_{RMS}}{V_{AVG}} \times 100\%$$

References

1. J. Zarnowski, M. Pace and M. Joyner, “1.5 FET per Pixel Standard CMOS Active Column Sensor,” SPIE Vol. 3649-27, Jan 1999.
2. T.L.Vogelsong, J.J.Zarnowski, M.Pace and T.Zarnowski, “Scientific/industrial camera-on-a-chip using Active Column Sensor CMOS imager core,” SPIE Vol. 3965-11, Jan 2000.
3. Terry Zarnowski, “The Active Column Sensor CMOS Imager – Giving Better Images for Less,” April 2000, Sensors, Advanstar Communications.

NOTICE

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6,965,407 6,911,639 6,693,270 6,633,029 6,590,198 6,084,229 6,818,877 7,045,758 7,057,150

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