DAVICOM Semiconductor, Inc.

DM130120

15V / 30V Selectable Output & 122 Hi-V Channels Driver IC

DATA SHEET

Preliminary

Version: DM130120-11-MCO-DS-P01

July 11, 2016

Content

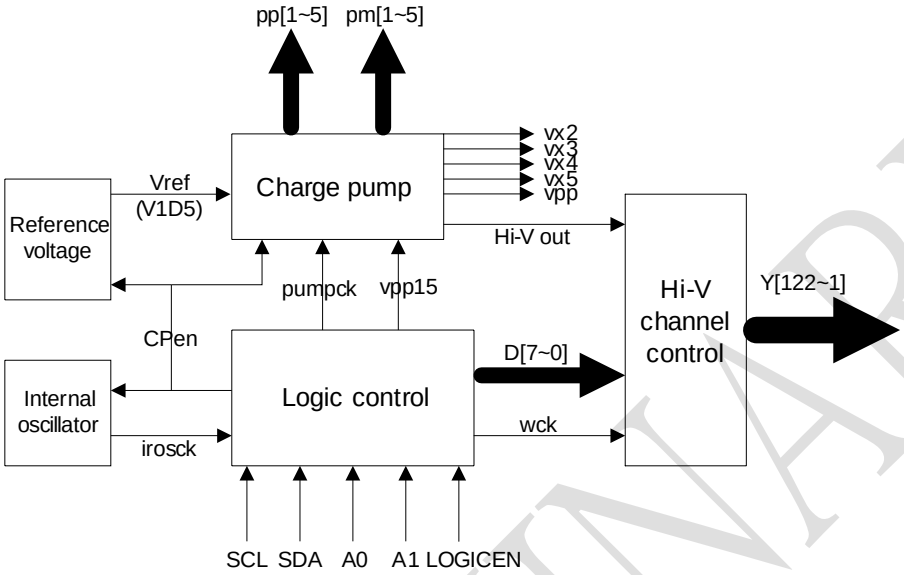
1 General Description

The DM130120 consist of Hi-V DC-DC charge pump for EPD (Electrophoretic display) application. User can chose 15V or 30V to drive EPD. All the function are controlled by 2-wires serial interface or SPI. DM130120 support synchronous serial signal interface (Maximum 4 chips cascadable).

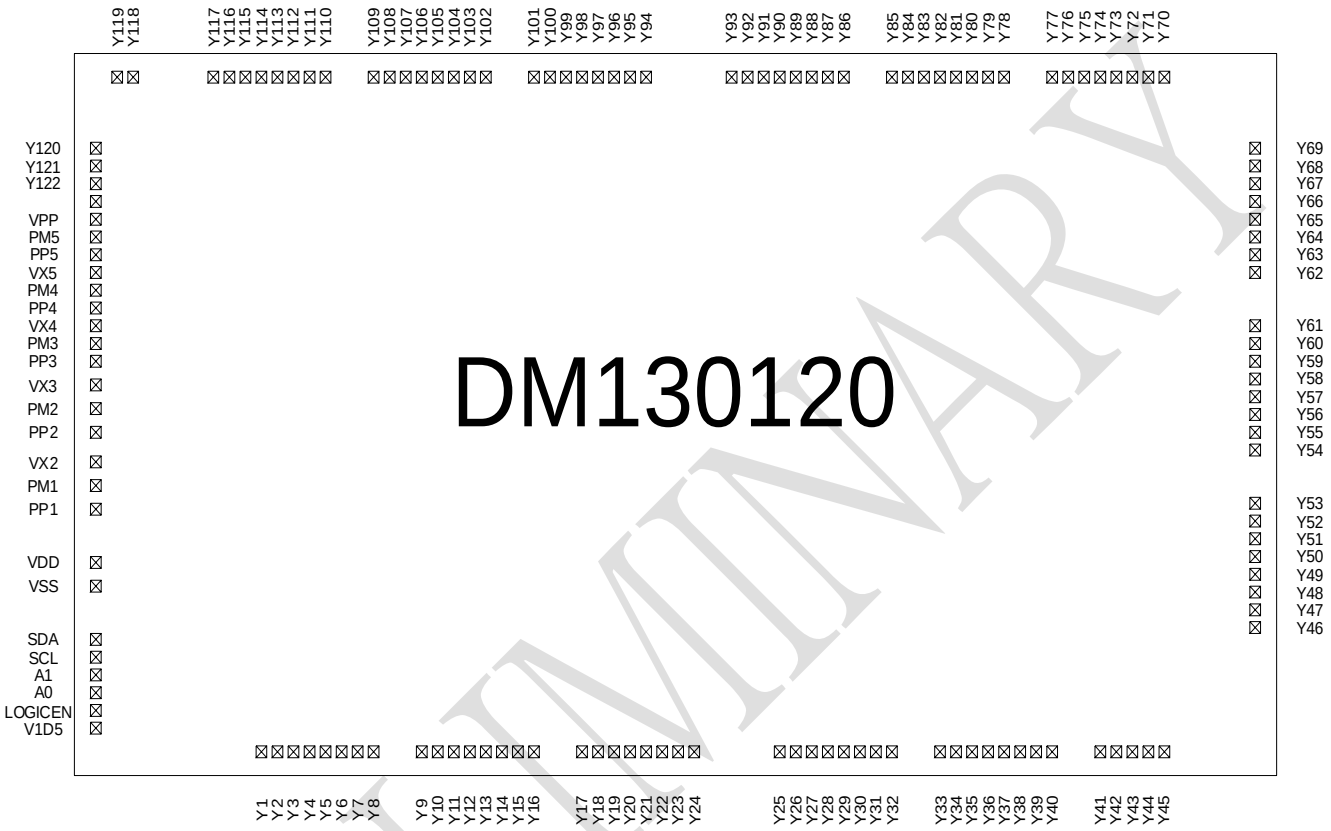
2 Features

- **Operating voltage 2.2V ~ 5.5V**
- **Selectable 15V or 30V driving voltage for EPD**
- **120 SEG + 1 COM + 1 Background**
- **DC-DC charge pump circuit**
- **ON chip RC oscillator**
- **2-wires serial interface**
- **SPI interface**
- **Voltage regulator**
- **Synchronous serial signal(Maximum 4 chips cascadable)**

3 Block Diagram



4 PAD Diagram



5 Pin Description

PIN NAME	Description
SCL	2-wires serial interface clock input
SDA / SPIEN	2-wires serial interface data input or SPIEN pin
A1 / SPICK	Device ID setting bit1 or SPICK pin
A0 / SPIDATA	Device ID setting bit0 or SPIDATA pin
LOGICEN	Select the control interface LOGICEN=1 2-wires serial interface LOGICEN=0 SPI interface
VPP	Charge pump output pin about 30v
VX5	Charge pump output pin about 15v
VX4	Charge pump output pin about 7.5v
VX3	Charge pump output pin about 5v
VX2	Charge pump output pin about 2.5v
PP[1:5]	Positive terminal for charge pump capacitor
PM[1:5]	Negative terminal for charge pump capacitor
Y[1:122]	EPD Hi-V channels
VDD	Positive power source
VSS	Negative power source
V1D5	Charge pump reference Voltage

Note：SCL & SDA need pull high resistor 4.7KΩ to VDD
VID5 needs connect to 0.1uF to VSS

5.1 TFBGA-145L Pin Assignment

	1	2	3	4	5	6	7
A	A1 / Y1	A2 / Y4	A3 / V1D5	A4 / LOGICEN	A5 / SDA	A6 / PP1	A7 / PM2
B	B1 / Y2	B2 / Y5	B3 / Y7	B4 / Y9	B5 / SCL	B6 / PP2	B7 / VX3
C	C1 / Y3	C2 / Y6	C3 / Y10	C4 / Y11	C5 / A1	C6 / VX2	C7 / PP3
D	D1 / Y8	D2 / Y12	D3 / Y 14	D4 / Y15	D5 / A0	D6 / PM1	D7 / VX4
E	E1 / Y13	E2 / Y16	E3 / Y18	E4 / Y19	E5 / VDD		
F	F1 / Y17	F2 / Y20	F3 / Y22	F4 / VSS			
G	G1 / Y21	G2 / Y23	G3 / Y25	G4 / Y26			
H	H1 / Y24	H2 / Y27	H3 / Y29	H4 / Y30			
J	J1 / Y28	J2 / Y31	J3 / Y32	J4 / Y33			
K	K1 / Y34	K2 / Y35	K3 / Y37	K4 / Y38	K5 / Y53	K6 / Y57	K7 / Y61
L	L1 / Y36	L2 / Y40	L3 / Y42	L4 / Y49	L5 / Y50	L6 / Y54	L7 / Y58
M	M1 / Y39	M2 / Y44	M3 / Y43	M4 / Y47	M5 / Y51	M6 / Y56	M7 / Y60
N	N1 / Y41	N2 / Y45	N3 / Y46	N4 / Y48	N5 / Y52	N6 / Y55	N7 / Y59
	8	9	10	11	12	13	
A	A8 / PM3	A9 / VX5	A10 / Y122	A11 / Y117	A12 / Y118	A13 / Y119	
B	B8 / PP4	B9 / PM5	B10 / Y120	B11 / Y116	B12 / Y115	B13 / Y113	
C	C8 / PM4	C9 / VPP	C10 / Y112	C11 / Y114	C12 / Y111	C13 / Y110	
D	D8 / PP5	D9 / Y121	D10 / Y108	D11 / Y109	D12 / Y107	D13 / Y106	
E			E10 / Y105	E11 / Y104	E12 / Y103	E13 / Y102	
F			F10 / Y100	F11 / Y101	F12 / Y99	F13 / Y98	
G			G10 / Y97	G11 / Y96	G12 / Y92	G13 / Y93	
H			H10 / Y95	H11 / Y94	H12 / Y91	H13 / Y90	
J			J10 / Y89	J11 / Y87	J12 / Y85	J13 / Y88	
K	K8 / Y65	K9 / Y83	K10 / Y86	K11 / Y84	K12 / Y80	K13 / Y82	
L	L8 / Y62	L9 / Y66	L10 / Y81	L11 / Y79	L12 / Y77	L13 / Y78	
M	M8 / Y64	M9 / Y68	M10 / Y76	M11 / Y75	M12 / Y70	M13 / Y74	
N	N8 / Y63	N9 / Y67	N10 / Y69	N11 / Y72	N12 / Y71	N13 / Y73	

5.2 LQFP-176L Pin Assignment

PIN No.	PIN Name	PIN No.	PIN Name	PIN No.	PIN Name	PIN No.	PIN Name
1	Y118	**45**	Y5	**89**	Y46	**133**	Y90
2	Y119	**46**	Y6	**90**	Y47	**134**	Y91
3		**47**	Y7	**91**	Y48	**135**	Y92
4		**48**	Y8	**92**	Y49	**136**	Y93
5		**49**	Y9	**93**	Y50	**137**	Y94
6		**50**	Y10	**94**	Y51	**138**	Y95
7		**51**	Y11	**95**	Y52	**139**	Y96
8		**52**	Y12	**96**	Y53	**140**	Y97
9	Y120	**53**	Y13	**97**	Y54	**141**	Y98
10	Y121	**54**	Y14	**98**	Y55	**142**	Y99
11	Y122	**55**	Y15	**99**	Y56	**143**	Y100
12	VPP	**56**	Y16	**100**	Y57	**144**	Y101
13	PM5	**57**	Y17	**101**	Y58	**145**	Y102
14	PP5	**58**	Y18	**102**	Y59	**146**	Y103
15	VX5	**59**	Y19	**103**	Y60	**147**	Y104
16	PM4	**60**	Y20	**104**	Y61	**148**	Y105
17	PP4	**61**	Y21	**105**	Y62	**149**	Y106
18	VX4	**62**	Y22	**106**	Y63	**150**	Y107
19	PM3	**63**	Y23	**107**	Y64	**151**	Y108
20	PP3	**64**	Y24	**108**	Y65	**152**	Y109
21	VX3	**65**	Y25	**109**	Y66	**153**	Y110
22	PM2	**66**	Y26	**110**	Y67	**154**	Y111
23	PP2	**67**	Y27	**111**	Y68	**155**	Y112
24	VX2	**68**	Y28	**112**	Y69	**156**	Y113
25	PM1	**69**	Y29	**113**	Y70	**157**	Y114
26	PP1	**70**	Y30	**114**	Y71	**158**	Y115
27	VDD	**71**	Y31	**115**	Y72	**159**	Y116
28	VSS	**72**	Y32	**116**	Y73	**160**	Y117
29	SDA	**73**	Y33	**117**	Y74	**161**	
30	SCL	**74**	Y34	**118**	Y75	**162**	
31	A1	**75**	Y35	**119**	Y76	**163**	
32	A0	**76**	Y36	**120**	Y77	**164**	
33	LOGICEN	**77**	Y37	**121**	Y78	**165**	
34	V1D5	**78**	Y38	**122**	Y79	**166**	
35		**79**	Y39	**123**	Y80	**167**	
36		**80**	Y40	**124**	Y81	**168**	
37		**81**	Y41	**125**	Y82	**169**	
38		**82**	Y42	**126**	Y83	**170**	
39		**83**	Y43	**127**	Y84	**171**	
40		**84**	Y44	**128**	Y85	**172**	
41	Y1	**85**	Y45	**129**	Y86	**173**	
42	Y2	**86**		**130**	Y87	**174**	
43	Y3	**87**		**131**	Y88	**175**	
44	Y4	**88**		**132**	Y89	**176**	

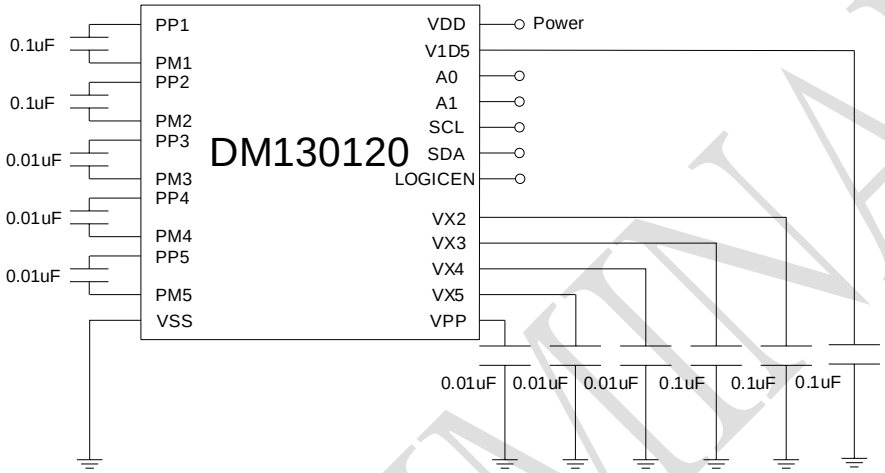
6 Function Description

6.1 Generate Hi-V Driving Bias Supply

6.1.1 Internal Charge Pump Supply

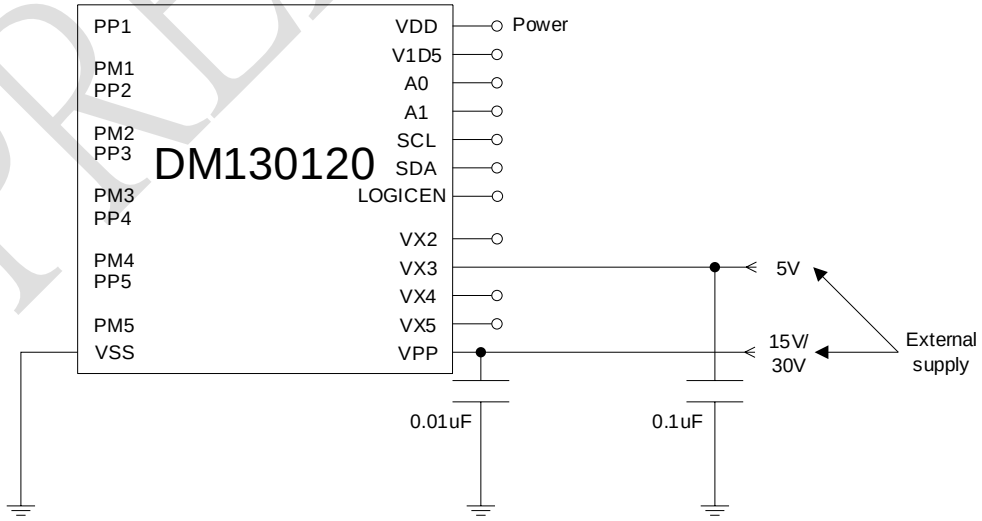
The charge pump circuit can generate Hi-voltage up to 30V. User also can select 0V, 15V or 30V to drive EPD by setting control register.

The value of Hi-voltage that pump can generate as following.
VPP=30V, VX5=15V, VSS=0V, set register #10h bit5 VPP15=0



6.1.2 External Driving Bias Supply

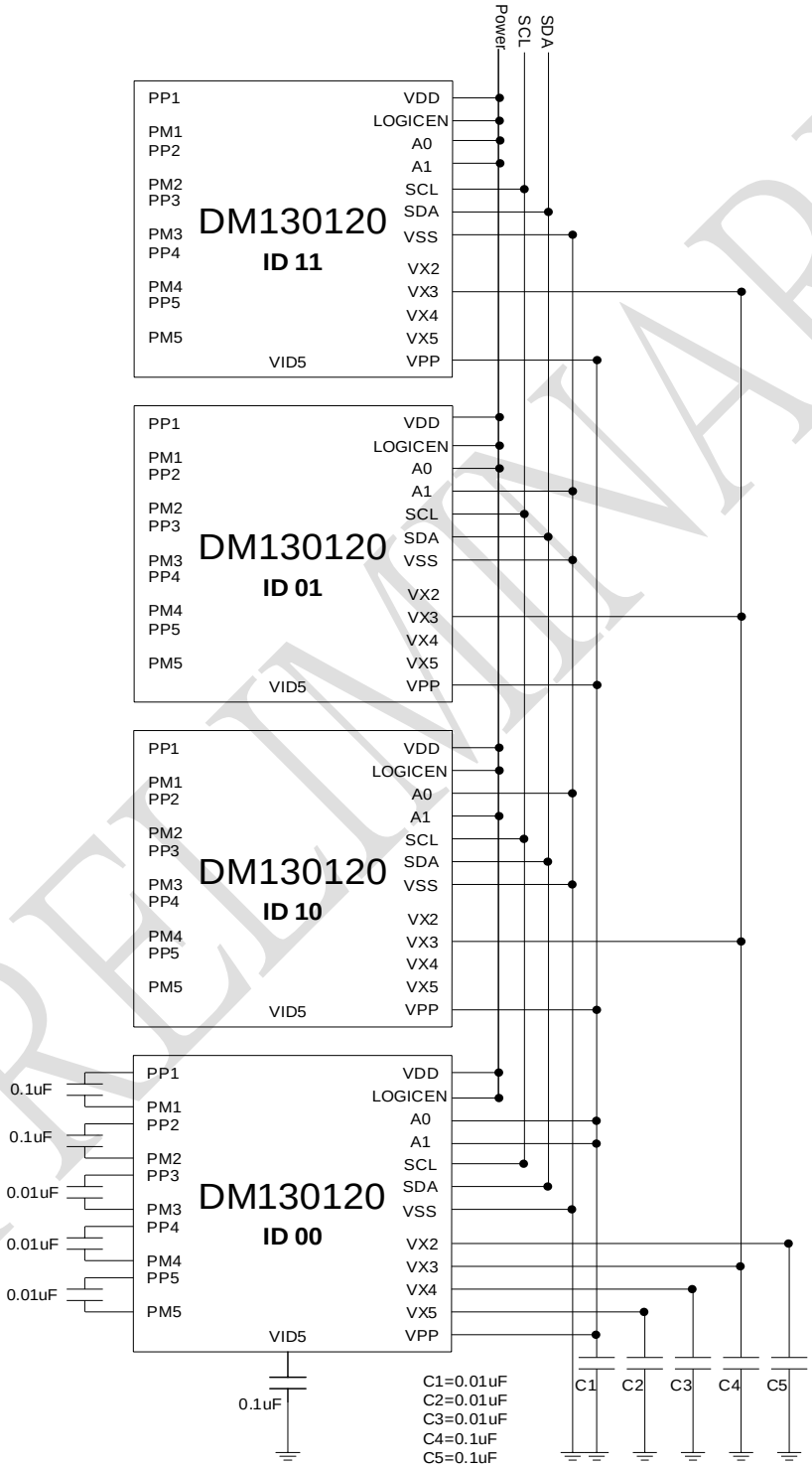
External Hi-V power source supply to VPP & VX3. First, user need to turn off internal pump function then supply 15V/30V to VPP , 5V to VX3



6.2 Multi-drivers Application

With 2-wires serial interface that the host device could control DM130120. (A1,A0) pins correspond the ID setting (Maximum support 4 chips). See the following figure for setting ID option.

Note: SPI don't support Multi-drivers application.



6.3 EPD Driver Control Register

REGISTER Address	Data							
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$00H	Y008	Y007	Y006	Y005	Y004	Y003	Y002	Y001
$01H	Y016	Y015	Y014	Y013	Y012	Y011	Y010	Y009
$02H	Y024	Y023	Y022	Y021	Y020	Y019	Y018	Y017
$03H	Y032	Y031	Y030	Y029	Y028	Y027	Y026	Y025
$04H	Y040	Y039	Y038	Y037	Y036	Y035	Y034	Y033
$05H	Y048	Y047	Y046	Y045	Y044	Y043	Y042	Y041
$06H	Y056	Y055	Y054	Y053	Y052	Y051	Y050	Y049
$07H	Y064	Y063	Y062	Y061	Y060	Y059	Y058	Y057
$08H	Y072	Y071	Y070	Y069	Y068	Y067	Y066	Y065
$09H	Y080	Y079	Y078	Y077	Y076	Y075	Y074	Y073
$0AH	Y088	Y087	Y086	Y085	Y084	Y083	Y082	Y081
$0BH	Y096	Y095	Y094	Y093	Y092	Y091	Y090	Y089
$0CH	Y104	Y103	Y102	Y101	Y100	Y099	Y098	Y097
$0DH	Y112	Y111	Y110	Y109	Y108	Y107	Y106	Y105
$0EH	Y120	Y119	Y118	Y117	Y116	Y115	Y114	Y113
$0FH	#	#	#	#	#	#	Y122	Y121
$10H	CPEN	C3	VPP15	C2	Load	C1	VSEL1	VSEL0

Y1~Y122 output setting：
Y1~Y120 mapping to segment pins
Y121 correspond to COM(Common) pin
Y122 correspond to BG(Background) pin

The output voltage (0V,15V,30V) for Y[1~122] are selectable.
If user want Y[1~122] to output 30V or 15V. Setting the correspond bit to “1”
If user want Y[1~122] to output 0V. Setting the correspond bit to “0”

Example：
If users wants Y9, Y11, Y13, Y15 output VPP and Y10, Y12, Y14,Y16 output “0V”
Register $01H = 01010101

Register “$10h” bit7 “CPEN”: Charge pump on / off
CPEN=1 , charge pump enable
CPEN=0 , charge pump disable

Register “$10h” bit6 “C3”：Internal test parameter C3. User has to set up “0” here.

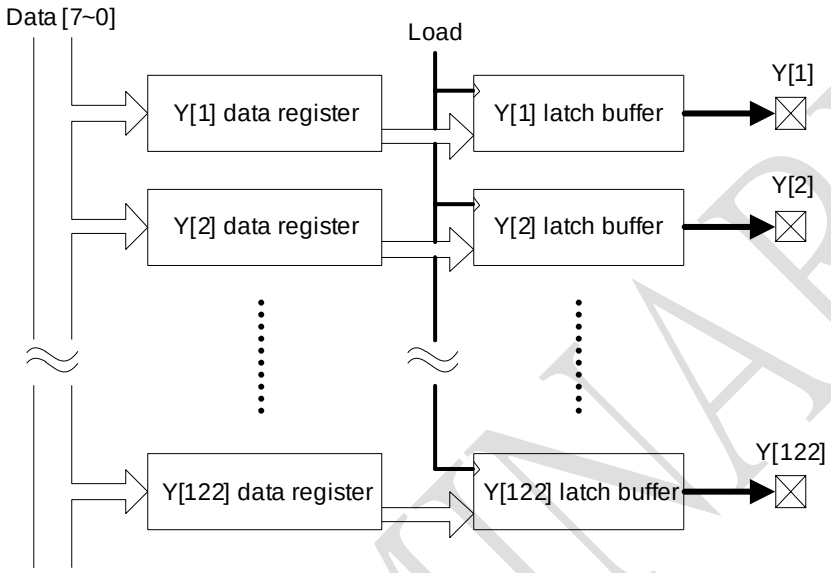
Register “$10h” bit5 “VPP15” ：Half VPP output switch
VPP15=1：Hi-V channels logic high will output VX5, the voltage equal to half VPP.
VPP15=0：Hi-V channels logic high will output VPP.

Register”$10h” bit4 “C2”：Internal test parameter “C2”. Set up “0” here for recommendation.

Register”$10h” bit3 “Load”：Load data from Y[1~122] and then latch out for synchronous
Load=1：Load data from Y[1~122] to output buffer
Load=0：Latch the buffer and output

Output Synchronous

For the reason of output synchronous that user have to set up $10h, bit3 = 0 first. This step will load the data Y [1~122] from register [$00h~$0Fh] into each buffer. And then set up $10h, bit3 = 1 for the next step. Y [1~122] latch buffers will latch and output the data synchronous.



Note: The data hold time for this bit should be over “1us”. That means, customer set up register $10h.bit3 =1 for latching output then wait over 1us that will be available for next data.

Register”$10h” bit2 “C1”: Internal test parameter “C1”. Set up “0” here for recommendation.

Register”$10h” bit0~1 “VSEL0~1”：Adjustable internal reference voltage
All the selections are shown as below:

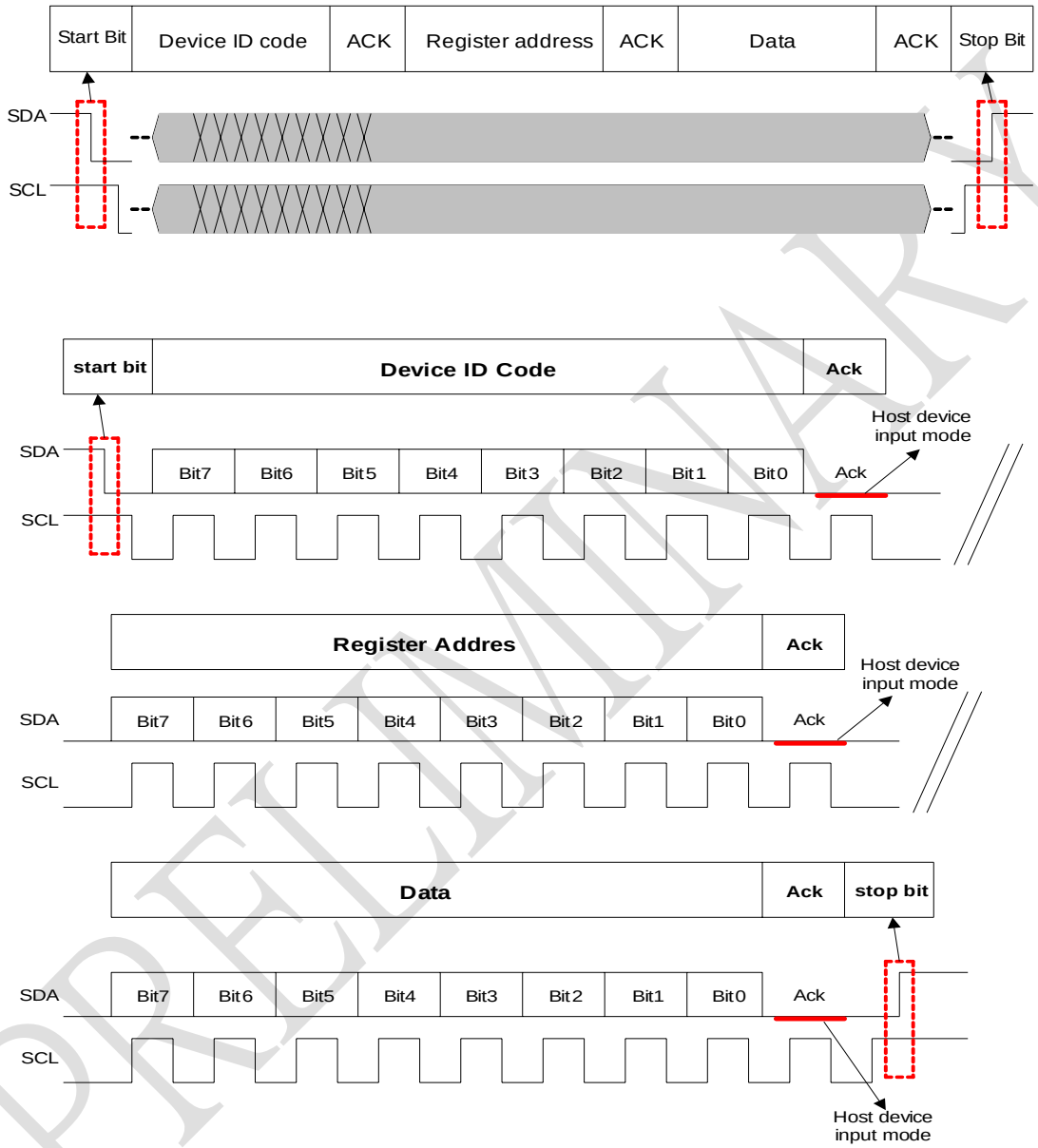
VSEL[1：0]	V1D5
00	1.5V
01	1.6V
10	1.7V
11	1.8V

Note:
1. All control registers don’t have initialize value after power on. Users need to initial all register manually.
2. $xxH means address and represent in hexadecimal form.
3. “xxxxxxxxb” means 8-bits data of register and represent in binary form.
4. The “VPP” here means the most high pumped voltage, “VX5” means half VPP and “GND” means the most low voltage of system power.
5. Write by default value 00b.

6.4 Control Signal Waveform

6.4.1 Format of One Byte (2-Wires Serial Interface)

This byte could be $00H ~ $10H, see 6.3 EPD driver control register.



Note: Timing diagram above is when SCL=500KHz

Device ID code：
ID code is defined by (A0&A1) pins. See multi-driver application in P10. Control signal input 8-bits “111100A1,A0” (A1,A0)=00,01,10,11 then only matched driver will operate.

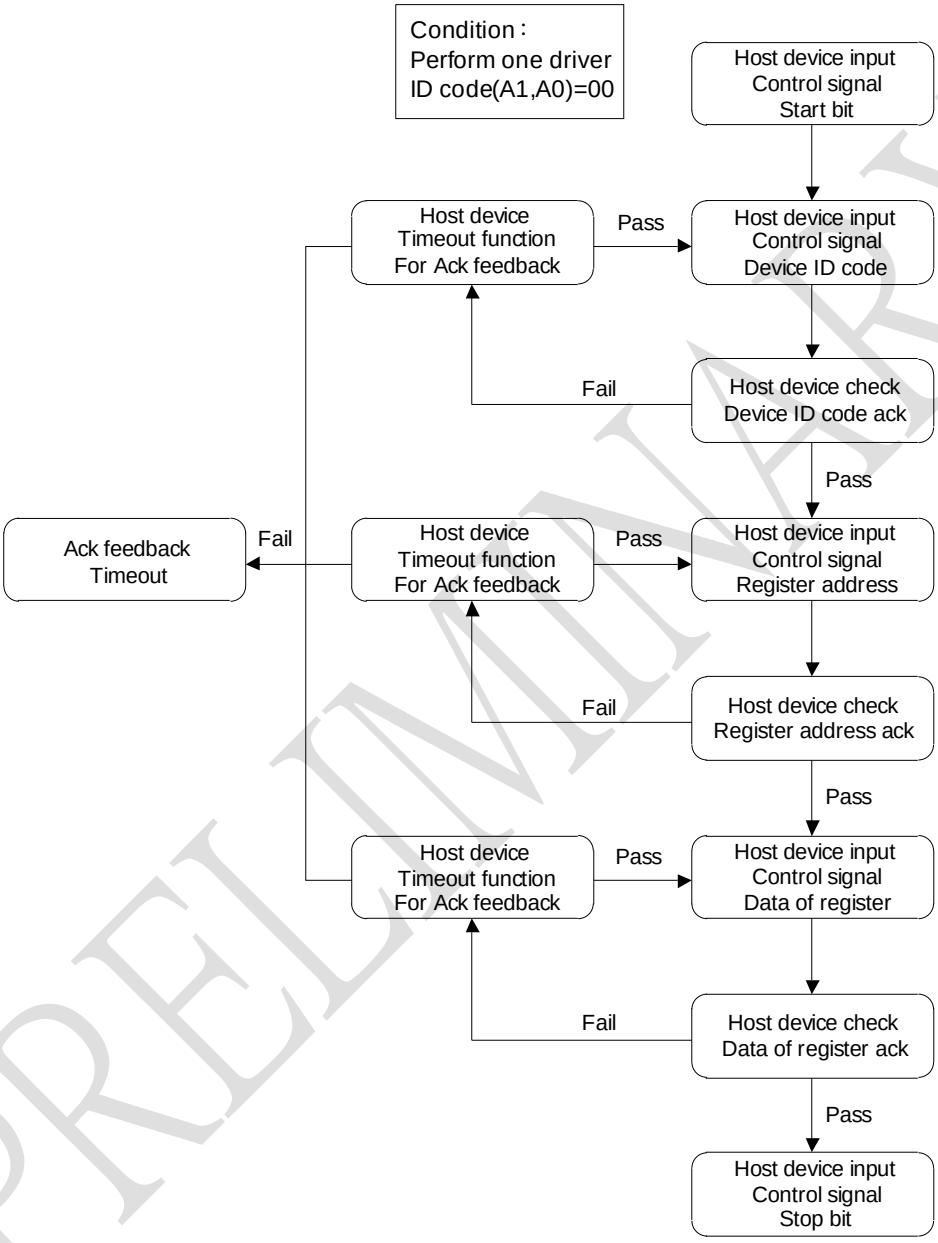
Register address：
Address of control register from $00H ~ $10H. The control signal here follow Device ID code

Data of register：
Definition of all control register see 6.3 EPD driver control register.

Condition setting

Perform with one driver IC and ID code (A1,A0)=00

Operate flow of one byte



Note：

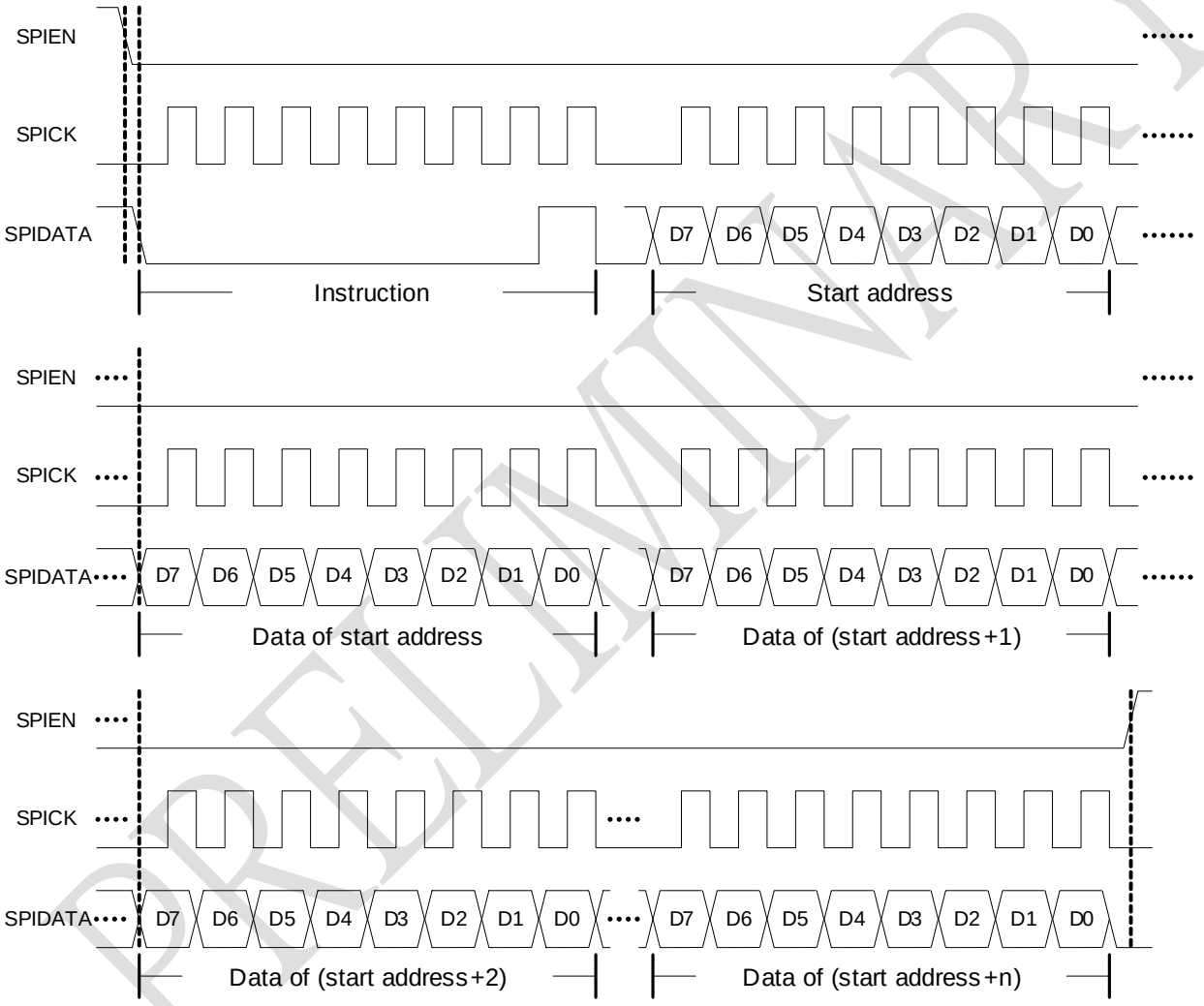
1. According to operating flow above, host device need set SDA to input mode at ACK feedback. Also check ACK feedback “Low” that means current byte transmission pass.
2. Each byte of control register has complete format as figure in P12. Following one-byte format to compose sequent transmission.
3. All the timing of pulse-width in operating flow above represents the minimum acceptable value.
4. Operating flow above is only for reference. For actual situation, please refer to E-paper spec.

6.4.2 SPI control waveform

There are two format of controlled signal as below.

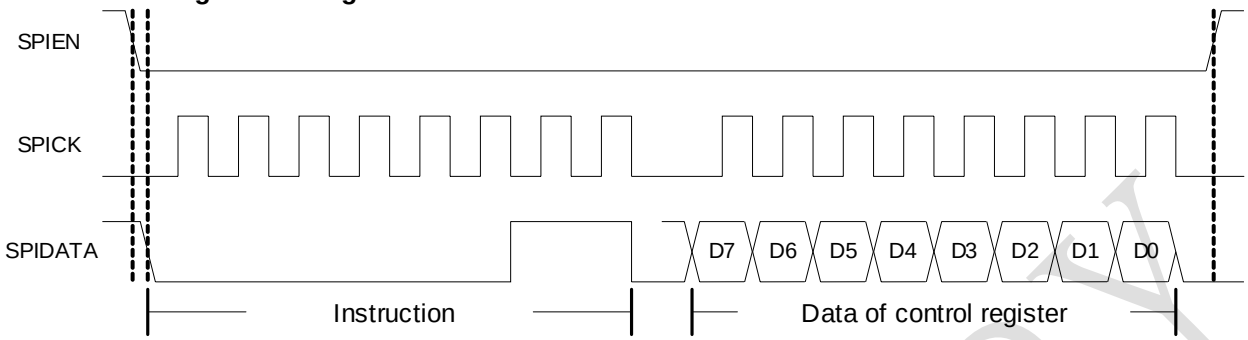
Instruction code	Function
00000001	Writing Data register
00000011	Writing control register

Format of writing data register



1. SPIEN low active
2. SPIDATA input instruction [00000001] to writing data register
3. SPIDATA input start address (selectable from $00H~$0FH)
4. SPIDATA input the data of start address
5. SPIDATA input data of next address. For example, start address from $00H à #FFH(contain of $00H) à #02H (here is the contain of $01H)….etc.
6. SPIEN high disable while data register writing finished.

Format of writing control register

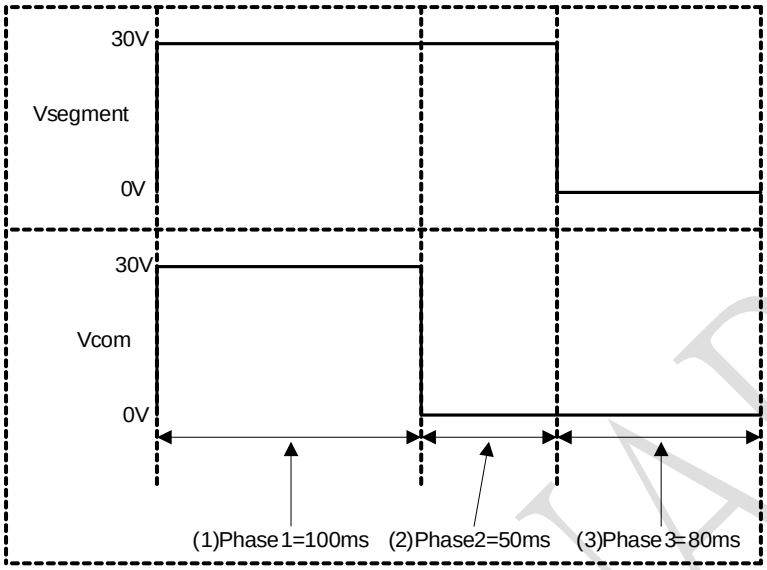


1. SPIEN low active
2. SPIDATA input instruction [00000011] for writing control register
3. SPIDATA input data of control register
4. SPIEN high disable after control register writing done.

Note：

1. ID code setting is not needed in SPI mode.
2. Writing data register could be sequent, but control register is single.

6.4.3 Com & Segment vs. Control Signal



Condition1-1：2-wires serial mode (one driver IC)

VDD=3V, use internal pumping function, perform with one driver IC, pin LOGICEN = 1, ID code (A1,A0)=00
Register $10H. bit5 VPP15=0, bit6 PUMPH=0 → VPP=30V
Vsegment including Y1~Y120, Vcom = Y121, Vbg = Y122

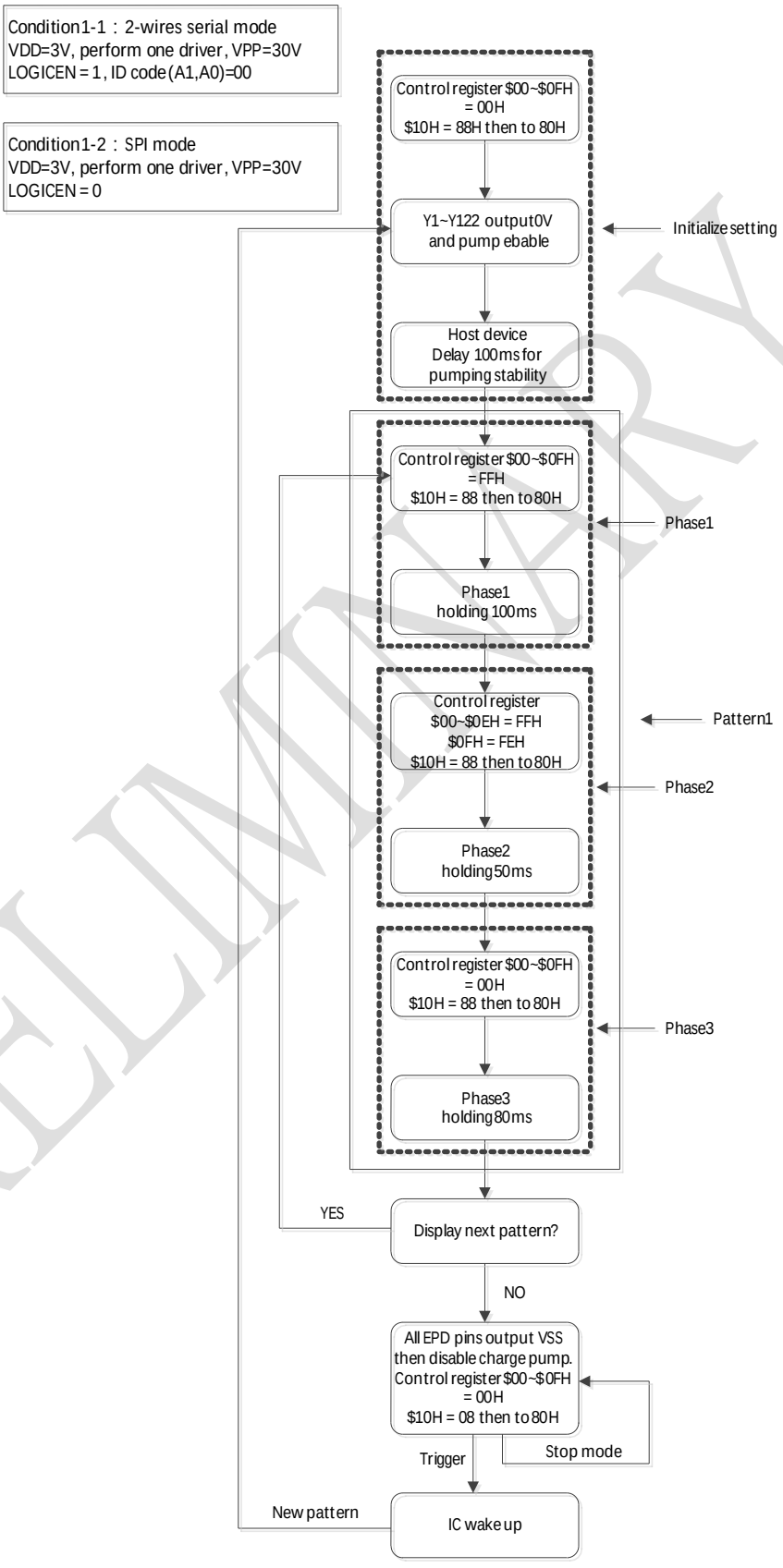
Condition1-2：SPI mode (one driver IC)

VDD=3V, use internal pumping function, perform with one driver IC, pin LOGICEN = 0
Register $10H. bit5 VPP15=0, bit6 PUMPH=0 → VPP=30V
Vsegment including Y1~Y120, Vcom = Y121, Vbg = Y122

Condition1-1 & 1-2 operate flow

1. Control register $00H~$0FH = “00000000b”, $10H = “10001000b”. This step Y1~Y122 will load data from data register and output “0V” to all EPD pins simultaneously.
   After that $10H = “10000000b” here will latch all EPD pins to “0V” and enable charge pump.
   Note! $10H bit3 load = 1 → 0 will load all data to EPD pins and then latch output state.
2. Host device delay 100ms for internal pumping stability.
3. Control register $00H~$0FH = “11111111b” , $10H = “10001000b”.
   Then $10H = “10000000b”. Here all EPD pins will output VPP.
4. Host device delay 100ms to display phase1 pattern.
5. Control register $00H~$0EH = “11111111b” , $0FH = “11111110b” , $10H = “10001000b”. Then $10H = “10000000b”. All segment & background will output VPP, Y121 output “0V”.
6. Host device delay 50ms to display phase2 pattern.
7. Control register $00H~$0FH = “00000000b” , $10H = “10001000b”.
   Then $10H = “10000000b”. All EPD pins will output “0V”.
8. Host device delay 80ms to display phase3 pattern.
9. All EPD pins output “0V” and disable charge pumping if there’s no pattern will be display.

Note：$xxH means address and represent in hexadecimal forml.
“xxxxxxxxb” means 8-bits data and represent in binary form.



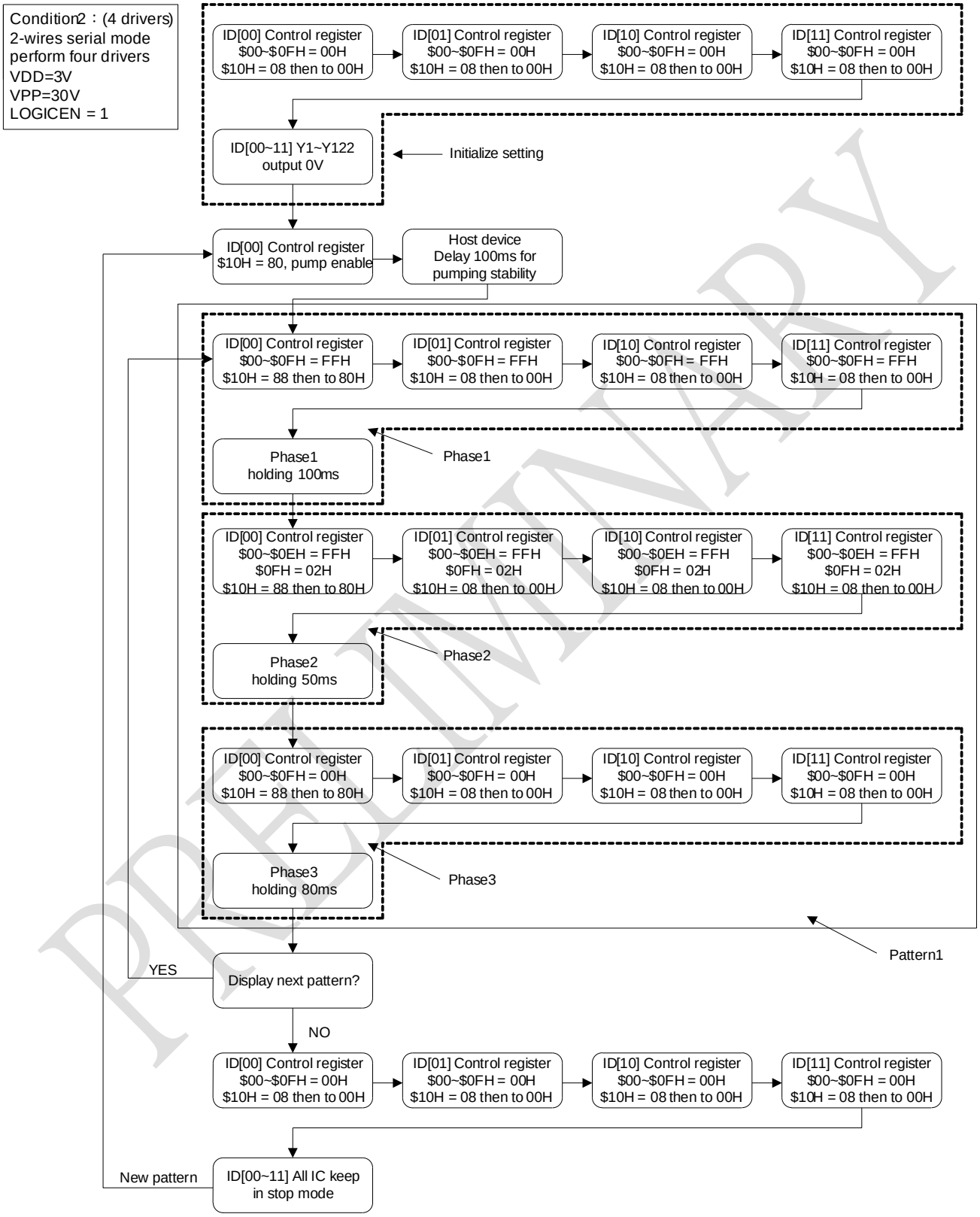
Condition2：2-wires serial mode(cascade four drivers)

VDD=3V , perform with four drivers, one driver to be the pumping source and others set up supply from external source, pin LOGICEN = 1
Register $10H. bit5 VPP15=0, bit6 PUMPH=0 → VPP=30V
Vsegment including Y1~Y120, Vcom = Y121, Vbg = Y122

Condition2 operate flow

1. ID[00] Control register $00H~$0FH = “00000000b”, $10H = “00001000b”. This step Y1~Y122 will load data from data register and output “0V” to all EPD pins simultaneously.
   After that $10H = “00000000b” here will latch all EPD pins to “0V”.
   Note! $10H bit3 load = 1 → 0 will load all data to EPD pins and then latch output state.
2. ID[01~11] follow step1 to initialize all EPD pins to output “0V”
3. ID[00] register $10H = “10000000b” to enable charge pump and take ID[00] as pumping source others IC set up supply from external source.
4. Host device delay 100ms for internal pumping stability.
5. ID[00~11] Control register $00H~$0FH = “11111111b” , *ID[00] $10H = “10001000b” , ID[01~11] $10H = “00001000b”. Then ID[00] $10H = “10000000b” , ID[01~11] $10H = “00000000b”. Here all EPD pins will output VPP.
6. Host device delay 100ms to display phase1 pattern.
7. ID[00~11] Control register $00H~$0EH = “11111111b” , $0FH = “00000010b” , *ID[00] $10H = “10001000b” , ID[01~11] $10H = “00001000b”. Then ID[00] $10H = “10000000b” , ID[01~11] $10H = “00000000b”. All segment & background will output VPP, but Y121 output “0V”.
8. Host device delay 50ms to display phase2 pattern.
9. ID[00~11] Control register $00H~$0FH = “00000000b” , *ID[00] $10H = “10001000b” , ID[01~11] $10H = “00001000b”. Then ID[00] $10H = “10000000b” , ID[01~11] $10H = “00000000b”. All EPD pins will output “0V”.
10. Host device delay 80ms to display phase3 pattern.
11. All EPD pins output “0V” and disable charge pumping if there’s no pattern will be display.

Note：$xxH means address and represent in hexadecimal form.
“xxxxxxxxb” means 8-bits data and represent in binary form.



7 Operating Ratings

Description	Symbol	Value			Unit
		Min	Typ	Max	
Working voltage	VDD	2.2	3	5.5	V
Driver High-voltage capability	Vdrv		30	32	V
Ripple	Vrip		200		mV
High-voltage1	Vpp15		15V	18V	V, (load =15M ohm)
High-voltage2	Vpp30		30V		V, (load =15M ohm)
Stop mode current	Istop		0.1		uA
Pumping enable current	Icpen		350		uA
Input high voltage	VIH		0.8*VDD		V
Input low voltage	VIL		0.2*VDD		V
2wir speed (SCL&SDA)	FI2C			1M	Hz
2wir load capacitance	CI2C		15		pF
SPI speed	FSPI			1M	Hz
SPI load capacitance	CSPI		15		pF

Note：

1. Symbol “2wir” represent SCL & SDA pins
2. Symbol “VPP_{15}” apply to Eink 15V film. For the better life time that customer have to tie each 122 channels to “0V” then turn off charge pumping.

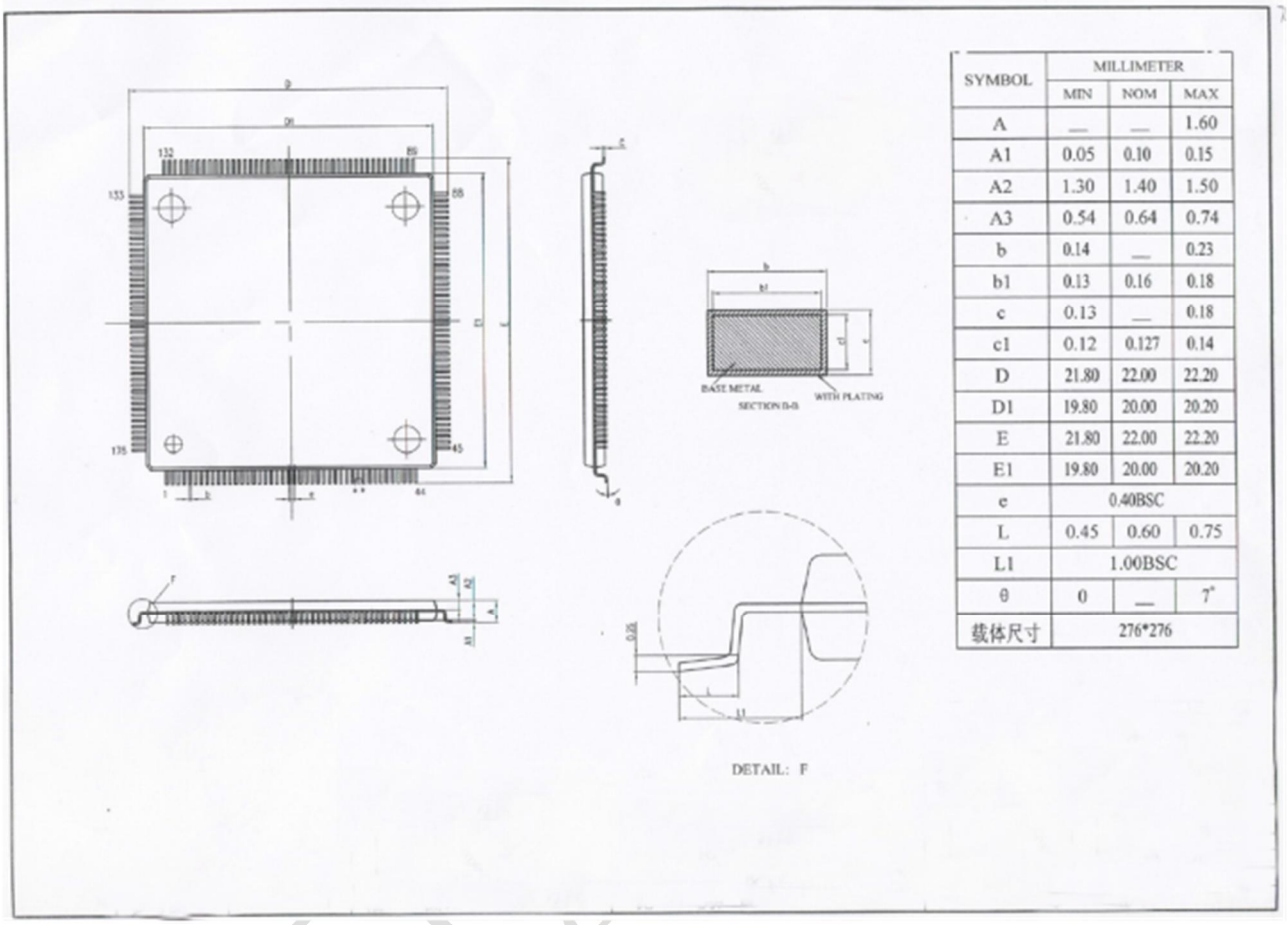
8 Absolute Maximum Ratings

Symbol	Description	Rating	Unit
Vdd	Supply Voltage	-0.5 ~ +3.6	V
Vin	Input Voltage	-0.5 ~ VDD +0.5	V
Vout	Output Voltage	-0.5 ~ VDD +0.5	V
Topr	Operation Temperature	0 ~ 70	℃
Tstg	Storage Temperature	-40 ~ 125	℃

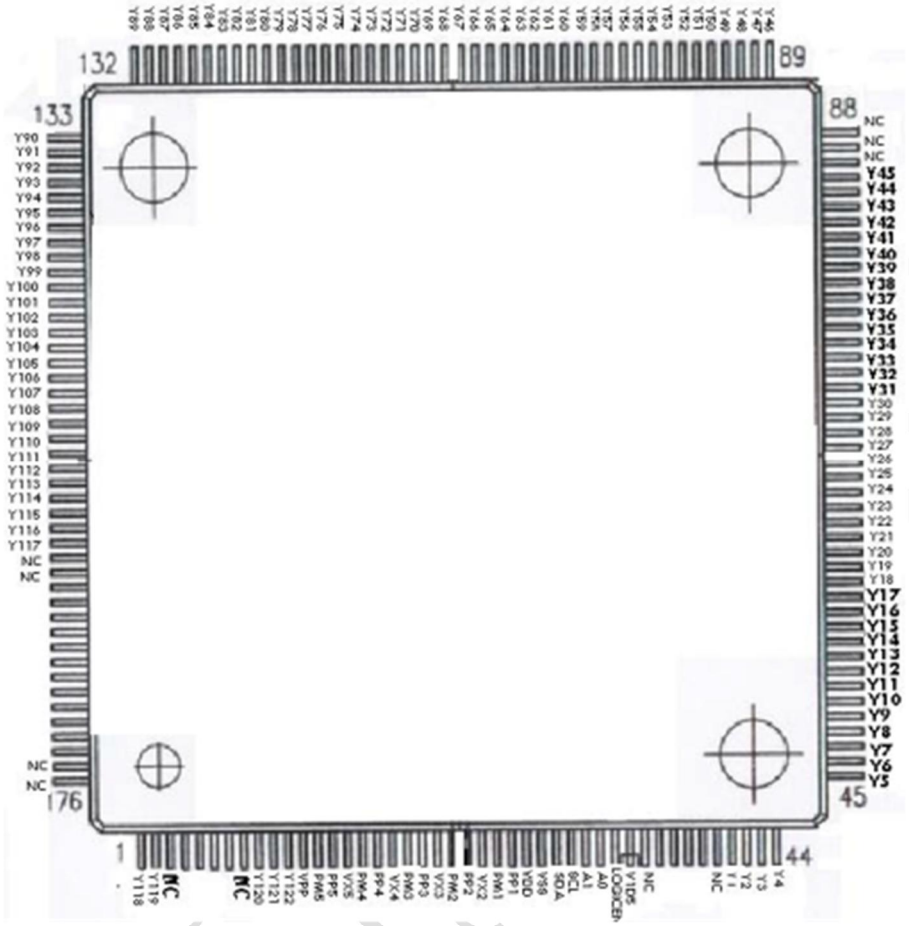
9 Package Information

9.1 Package Detail Information

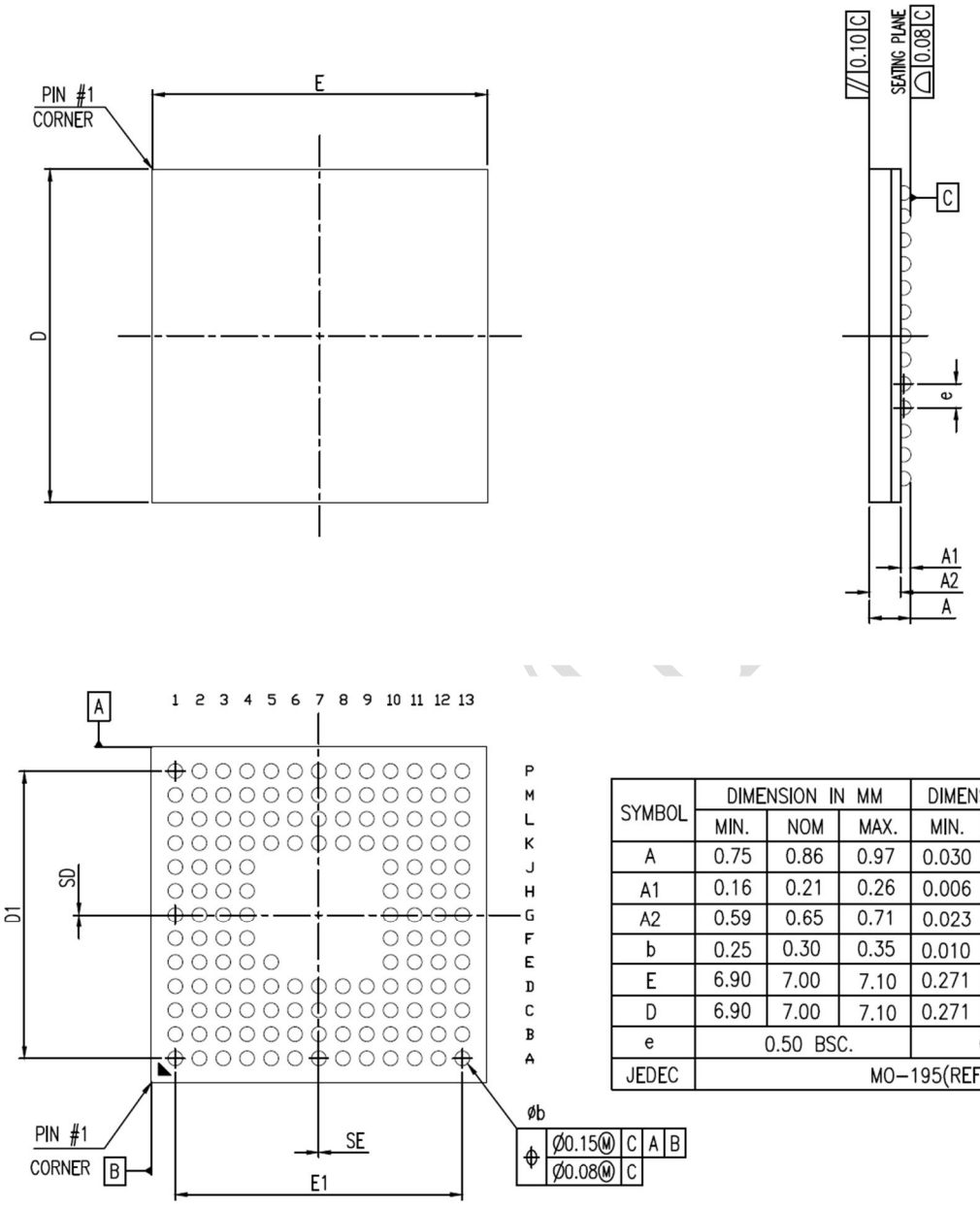
LQFP-176L



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	0.10	0.15
A2	1.30	1.40	1.50
A3	0.54	0.64	0.74
b	0.14	—	0.23
b1	0.13	0.16	0.18
c	0.13	—	0.18
c1	0.12	0.127	0.14
D	21.80	22.00	22.20
D1	19.80	20.00	20.20
E	21.80	22.00	22.20
E1	19.80	20.00	20.20
e	0.40BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	7°
载体尺寸	276*276		



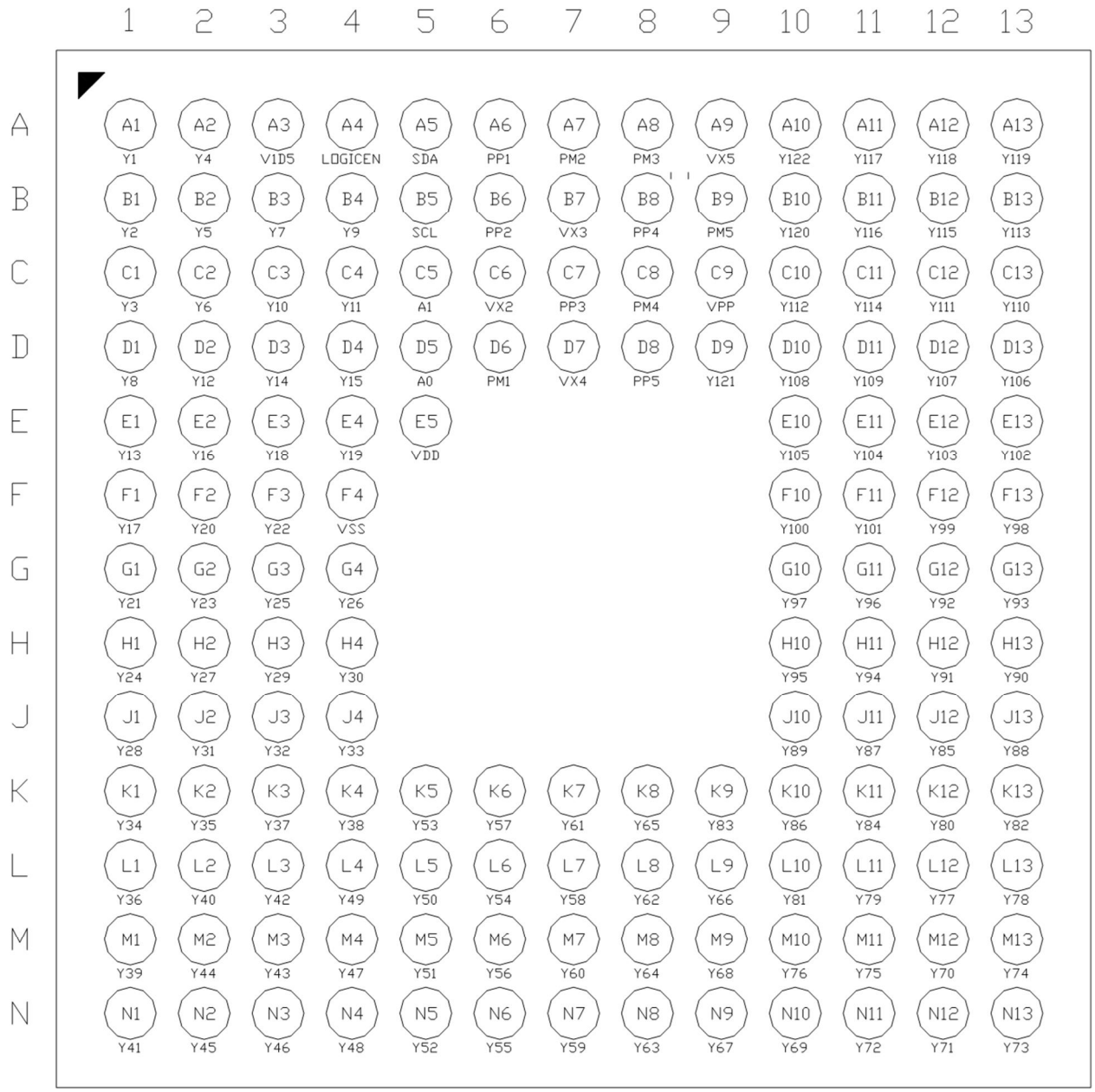
TFBGA-145L



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	0.75	0.86	0.97	0.030	0.034	0.038
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.59	0.65	0.71	0.023	0.026	0.028
b	0.25	0.30	0.35	0.010	0.012	0.014
E	6.90	7.00	7.10	0.271	0.276	0.280
D	6.90	7.00	7.10	0.271	0.276	0.280
e	0.50 BSC.			0.020 BSC.		
JEDEC	MO-195(REF.)					

N	SD(mm)	SE (mm)	D1 (mm)	E1 (mm)	JEDEC(REF)
145	0.00 BSC.	0.00 BSC.	6.00 BSC.	6.00 BSC.	

TFBGA-145L


1 2 3 4 5 6 7 8 9 10 11 12 13
A A1 Y1 | A2 Y4 | A3 V1D5 | A4 LOGICEN | A5 SDA | A6 PP1 | A7 PM2 | A8 PM3 | A9 VX5 | A10 Y122 | A11 Y117 | A12 Y118 | A13 Y119
B B1 Y2 | B2 Y5 | B3 Y7 | B4 Y9 | B5 SCL | B6 PP2 | B7 VX3 | B8 PP4 | B9 PM5 | B10 Y120 | B11 Y116 | B12 Y115 | B13 Y113
C C1 Y3 | C2 Y6 | C3 Y10 | C4 Y11 | C5 A1 | C6 VX2 | C7 PP3 | C8 PM4 | C9 VPP | C10 Y112 | C11 Y114 | C12 Y111 | C13 Y110
D D1 Y8 | D2 Y12 | D3 Y14 | D4 Y15 | D5 A0 | D6 PM1 | D7 VX4 | D8 PP5 | D9 Y121 | D10 Y108 | D11 Y109 | D12 Y107 | D13 Y106
E E1 Y13 | E2 Y16 | E3 Y18 | E4 Y19 | E5 VDD | E10 Y105 | E11 Y104 | E12 Y103 | E13 Y102
F F1 Y17 | F2 Y20 | F3 Y22 | F4 VSS | F10 Y100 | F11 Y101 | F12 Y99 | F13 Y98
G G1 Y21 | G2 Y23 | G3 Y25 | G4 Y26 | G10 Y97 | G11 Y96 | G12 Y92 | G13 Y93
H H1 Y24 | H2 Y27 | H3 Y29 | H4 Y30 | H10 Y95 | H11 Y94 | H12 Y91 | H13 Y90
J J1 Y28 | J2 Y31 | J3 Y32 | J4 Y33 | J10 Y89 | J11 Y87 | J12 Y85 | J13 Y88
K K1 Y34 | K2 Y35 | K3 Y37 | K4 Y38 | K5 Y53 | K6 Y57 | K7 Y61 | K8 Y65 | K9 Y83 | K10 Y86 | K11 Y84 | K12 Y80 | K13 Y82
L L1 Y36 | L2 Y40 | L3 Y42 | L4 Y49 | L5 Y50 | L6 Y54 | L7 Y58 | L8 Y62 | L9 Y66 | L10 Y81 | L11 Y79 | L12 Y77 | L13 Y78
M M1 Y39 | M2 Y44 | M3 Y43 | M4 Y47 | M5 Y51 | M6 Y56 | M7 Y60 | M8 Y64 | M9 Y68 | M10 Y76 | M11 Y75 | M12 Y70 | M13 Y74
N N1 Y41 | N2 Y45 | N3 Y46 | N4 Y48 | N5 Y52 | N6 Y55 | N7 Y59 | N8 Y63 | N9 Y67 | N10 Y69 | N11 Y72 | N12 Y71 | N13 Y73

10 Ordering Information

Part Number	Pin Count	Package
DM130120W	-	Wafer (Pb-Free)
DM130120WB	-	Wafer + Gold bump (Pb-Free)
DM130120	146	Dice (Pb-Free)
DM130120B	146	Dice + Gold bump (Pb-Free)
DM130120GP	145	TFBGA 145L (Pb-Free)
DM130120EP	176	LQFP 176L (Pb-Free)
DM130120C	177	COF (Roll) (Pb-Free)
DM130120P	177	COF (Tray) (Pb-Free)

Disclaimer

The information appearing in this publication is believed to be accurate. Integrated circuits sold by DAVICOM Semiconductor are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. DAVICOM makes no warranty, express, statutory, implied or by description regarding the information in this publication or regarding the information in this publication or regarding the freedom of the described chip(s) from patent infringement. FURTHER, DAVICOM MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. DAVICOM reserves the right to halt production or alter the specifications and prices at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders. Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by DAVICOM for such applications.

Please note that application circuits illustrated in this document are for reference purposes only.

DAVICOM's terms and conditions printed on the order acknowledgment govern all sales by DAVICOM. DAVICOM will not be bound by any terms inconsistent with these unless DAVICOM agrees otherwise in writing. Acceptance of the buyer's orders shall be based on these terms.

Company Overview

DAVICOM Semiconductor Inc. develops and manufactures integrated circuits for integration into data communication products. Our mission is to design and produce IC products that are the industry's best value for Data, Audio, Video, and Internet/Intranet applications. To achieve this goal, we have built an organization that is able to develop chipsets in response to the evolving technology requirements of our customers while still delivering products that meet their cost requirements.

Products

We offer only products that satisfy high performance requirements and which are compatible with major hardware and software standards. Our currently available and soon to be released products are based on our proprietary designs and deliver high quality, high performance chipsets that comply with modem communication standards and Ethernet networking standards. ***For customized products, please contact to Davicom's sales***

Contact Windows

For additional information about DAVICOM products, contact the Sales department at:

Headquarters

Hsin-chu Office:
No.6, Li-Hsin 6th Rd.,
Hsinchu Science Park,
Hsin-chu City 300, Taiwan, R.O.C.
TEL: +886-3-5798797
FAX: +886-3-5646929
MAIL: sales@davicom.com.tw
HTTP: http://www.davicom.com.tw

WARNING
Conditions beyond those listed for the absolute maximum may destroy or damage the products. In addition, conditions for sustained periods at near the limits of the operating ranges will stress and may temporarily (and permanently) affect and damage structure, performance and function.