

General Description

The DM1613 is a liquid crystal dot matrix display module that consists of LCD panel LCD-5013, LCD control driver HD44780 and is capable of providing 16 characters x 1 line (5 x 7 dots / character + cursor) display. It contains a controller, a data RAM, and a character generator ROM required for providing display. Data interfacing is in 8-bit parallel or 4-bit parallel and data can be written in or read from a microprocessor.

General Specifications

1. Display method	1/5bias 1/16duty
2. Display content	16 characters x 1 line
3. Dots organizing 1 character	5 x 7 dots/character + cursor
4. Display data RAM	80 x 8 bits
5. Character generator ROM	160-character JIS font set + 32-character special font set Refer to Table 1.
6. Character generator RAM	64 x 8 bits 5 x 7 dots 8 characters
7. Instruction function	Refer to Table 2.
8. Circuit diagram	Refer to Fig. 3.

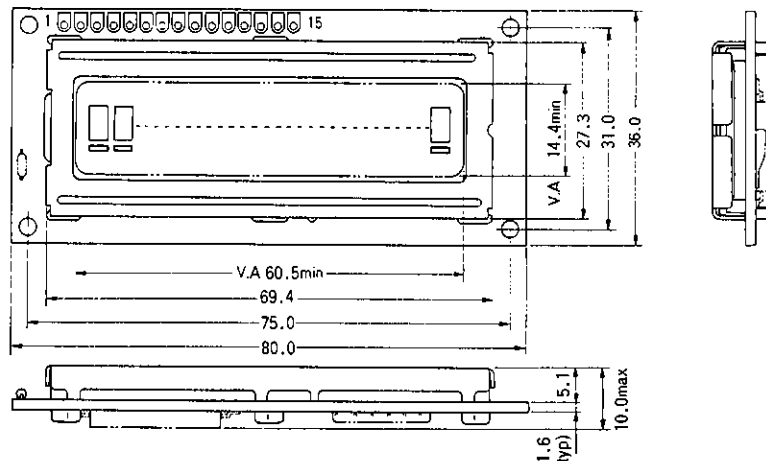
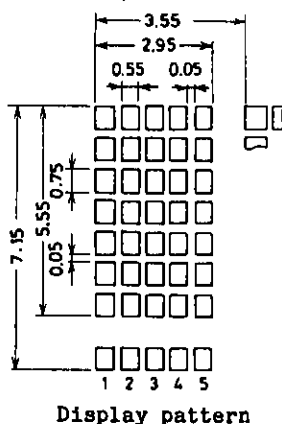
Outline

1. Module outline	36.0(W) x 80.0(L) x 10(T) (mm ³)
2. View area	60.5 x 14.4 (mm ²)
3. Dot size	0.55 x 0.75 (mm ²)
4. Dot pitch	0.60 x 0.80 (mm ²)
5. Character size(5x7 dots)	2.95 x 5.55 (mm ²)

Absolute Maximum Ratings at Ta=25°C

			unit
Maximum Supply Voltage	$V_{DD}-V_{SS}$	-0.3 to +7	V
Input Voltage	V_I	-0.3 to $V_{DD}+0.3$	V
LCD Drive Voltage	$V_{DD}-V_O$	-0.3 to +9	V
Operating Temperature	T_{opr}	0 to +50	°C
Storage Temperature	T_{stg}	-20 to +70	°C

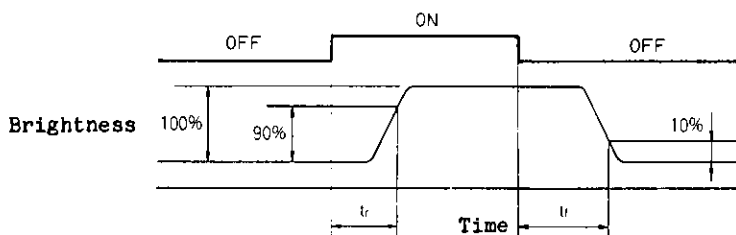
Module Dimensions 5009 (unit: mm)



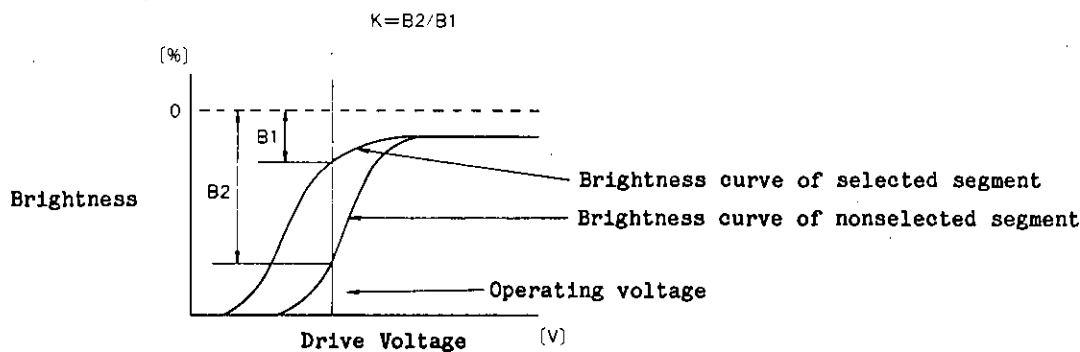
Electro-optical Characteristics at Ta=25°C, V_{DD}-V_{SS}=5V unless otherwise specified

		min	typ	max	unit
Input "High" Voltage	V _{IH}	2.2		5.0	V
Input "Low" Voltage	V _{IL}	0		0.6	V
Output "High" Voltage	V _{OH}	2.4			V
					DB0 to DB7, -I _{OH} =0.2mA
Output "Low" Voltage	V _{OL}			0.4	V
					DB0 to DB7, I _{OL} =1.2mA
Pull-up MOS Current	I _P	50	125	250	μA
					DB0 to DB7, RS, R/W
Current Dissipation	I _{DD}		1.5	3.0	mA
					No input/output current included
Oscillation Frequency	F _{OSC}	190	270	350	kHz
Viewing Angle	φ ₂ -φ ₁	20	30		degree
					K=1.4, θ=0°
Contrast Ratio	K	3.0			
					φ=20°, θ=0°
Rise Time	t _r		150	250	ms
Fall Time	t _f		150	250	ms
LCD Drive Voltage	V _{DD} -V _O	4.4	4.5	4.6	V
(Recommended Value)		4.0	4.1	4.2	V
1/16 duty		3.4	3.5	3.6	V
					Ta=0°C, φ=20°, θ=0°, K≥3
					Ta=25°C, φ=20°, θ=0°, K≥3
					Ta=50°C, φ=20°, θ=0°, K≥3

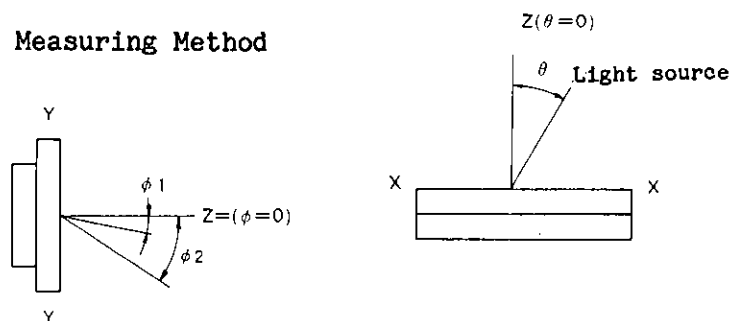
(1) Test Condition for Response Time (t_r, t_f)



(2) Definition of Contrast Ratio (K)



(3) Contrast Ratio Measuring Method



Angles ϕ and θ are defined as shown above.

The light source is placed in the θ direction at an angle of 30° and the sensor is placed in the ϕ direction to measure the contrast.

Pin Description

No.	Pin Name	Function
1	V _{SS}	(-) power supply pin 0V
2	V _{DD}	(+) power supply pin +5V
3	V _O	Pin for applying LCD drive voltage
4	RS	Input pin, HI=Data, LOW=Instruction
5	R/W	Input pin, HI=Read, LOW=Write
6	E	Input pin, Enable signal
7	DB0	Data bus line
8	DB1	
9	DB2	
10	DB3	
11	DB4	
12	DB5	
13	DB6	
14	DB7	
15	NC	

Timing Characteristics

			min	typ	max	unit
Enable Cycle Time		t_{cycE}	1000			ns
Enable Pulse Width	High level	PW_{EH}	450			ns
Enable Rise/Fall Time		t_{Er}, t_{Ef}			25	ns
Setup Time	RS, R/W, E	t_{As}	140			ns
Address Hold Time		t_{AH}	10			ns
Data Delay Time		t_{DDR}			320	ns
Data Setup Time		t_{DSW}	195			ns
Data Hold Time		$t_H(t_{DHR})$	10(20)			ns

Write Operation

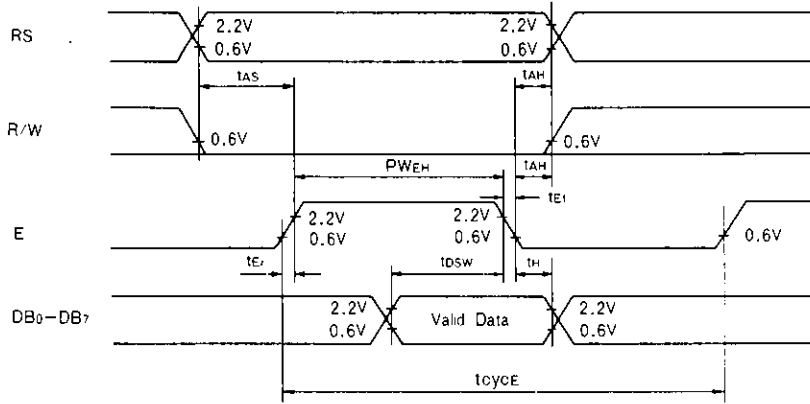


Fig. 1 Interface Timing (Data Write)

Read Operation

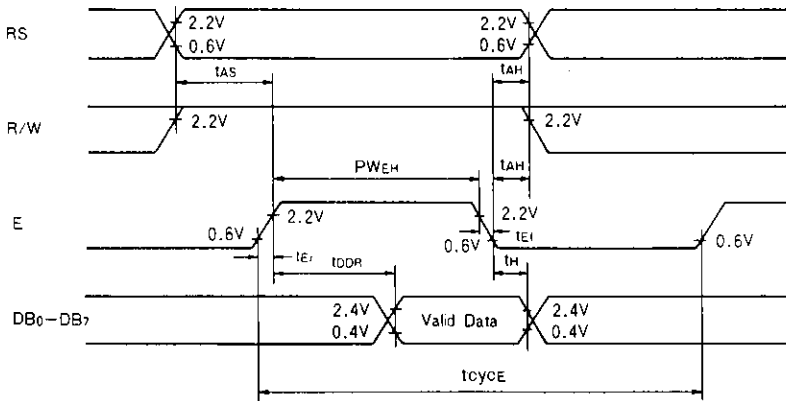


Fig. 2 Interface Timing (Data Read)

Table 1 Character Code

Hi-order 4 bits Low-order 4 bits	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)		0	a	P	^	P	-	9	3	e	e	P
xxxx0001	(2)	!	1	A	O	a	g	u	7	#	4	a	g
xxxx0010	(3)	"	2	B	R	b	r	T	i	u	x	P	e
xxxx0011	(4)	#	3	C	S	c	s	J	9	T	E	e	e
xxxx0100	(5)	\$	4	D	T	d	t	\	I	I	†	P	a
xxxx0101	(6)	%	5	E	U	e	u	.	*	†	1	e	0
xxxx0110	(7)	&	6	F	V	f	v	7	0	2	3	P	Z
xxxx0111	(8)	'	7	G	W	g	w	7	†	†	7	g	†
xxxx1000	(1)	(G	H	X	h	x	4	0	*	U	s	†
xxxx1001	(2))	9	I	Y	i	y	6	7	J	U	'	U
xxxx1010	(3)	*	#	J	Z	j	z	2	3	4	5	j	†
xxxx1011	(4)	+	;	K	L	k	l	(*	†	E	*	†
xxxx1100	(5)	,	<	L	*	I	l	†	3	7	7	e	†
xxxx1101	(6)	-	=	M	I	m	i)	2	†	†	†	†
xxxx1110	(7)	.	>	N	^	n	^	3	3	†	†	†	†
xxxx1111	(8)	/	?	O	_	o	_	†	w	y	7	†	†

(Note) The CG RAM is a character generator RAM used to store the character patterns that can be program-rewritten, as desired, by the user.

Table 2 Instruction Function

Instruction	Code										Contents	Execution Time ($f_{OSC}=250kHz$)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Display clear	0	0	0	0	0	0	0	0	0	1	Clears all display and returns the cursor to the home position (address 0).	82 μ s to 1.64ms
Cursor home	0	0	0	0	0	0	0	0	1	*	Returns the cursor to the home position (address 0). Also returns the display being shifted to the original position. The DD RAM contents remain unaffected.	40 μ s to 1.6ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor move direction and specifies whether or not to shift the display. These operations are performed during data write and read.	40 μ s
Display ON/OFF control	0	0	0	0	0	0	1	D	C	B	Sets all display ON/OFF(D), cursor ON/OFF(C), cursor position character blink (B).	40 μ s
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves the cursor and shifts the display without affecting the DD RAM contents.	40 μ s
Function set	0	0	0	0	1	DL	N	F	*	*	Sets the interface data length (DL), number of display lines (L), and character font (F).	40 μ s
CG RAM address set	0	0	0	1	ACG					Sets the CG RAM address. RAM data is sent/received after this setting.		40 μ s
DD RAM address set	0	0	1	ADD					Sets the DD RAM address. DD RAM data is sent/received after this setting.		40 μ s	
Busy flag/address read	0	1	BF	AC					Reads the contents of busy flag (BF) indicating internal operation is in progress and reads the contents of address counter.		1 μ s	
CG RAM/DD RAM data write	1	0	Write Data					Writes data into the DD RAM or CG RAM.		40 μ s		
CG RAM/DD RAM data read	1	1	Read Data					Reads data from the DD RAM or CG RAM.		40 μ s		
	I/D=1: Increment (+1) I/D=0: Decrement (-1) S=1: Accompanied by display shift S/C=1: Display shift S/C=0: Cursor move R/L=1: Right-shift R/L=0: Left-shift DL=1: 8 bits DL=0: 4 bits N=1: 2 lines N=0: 1 line F=1: 5 x 10 dots F=0: 5 x 7 dots BF=1: Internally operating BF=0: Possible to accept instruction										DD RAM: Display data RAM CG RAM: Character generator RAM ACG: CG RAM address ADD: DD RAM address Corresponds to cursor address. AC: Address counter used for both DD RAM and CG RAM.	The change in the frequency (f_{OSC}) also causes the execution time to be changed. (Example) When $f_{OSC}=270kHz$, $40\mu s \times \frac{250}{270}$ 37 μ s.

Fig. 3 Circuit Diagram DM1613

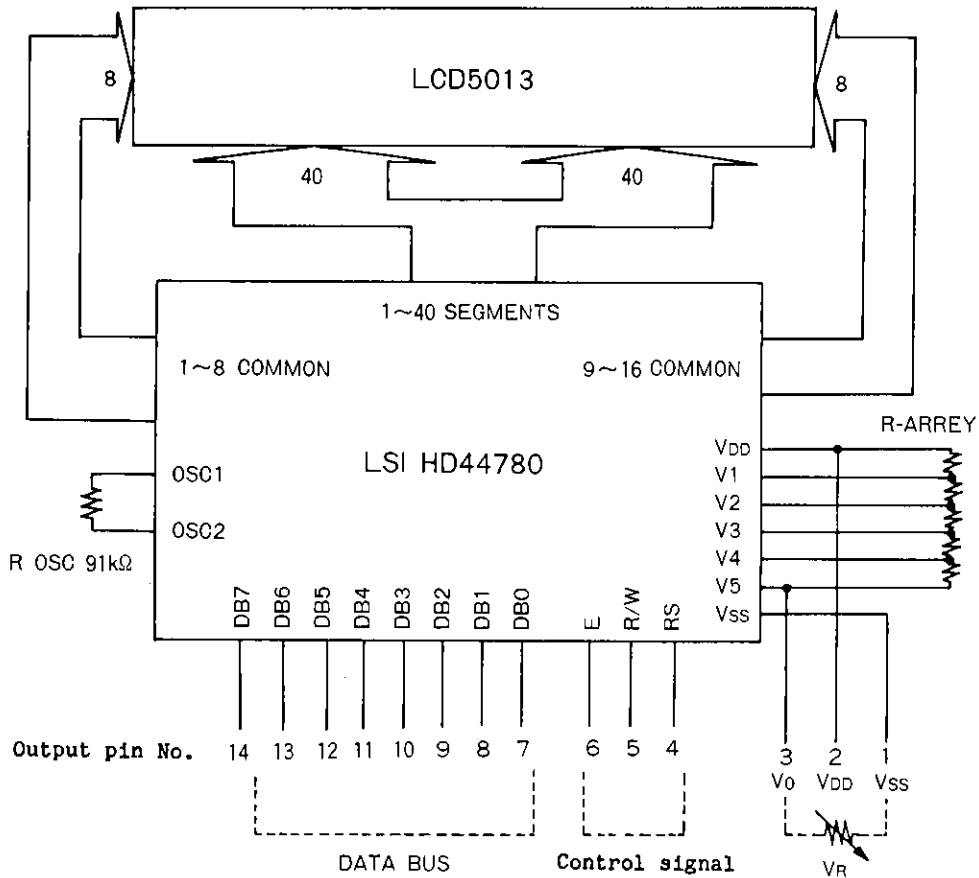
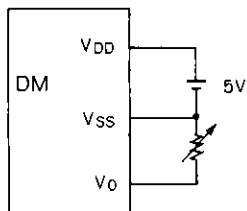


Fig. 4 Sample Power Supply



$V_{DD}-V_0$: LCD drive voltage
 The LCD drive voltage can be varied from approximately 3V to 5V by a variable resistor of 5kohms connected across V_{SS} and V_0 .

■ No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.

■ Anyone purchasing any products described or contained herein for an above-mentioned use shall:

- ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use;
- ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.

■ Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.