DM164

Version **:** *A.001*
Issue Date **:** *2007/09/04*
File Name **:** *SP-DM164-A.001.doc*
Total Pages **:** *28*

8x3-CHANNEL CONSTANT CURRENT LED DRIVER

新竹市科學園區展業一路 9 號 7 樓之 1
SILICON TOUCH TECHNOLOGY INC.
9-7F-1, Prosperity Road I, Science Based Industrial Park,
Hsin-Chu, Taiwan 300, R.O.C.
Tel：886-3-5645656 Fax：886-3-5645626

DM164

8x3-CHANNEL CONSTANT CURRENT LED DRIVERS

General Description

The DM164 is a LED current sink driver incorporating independent shift registers and data latches for grayscale PWM data (GD mode[*1]) and current adjustment data (D&G mode[*1]), 8x3-channels constant current circuitry with current value set by 3 external resistors, 65,536 grayscale PWM function unit, 128 levels current adjustment for each channel and 256 levels global brightness control (White balance). Each channel provides maximum current of 90mA. The DM164 also supports the LED open detection capability, thermal alarm and shutdown function. There are two methods to communicate error signals to the system. One is through serial output data to indicate which channel has failure. The other is by means of dedicated Alarm pin.

Features

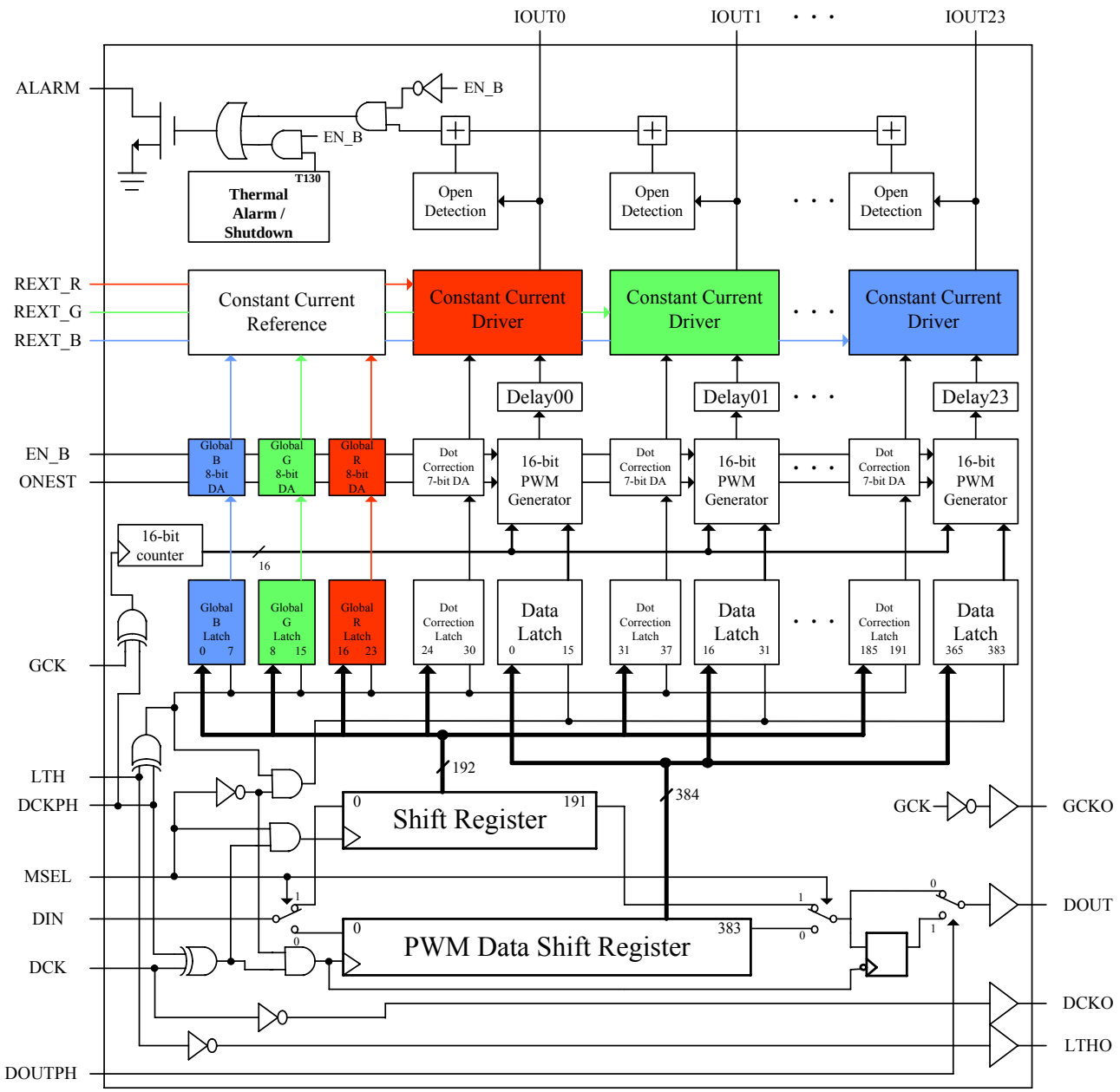
- Constant current outputs with current value set by 3 external resistors.
- Max PWM clock frequency
  Cascade: 36MHz@VDD=3.3V(Refresh rate≒550Hz), 40MHz@VDD=5V (610Hz)
- Max data clock frequency
  Cascade: 30MHz@VDD=3.3V, 35MHz@VDD=5V
- Maximum output current: 90mA
- Maximum output voltage: 17V
- 16-bit grayscale for each LED
- 8-bit current adjustment for global brightness control (White Balance)
- 7-bit current adjustment for each LED (Dot Correction)
- Supply Voltage: 3V to 5.5V
- LED Open Detection
- Thermal Alarm and Shutdown
  Alarm (junction temperature >130^{o}C)
  Shutdown (junction temperature > 170^{o}C)
- One-Shot Option
- Built-in Buffer for Data, PWM Clock, Latch signal and Data Clock
- Average Separate IOUT PWM Waveform Option

Package

- LQFP48 (7mmX7mm), QFN48 (7mmX7mm)

*1: See Page 10

Block Diagram

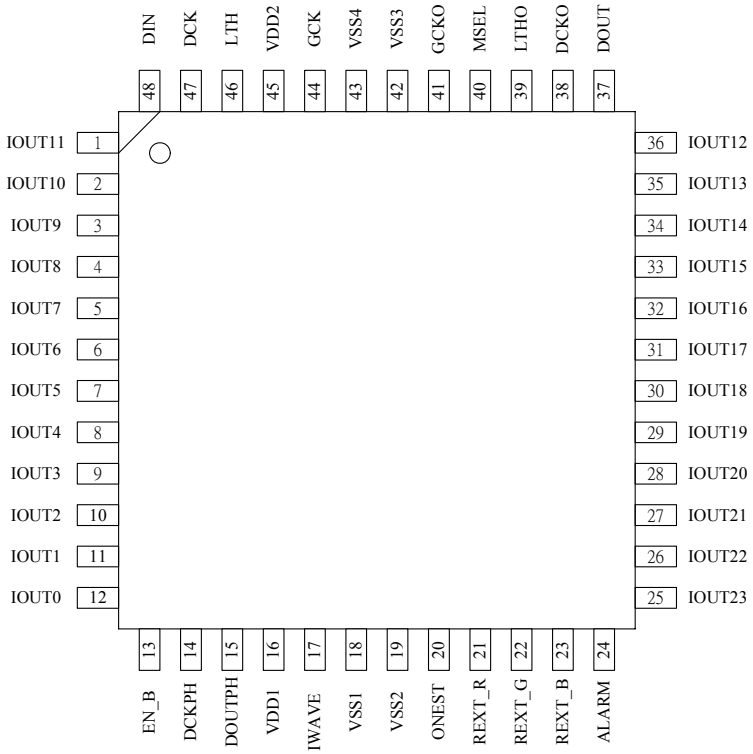


DISSIPATION RATINGS

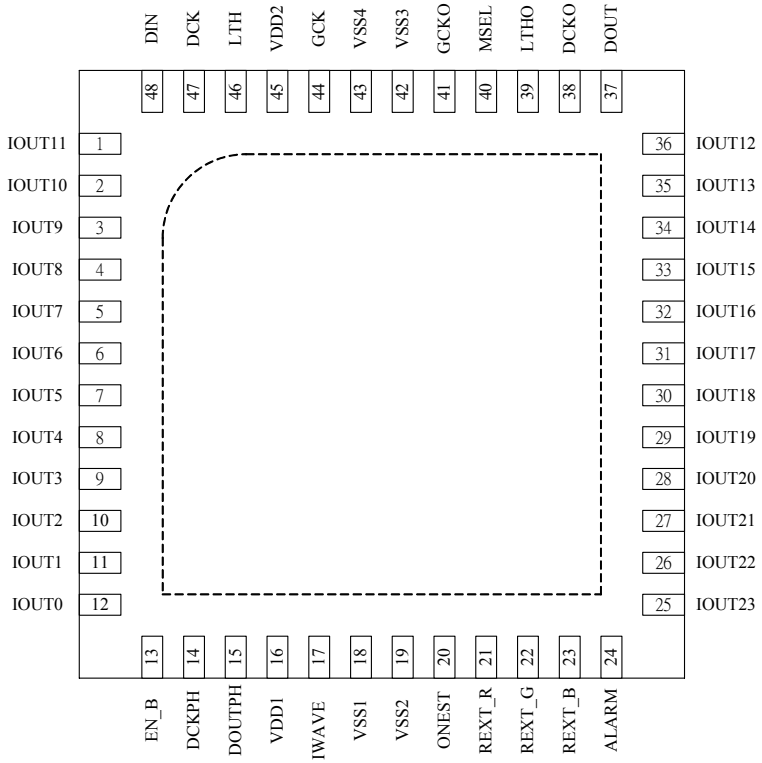
PACKAGE	POWER DISSIPATION (Tj_max=150 °C)	THERMAL RESISTANCE (Rja, Ta=25°C)
QFN48	4.00 W	31.22 °C/W
LQFP48	2.16 W	57.86 °C/W

Pin Description

LQFP48 (Top View)



QFN48 (Top View)



PIN NAME	*FUNCTION*	*QFN48 / LQFP48 pin number*
VDD1,VDD2	Power supply terminal.	16,45
VSS1~4	Ground terminal.	18,19,42,43
REXT_R REXT_G REXT_B	External resistor connected between REXT and GND for driver current setting. REXT_R controls outputs: IOUT0, 3, 6, 9, 12, 15, 18, 21. REXT_G controls outputs: IOUT1, 4, 7, 10, 13, 16, 19, 22. REXT_B controls outputs: IOUT2, 5, 8, 11, 14, 17, 20, 23.	21 22 23
IOUT0~11	LED driver outputs.	12,11,10,9,8,7, 6,5,4,3,2,1
IOUT12~23	LED driver outputs.	36,35,34,33,32,31 30,29,28,27,26,25
DIN	Serial input for grayscale PWM data and current adjustment data.	48
DOUT	Serial output for grayscale PWM data and current adjustment data.	37
DCK	Synchronous clock input for serial data transfer. The input data of DIN can be transferred at either the rising edges of DCK or the falling edges of DCK depending on the signal DCKPH.	47
DCKO	Synchronous clock output for serial data transfer. **DCKO=** $\overline{\text{DCK}}$ **.**	38
DCKPH	When DCKPH = L, input data is shifted in by rising edge of DCK, When DCKPH = H, input data is shifted in by falling edge of DCK	14
DOUTPH	When DOUTPH = H, DOUT is shifted out with half DCK cycle delay When DOUTPH = L, DOUT is shifted out without delay	15
LTH	Data latch input pin. When DCKPH=L & LTH=H or DCKPH=H & LTH=L, internal latches become transparent and PWM counter value will be set to FFFF(h). When DCKPH=L & LTH=L or DCKPH=H & LTH=H, internal latches hold data.	46
LTHO	Data latch output pin. **LTHO=** $\overline{\text{LTH}}$	39
GCK	Clock input for PWM operation. When DCKPH=L (DCKPH=H), the internal PWM counter will count up with rising (falling) edge of GCK.	44

GCKO	Clock output. **GCKO=**$\overline{GCK}$	41
EN_B	Blank all outputs. When EN_B = H, all outputs are forced OFF. When EN_B = L, all outputs are controlled by grayscale PWM control.	13
MSEL	When MSEL = H, the device is operated in Dot Correction Data & Global Brightness Control Data Input Mode (D&G mode). When MSEL = L, the device is operated in Grayscale PWM Data Input Mode (GD mode).	40
ALARM	Output open drain terminal for an alarm function. when EN_B = L, It will go low as LED open when EN_B = H, It will go low as chip overheated.	24
IWAVE	When IWAVE = H, traditional Iout waveform. When IWAVE = L, average separate Iout waveform.	17
ONEST	When ONEST = H, one-shot function is enabled. When ONEST = L, one-shot function is disabled.	20

Maximum Ratings (Ta=25°C, Tj(max) = 150°C)

CHARACTERISTIC	SYMBOL	RATING					UNIT
Supply Voltage	V_{DD}	-0.3 ~ 7.0					V
Input Voltage	V_{IN}	-0.3 ~ V_{DD}+0.3					V
Output Current	I_{OUT}	90					mA
Output Voltage	V_{OUT}	-0.3 ~ 17					V
DCK Frequency	F_{DCK}	Cascade	Vdd=5V	35	Vdd=3.3V	30	MHz
GCK Frequency	F_{GCK}	Cascade	Vdd=5V	40	Vdd=3.3V	36	MHz
GND Terminal Current	I_{GND}	2200					mA
Power Dissipation	P_D	4.00 (QFN48); 2.16 (LQFP48) (Ta=25°C)					W
Thermal Resistance	$R_{th(j-a)}$	31.22 (QFN48); 57.86 (LQFP48)					℃/W
Operating Temperature	T_{op}	-40 ~ 85					℃
Storage Temperature	T_{stg}	-55 ~ 150					℃

Recommended Operating Condition

DC Characteristics (Ta = 25°C)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	—	3	—	5.5	V
Output Voltage	V_{OUT}	—	—	—	17	V
Output Current	I_O	OUTn	—	—	90	mA
	I_{OH}	SERIAL-OUT	—	—	—	
	I_{OL}	SERIAL-OUT	—	—	—	
Input Voltage	V_{IH}	—	0.7 V_{DD}	—	V_{DD}+0.2	V
	V_{IL}	—	-0.2	—	0.3 V_{DD}	

AC Characteristics (V_{DD} = 5.0 V, Ta = 25°C, REXT = 3.9kΩ)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
DCK Frequency	FDCK	Cascade operation	—	—	35	MHz
DCK pulse duration	Twhdk / Twldk	High or low level	—	13	—	ns
DCK rise/fall time	Trdk/ Tfdk	Single, CLoad=13pF	—	5	—	ns
GCK Frequency	FGCK	Cascade operation	—	—	40	MHz
GCK pulse duration	Twhgk / Twlgk	High or low level	—	12	—	ns
GCK rise/fall time	Trgk/ Tfgk	Single, CLoad=13pF	—	5	—	ns
Set-up Time for DIN	Tsu0	Before DCK rising edge	—	10	—	ns
Hold Time for DIN	Th0	After DCK rising edge	—	10	—	ns
Set-up Time for DCK	Tsu1	Before LTH falling edge	—	30	—	ns
LTH Pulse Width	TwLTH	—	—	15	—	ns
Set-up Time for LTH	Tsu2	Before GCK rising edge	—	10	—	ns
Set-up Time for MSEL	Tsu3	Before DCK rising edge	—	10	—	ns
Hold Time for MSEL	Th3	After DCK rising edge	—	30	—	ns

AC Characteristics (V_{DD} = 3.3 V, Ta = 25°C, REXT = 3.9kΩ)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
DCK Frequency	FDCK	Cascade operation	—	—	30	MHz
DCK pulse duration	Twhdk / Twldk	High or low level	—	15	—	ns
DCK rise/fall time	Trdk/ Tfdk	Single, CLoad=13pF	—	4	—	ns
GCK Frequency	FGCK	Cascade operation	—	—	36	MHz
GCK pulse duration	Twhgk / Twlgk	High or low level	—	13	—	ns
GCK rise/fall time	Trgk/ Tfgk	Single, CLoad=13pF	—	4	—	ns
Set-up Time for DIN	Tsu0	Before DCK rising edge	—	10	—	ns
Hold Time for DIN	Th0	After DCK rising edge	—	10	—	ns
Set-up Time for DCK	Tsu1	Before LTH falling edge	—	30	—	ns
LTH Pulse Width	TwLTH	—	—	15	—	ns
Set-up Time for LTH	Tsu2	Before GCK rising edge	—	10	—	ns
Set-up Time for MSEL	Tsu3	Before DCK rising edge	—	10	—	ns
Hold Time for MSEL	Th3	After DCK rising edge	—	30	—	ns

See Page 9: Timing Diagram

Electrical Characteristics (V_{DD} = 5.0 V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION		MIN.	TYP.	MAX.	UNIT
Input Voltage "H" Level	V_{IH}	—		0.7 V_{DD}	—	V_{DD}	V
Input Voltage "L" Level	V_{IL}	—		GND	—	0.3 V_{DD}	
Output Leakage Current	I_{leak}	V_{OUT} = 17 V		—	—	±0.1	uA
Output Voltage (DOUT)	V_{OL}	I_{OL} = 2 mA		—	—		V
	V_{OH}	I_{OH} = -2 mA			—	—	
Output Current (Channel-Channel)	I_{OL1}	V_{OUT} = 1.0V R_{EXT} = 3.9kΩ		—	±1	±3	%
Output Current (Chip-Chip)	I_{OL3}	V_{OUT} = 1.0V R_{EXT} = 3.9kΩ		—	—	±6	%
Output Voltage Regulation	% / Vout	R_{EXT} = 3.9kΩ Vout = 1.0~3.0V		—	±0.1	±0.5	% / V
Supply Current[1]	$I_{DD, analog}$	VDD=5.0V, R_{EXT} = 3.9kΩ		—	13	—	mA
		, R_{EXT} = 1.4kΩ		—	34	—	
		VDD=3.3V, R_{EXT} = 3.9kΩ		—	12	—	
		, R_{EXT} = 1.4kΩ		—	33	—	
	$I_{DD, digital}$	Cload=2pF, DCK=GCK=10MHz	VDD=5.0V	—	2.4	—	
			VDD=3.3V	—	1.8	—	

Switching Characteristics (V_{DD} = 5.0V, Ta = 25°C)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
DOUT Rise time	t_r	VIH=VDD VIL=GND	—	5	10	ns
DOUT Fall time	t_f	REXT=3.9kΩ CL=13pF	—	5	10	ns
IOUT Rise time	t_r	VIH=VDD, VIL=GND REXT=3.9kΩ	—	8	30	ns
IOUT Fall time	t_f	VLED=5.0V RL=100Ω, CL=33pF 10% to 80%	—	8	30	ns

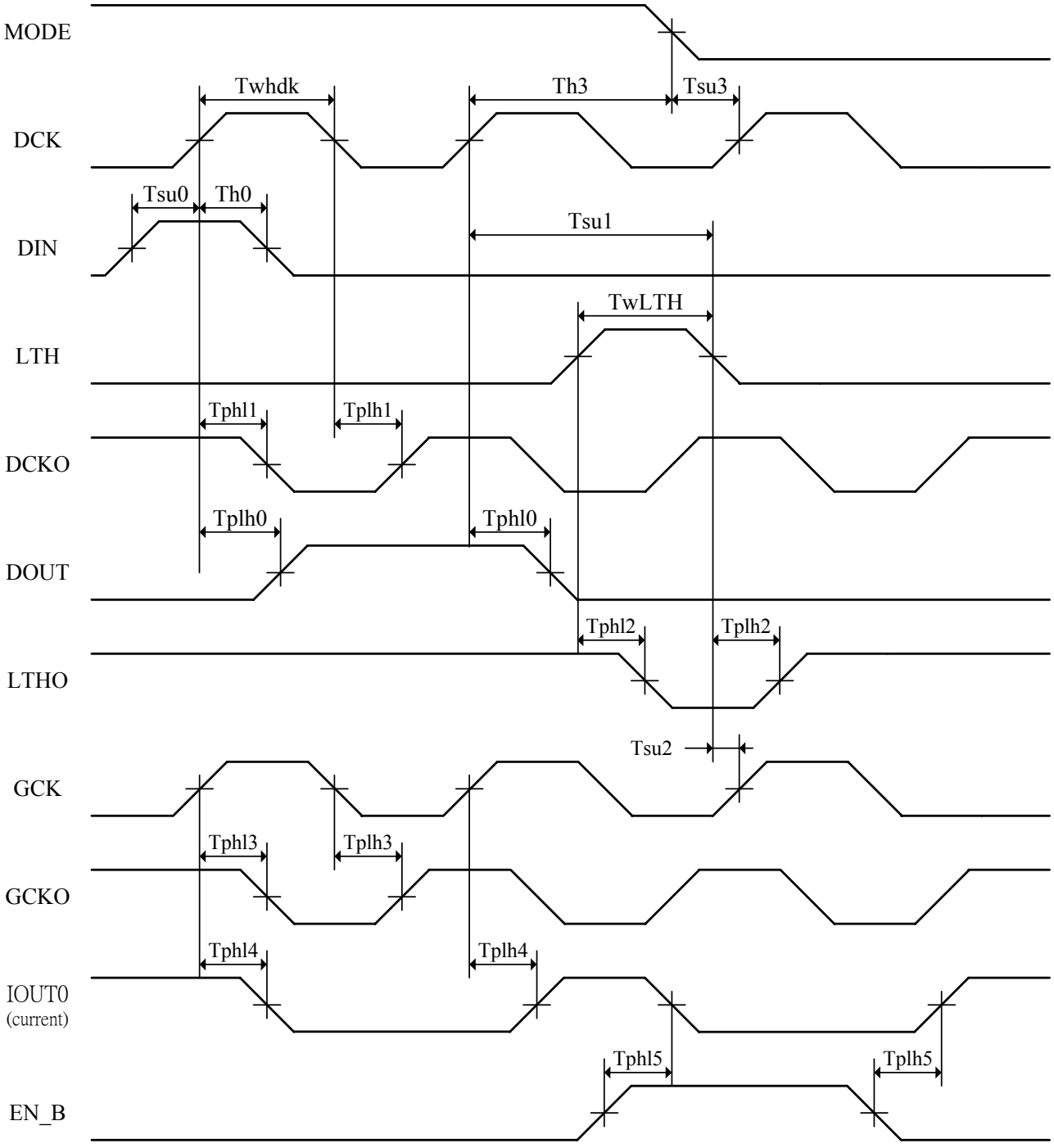
DOUT	Tplh0	After DCK rising edge	—	28	—	ns
DOUT	Tphl0	After DCK rising edge	—	28	—	ns
DCKO	Tplh1	After DCK falling edge	—	14	—	ns
DCKO	Tphl1	After DCK rising edge	—	17	—	ns
LTHO	Tplh2	After LTH falling edge	—	14	—	ns
LTHO	Tphl2	After LTH rising edge	—	17	—	ns
GCKO	Tplh3	After GCK falling edge	—	16	—	ns
GCKO	Tphl3	After GCK rising edge	—	16	—	ns
IOUT0 (turn on)	Tplh4	After GCK rising edge	—	30	—	ns
IOUT0 (turn off)	Tphl4	After GCK rising edge	—	31	—	ns
IOUT0 (turn on)	Tplh5	After EN_B falling edge	—	27	—	ns
IOUT0 (turn off)	Tphl5	After EN_B rising edge	—	25	—	ns

Switching Characteristics (V_{DD} = 3.3V, Ta = 25°C)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
DOUT Rise time	t_r	VIH=VDD VIL=GND REXT=3.9kΩ CL=13pF	—	4	10	ns
DOUT Fall time	t_f		—	4	10	ns
IOUT Rise time	t_r	VIH=VDD, VIL=GND REXT=3.9kΩ VLED=5.0V RL=100Ω, CL=33pF 10% to 80%	—	12	30	ns
IOUT Fall time	t_f		—	12	30	ns

DOUT	Tplh0	After DCK rising edge	—	35	—	ns
DOUT	Tphl0	After DCK rising edge	—	35	—	ns
DCKO	Tplh1	After DCK falling edge	—	21	—	ns
DCKO	Tphl1	After DCK rising edge	—	19	—	ns
LTHO	Tplh2	After LTH falling edge	—	20	—	ns
LTHO	Tphl2	After LTH rising edge	—	20	—	ns
GCKO	Tplh3	After GCK falling edge	—	23	—	ns
GCKO	Tphl3	After GCK rising edge	—	23	—	ns
IOUT0 (turn on)	Tplh4	After GCK rising edge	—	42	—	ns
IOUT0 (turn off)	Tphl4	After GCK rising edge	—	41	—	ns
IOUT0 (turn on)	Tplh5	After EN_B falling edge	—	39	—	ns
IOUT0 (turn off)	Tphl5	After EN_B rising edge	—	33	—	ns

Timing Diagram



Serial Data Interface

The DM164 includes a flexible data transfer interface. The data can be transferred from DIN pin to the shift registers at either the rising edge of DCK or the falling edge of DCK depending on the signal DCKPH. After all data are clocked in, a high level LTH signal can transfer the serial data to the data latches (Level Sensitive). The serial data format can be 192-bit or 384-bit wide, depending on the operating mode of the device.

Operating Modes

The DM164 has two operating modes depending on the signal MSEL. Table 1 shows the available operating modes. When MSEL = H, the device operates at the D&G mode. D&G mode is used to set dot correction data and global brightness control data after IC power up or any time. When MSEL = L, the device becomes GD mode. GD mode is used to set grayscale PWM data after D&G mode.

Table 1. Two Operating Modes

MSEL	MODE	SHIFT REGISTER
H	Dot Correction Data & Global Brightness Control Data Input Mode (D&G mode)	192-bit
L	Grayscale PWM Data Input Mode (GD mode)	384-bit

D&G Mode Data Format

At D&G mode, dot correction data of all channels and global brightness control data of different colors are transferred into the chip at the same time. The complete dot correction data format consists of 24 x 7-bit and the global brightness control data of three different colors consists of 3 x 8-bit. The total shift registers width at D&G mode is 192-bit. All data is clocked in with MSB first. Figure 1 shows the D&G mode data format.

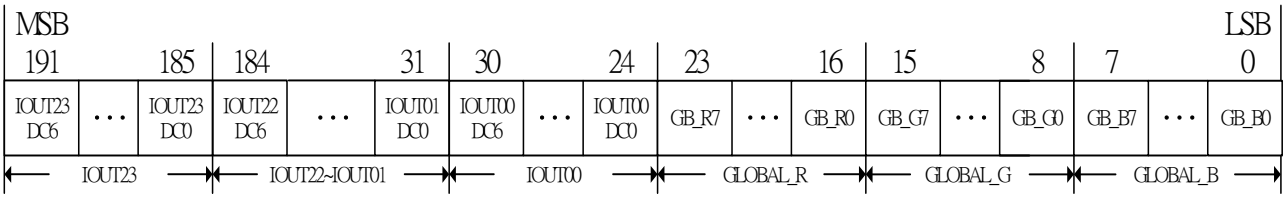


Figure 1. D&G Mode Data Format (D&G[191:0])

To operate the DM164 in D&G mode, MSEL must be set to high. The shift register width is then set to 192-bit wide. The input data can be transferred at either the rising edge of DCK

or the falling edge of DCK by setting DCKPH to L or H. After all data are transferred into the D&G mode shift registers, the D&G mode data can be latched from shift registers to the data latches by a LTH signal at either D&G mode or GD mode. Figure 2 shows the D&G mode data input timing chart.

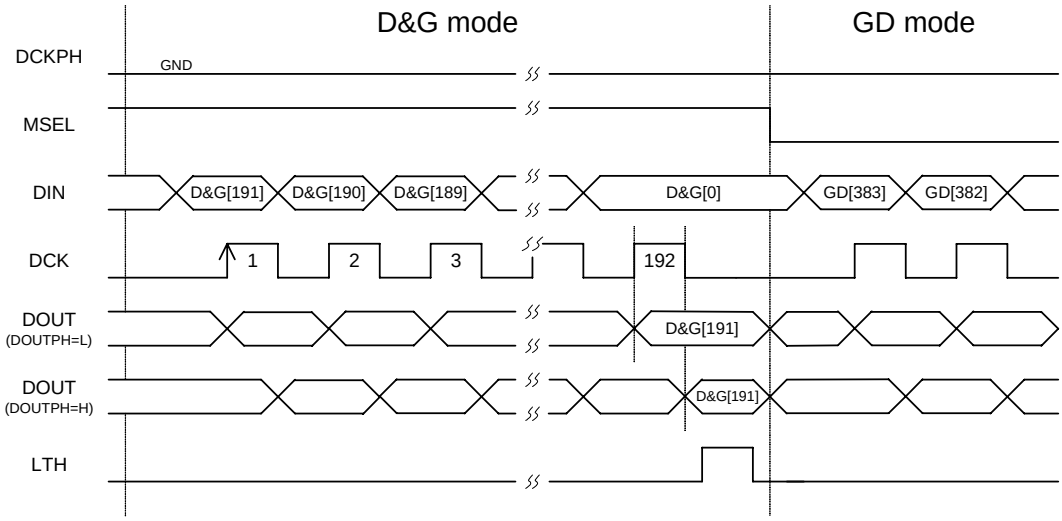


Figure 2. D&G Mode Data Input Timing Chart

GD Mode Data Format

At GD mode, the grayscale PWM data will be transferred to the shift registers. The complete grayscale PWM data format consists of 24 x 16-bit. The total shift registers width at GD mode is 384-bit. All grayscale PWM data is clocked in with MSB first. Figure 3 shows the GD mode data format.

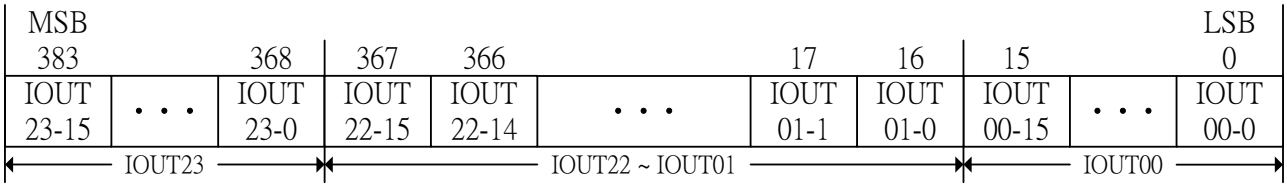


Figure 3. GD Mode Data Format (GD[383:0])

When MSEL is set to low, the DM164 enters GD mode. The internal shift registers changes to 384-bit wide. The input data can be transferred at either the rising edge of DCK or the falling edge of DCK by setting DCKPH to L or H. After all data are transferred into the GD mode shift registers, the GD mode data can be latched from shift registers to the data latches by a LTH signal at GD mode only. Figure 4 shows the GD mode data input timing chart.

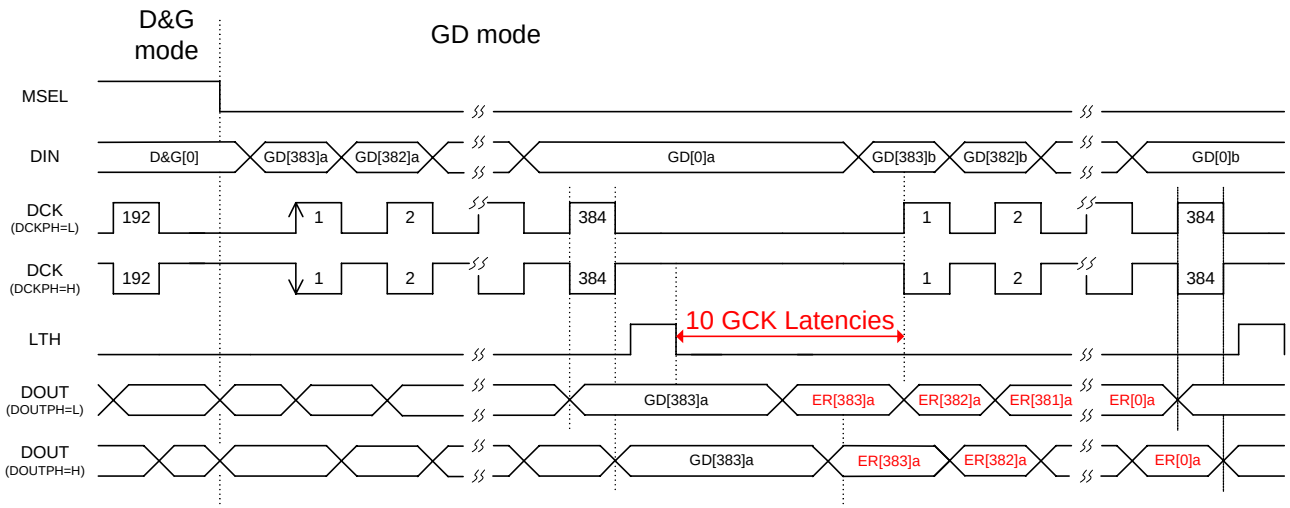


Figure 4. GD Mode Data Input Timing Chart

Thermal Alarm and Shutdown

The DM164 provides a temperature error detection circuit, when EN_B=H and the junction temperature of the IC reaches about 130°C, a T130 signal will change the ALARM pin to low level. At this moment, the system should start up the fan or decrease the output currents to lower the junction temperature. If the system has not any protected circuit, the junction temperature might continue to rise. Once it reaches approximately above 170°C, a T170 signal and a Shutdown signal will cause the driver to shutdown all the outputs, the ALARM pin remains in low level. Basically, the IC will cool down and return to the safe operating temperature approximately below 130°C. When the operating temperature below 130°C, the ALARM pin will reset to high level, disable the warning, and restart all the outputs. Operation in the thermal situation for a long time may cause chip damage permanently. The thermal error signals (T130, T170, Shutdown) can be transferred out from DOUT pin.

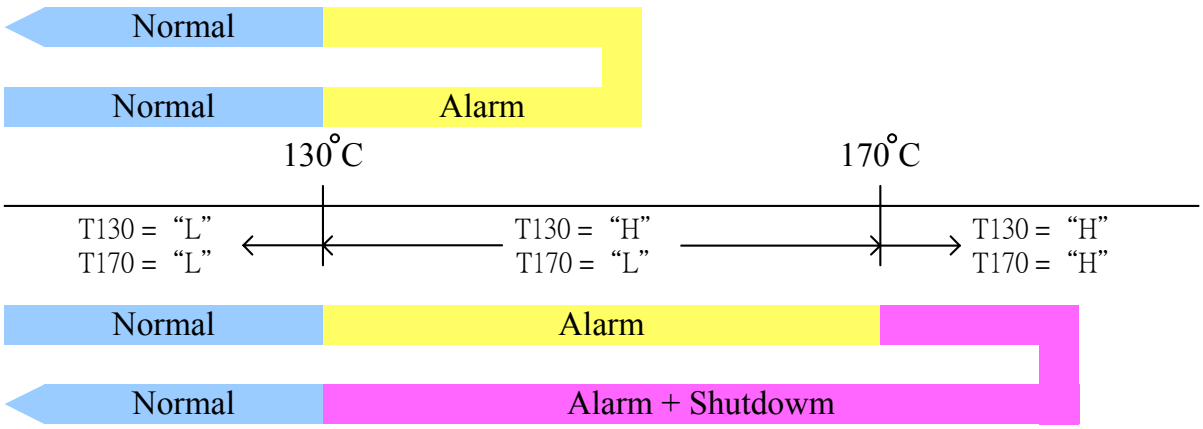


Figure 5. Thermal Alarm and Shutdown

Open Detection

If there is any one of the 24 LEDs open or disconnected, the DM164 can detect and report the error. The open detection circuit works when the following two conditions are met simultaneously:

1. IOUTn is on (IOUTn > 200ns and EN_B="L").
2. When the output voltage at IOUTn is less than 0.2 V

The open error signal (OPE) has two methods to communicate the error signals to the system. One is through serial output data to indicate which channel has failure (OPEn=H => IOUTn is open). The other is by means of dedicated Alarm pin when EN_B=L.

Status Information Output

When the DM164 operates at GD mode, after the LTH signal latches the input data from shift registers to the data latches, the shift registers data will be replaced by the status information. The status information includes the thermal error signals (Shutdown, T130 and T170,), open error signals (OPE) and dot correction data (DC), which will be transferred out from DOUT pin. Figure 6 shows the status information format.

(a. IOUT shut down => Shut down=L, **b.** Tj>130℃ => T130=H, **c.** Tj>170℃ => T170=H**)**

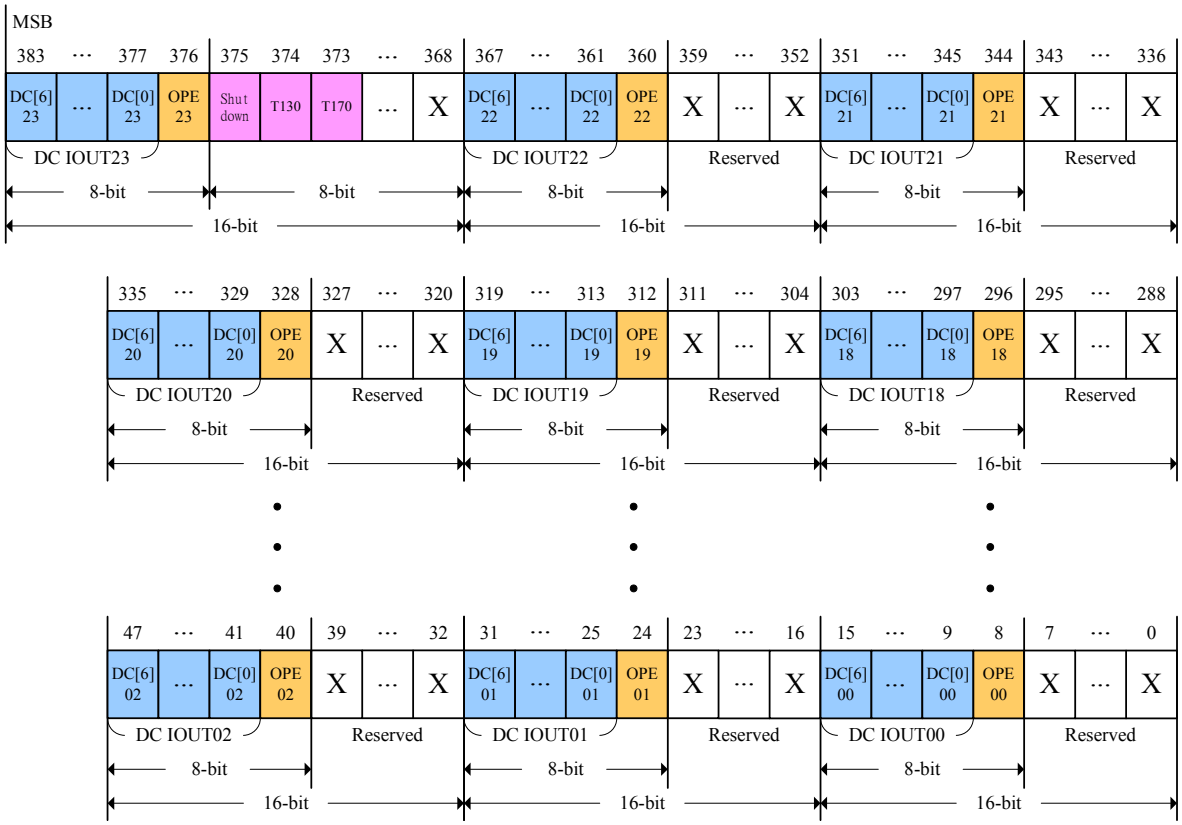


Figure 6. Status Information Data Format (ER[383:0])

In order to catch correct open error signals. DCK must wait for at least 10 GCK latencies after the LTH signal latches the input data. Figure 7 shows the timing chart.

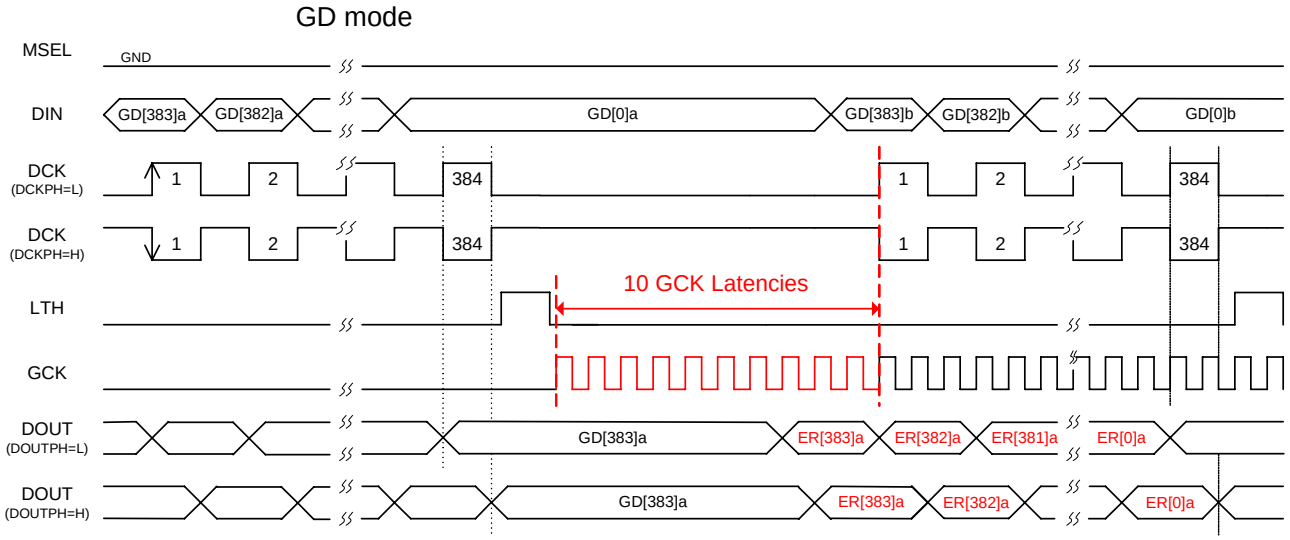


Figure 7. Open Error Signals Timing Chart

IOUT Delay & EN_B Delay

The DM164 provides delay circuits between IOUTs. All IOUTs are divided into eight groups and every three outputs of different colors form a group. For example, IOUT0 IOUT1 and IOUT2 form the group1; IOUT3 IOUT4 and IOUT5 form the group2. The delay time between every group is half GCK cycle time. Each IOUT delay in the same group is 5ns (typical). Figure 8 shows the IOUT delay timing chart. Besides the iout delay, the EN_B is also associated with GKC signal. When EN_B goes high and GCK keeps going, then each group of IOUTs will turn off one by one depending on the GCK sequence. If EN_B goes high but GCK stops going, then the IOUTs will not turn off normally.

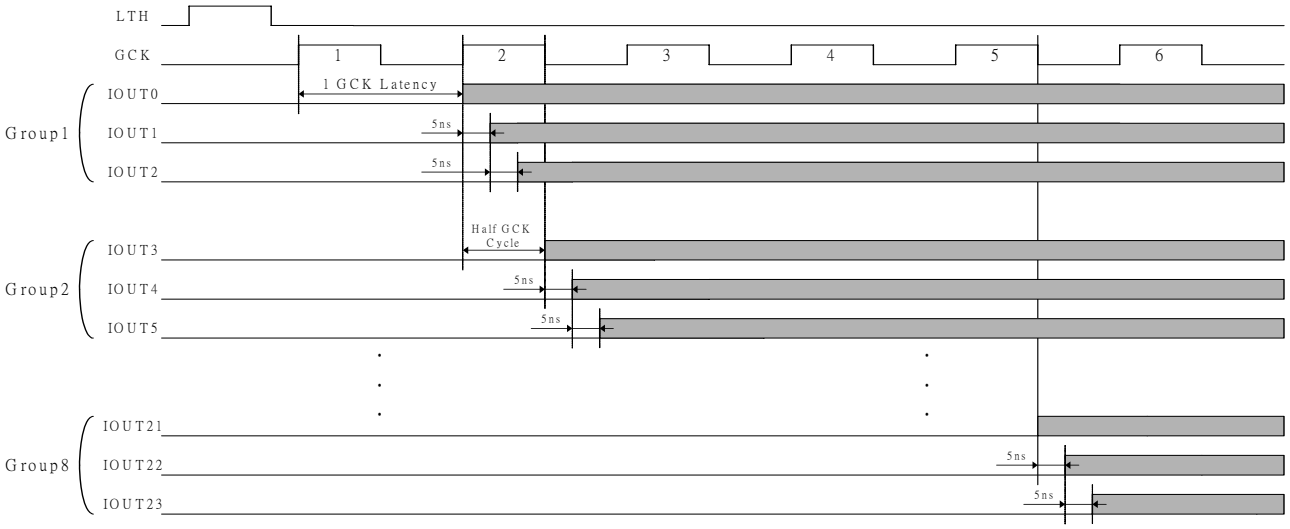
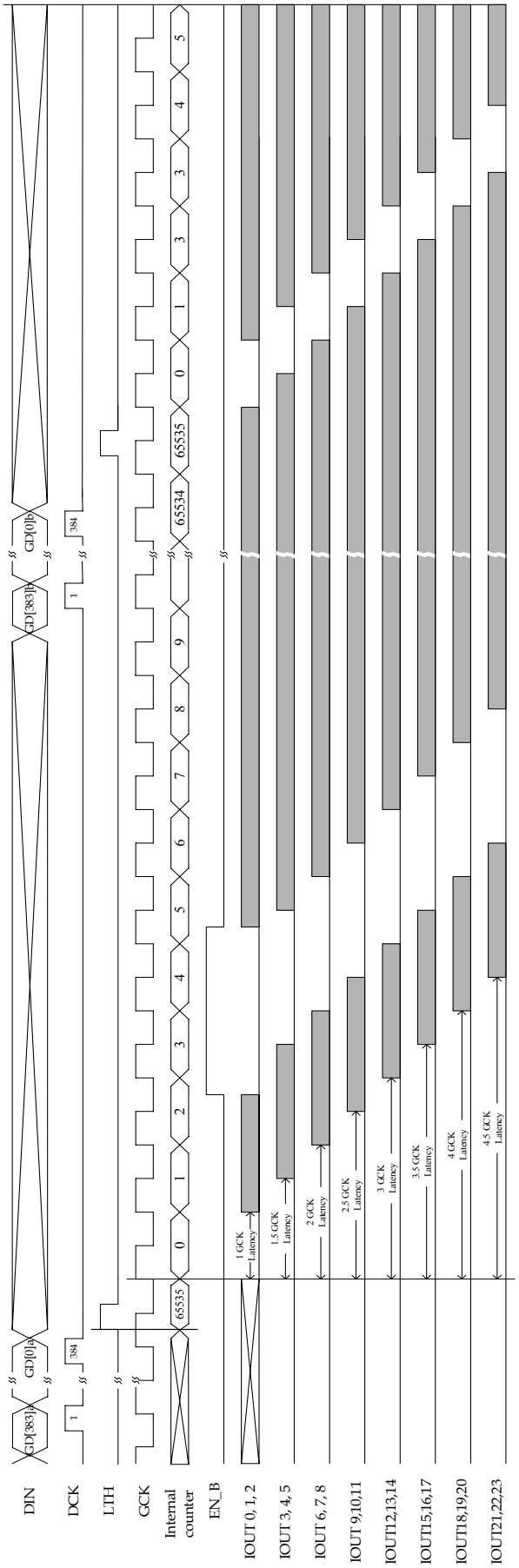


Figure 8. IOUT Delay Timing Chart

Iout Delay & EN_B Delay Waveform



One-Shot Option

The DM164 provides an option that users can make the output turn on for just a PWM cycle time, i.e. in the GD mode, after a LTH signal, the output only turn on for 65536 T_{GCK} time. After 65536 T_{GCK}, the output will automatically turn off. This is called One-Shot function. Figure 9 shows the difference between One-Shot or not. When ONEST = H, one-shot function is enabled. The output will just turn on at 1_{st} PWM cycle. When ONEST = L, one-shot function is disabled. The output will repeat at every PWM cycle.

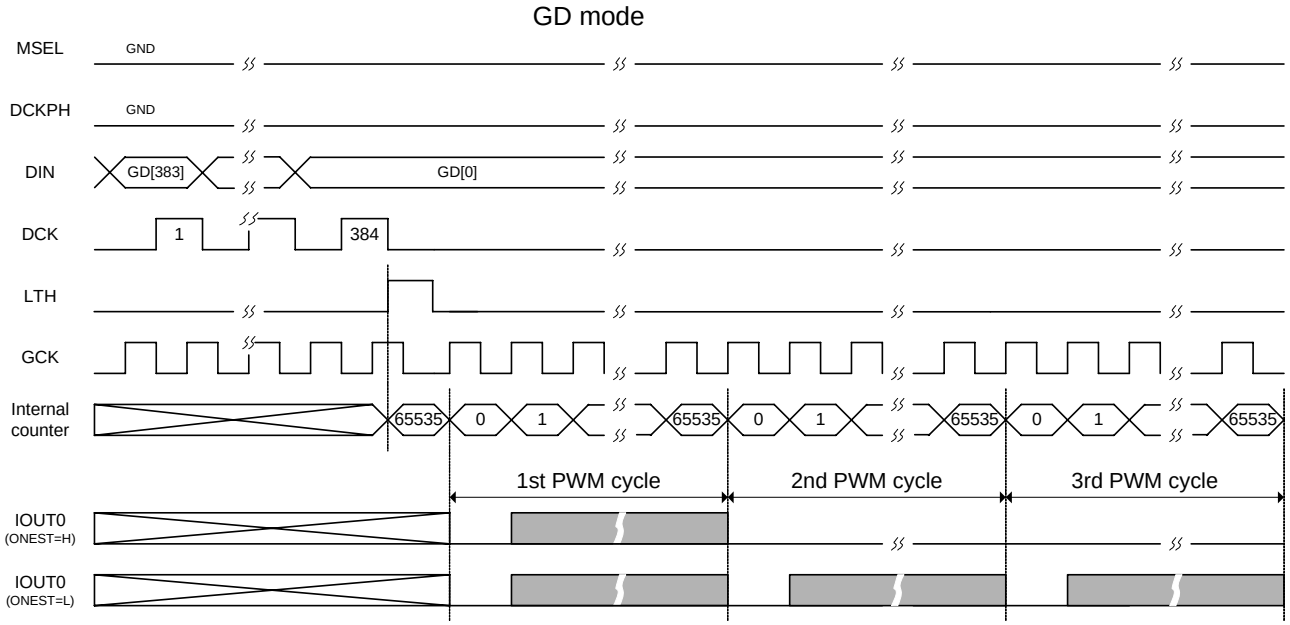


Figure 9. One-Shot Operation

Grayscale PWM Operation

When DCKPH=L, the grayscale PWM cycle starts with the falling edge of LTH (see Figure 10). A LTH = H signal will set the 16-bit PWM counter value to FFFFh. The first GCK pulse after LTH increases the PWM counter by one and switches on all IOUT with grayscales value not zero. Each following rising edge of GCK increases the PWM counter by one. The DM164 compare the grayscale PWM value of each output IOUT with grayscale counter value. If the grayscale PWM value is larger than grayscale counter value, the IOUT will switch on.

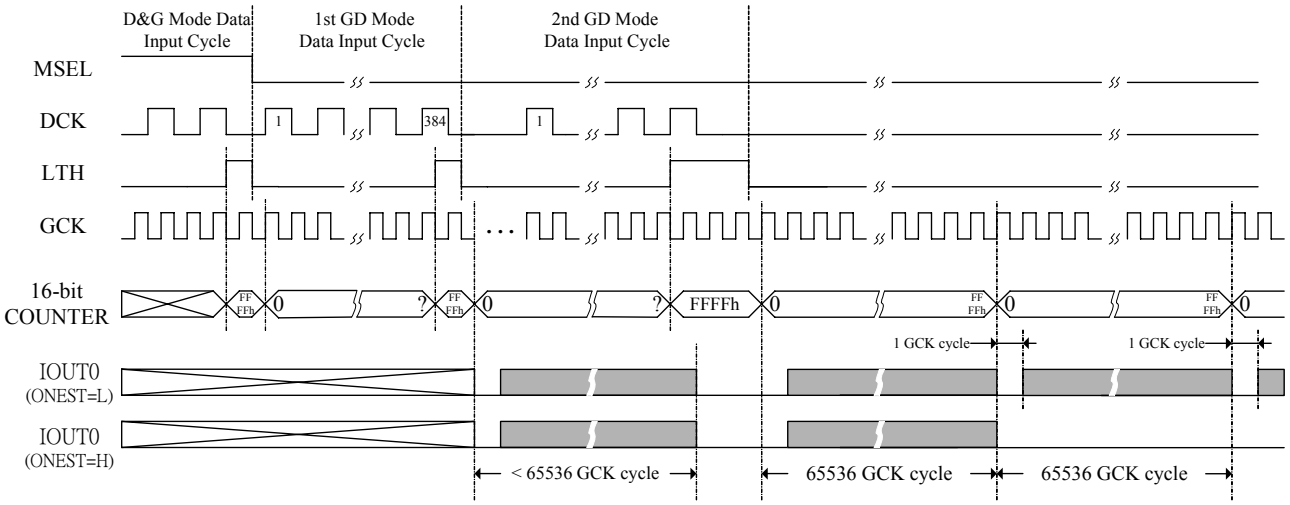


Figure 10. Grayscale PWM Operation

Maximum Output Current

The maximum output current is set by an external resistor. The resistor is connected between Rext and GND. Varying the resistor value can adjust the current scale ranging from 5mA to 90mA. The reference voltage of REXT terminal (Vrext) is approximately 1.23V. The maximum output current (I_{max}) value can be calculated roughly by the following equation:

$$\text{Imax} \cong \frac{\text{Vrext (V)}}{\text{Rrext } (\Omega)} \times 64$$

where:
Vrext = 1.23V
Rrext = external resistor.

Global Brightness Control

The global brightness control function can adjust the global current of each color independently. The output current (I_{global}) can be adjusted in 256 steps from ((1/256)*100)% to 100% of the maximum output current. The following equation can calculate the global brightness control current (I_{global})

$$\text{Iglobal} \cong \frac{\text{GB+1}}{256} \times \text{Imax}$$

where:
I_{max} = the maximum output current.
GB = the global brightness control value for different colors.

Dot Correction

Besides global brightness control, the DM164 also has the capability to adjust the output current of each channel IOUT00 to IOUT23 independently. The output current (I_{dot}) can be adjusted in 128 steps from ((1/128)*100) % to 100% of the global brightness control current. The following equation can calculate the dot correction current (I_{dot})

$$Idot \cong \frac{DC+1}{128} \times Iglobal \cong \frac{DC+1}{128} \times \frac{GB+1}{256} \times Imax$$

where:

I_{global} = the global brightness control current

DC = the dot correction value for each output.

Average Separate IOUT Waveform

The DM164 incorporates a different PWM counter, hence the IOUT waveform demonstrate a very different characteristics compare to conventional PWM counter. In the DM164, when IWAVE="L," the IOUT waveform is averagely divided into 32(maximum) sections. Figure 11 shows the difference between traditional IOUT waveform and particular IOUT waveform.

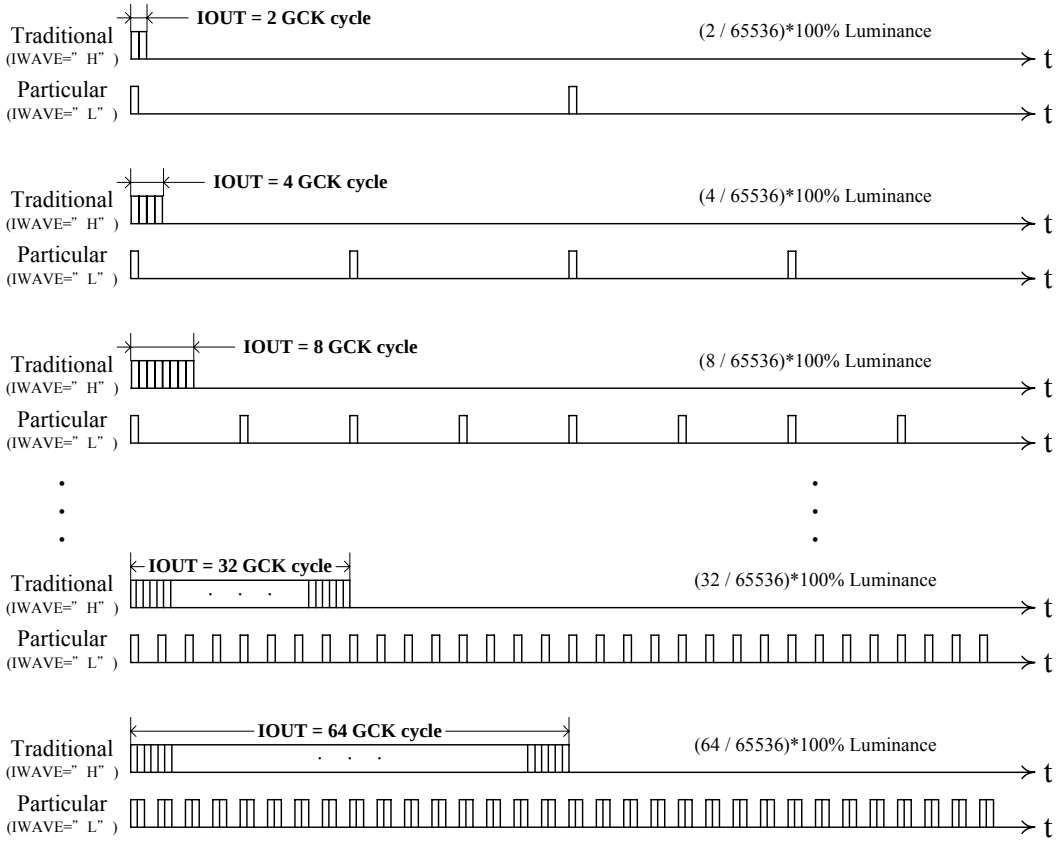
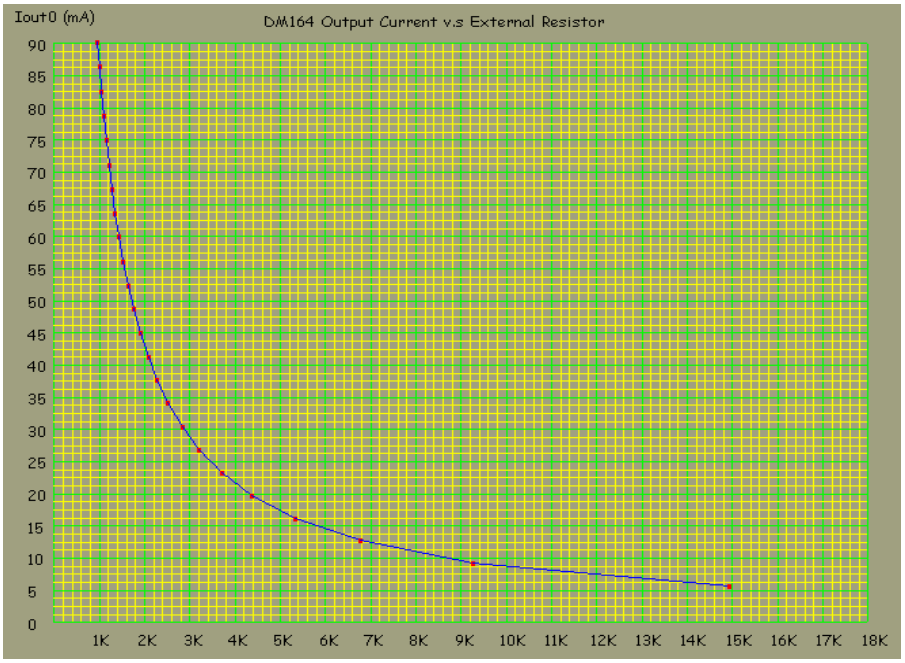
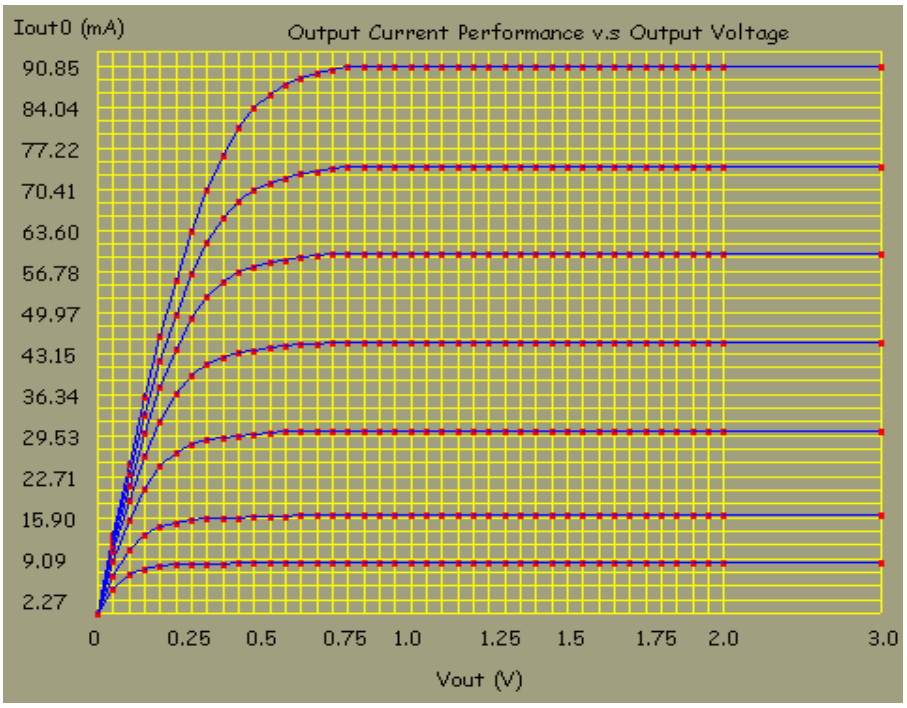


Figure 11. Average Separate IOUT Waveform

Output Current vs. External Resistor



Output Current Performance vs. Output Voltage



Application Diagram

a) DCK LTH and GCK signals: **Global Connected**

* Each DCKPH input pin of all chips should be connected to the same voltage level. Figure 12 shows that all DCKPH pins are connected to VSS.

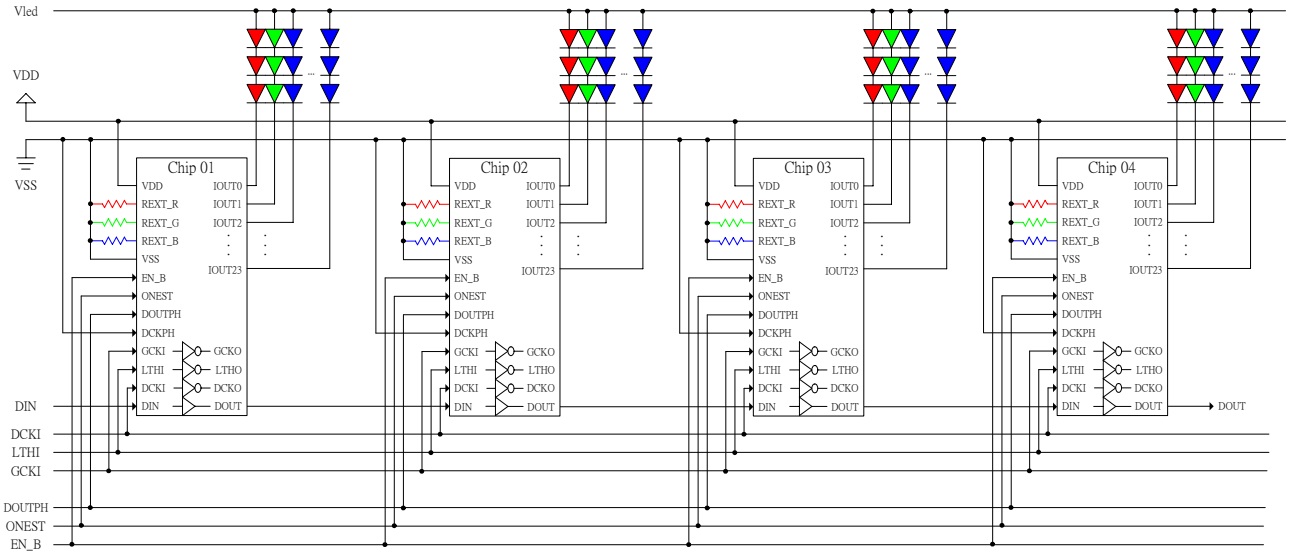


Figure 12. DCK LTH and GCK signals: Global Connected

b) DCK LTH and GCK signals: **Cascade Connected**

* DCKPH input pins of odd stages (Chip01, Chip03…) and even stages (Chip02, Chip04…) should be connected to different voltage level. Figure 13 shows that CLKPH pins of odd stages are connected to VSS, and CLKPH pins of even stages are connected to VDD.

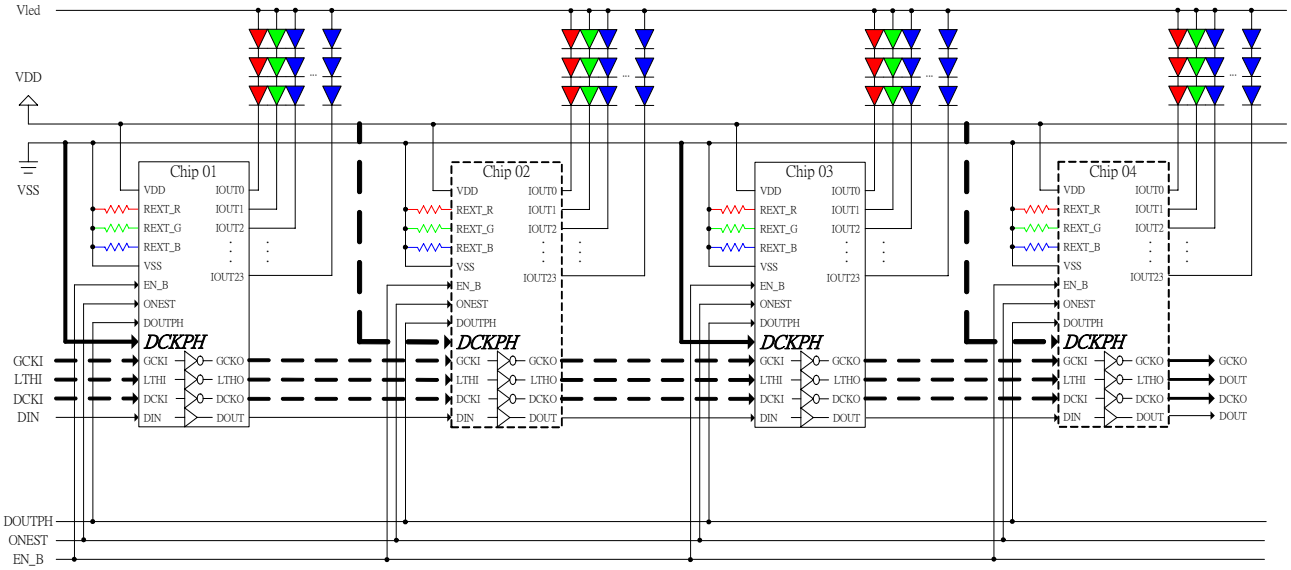
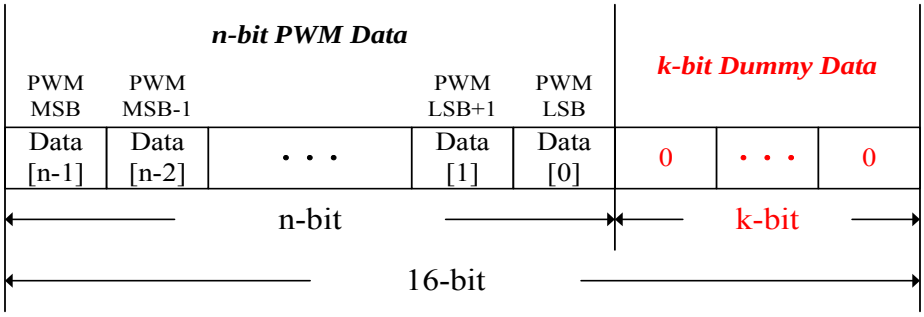


Figure 13. DCK LTH and GCK signals: Cascade Connected

c) 10~15-bit PWM Grayscale Application

When the DM164 operates at n-bit PWM grayscale application, where n is less than 16. The 16-bit GD mode data format of each channel is showed below:



The k-bit LSB of 16-bit GD mode data of each channel must be filled with all “0”. (k=16-n)

For example:

When the DM164 operates at 14-bit PWM grayscale application, the 2-bit LSB of the 16-bit GD mode data must be filled with “0”. The 16-bit data format is showed below:

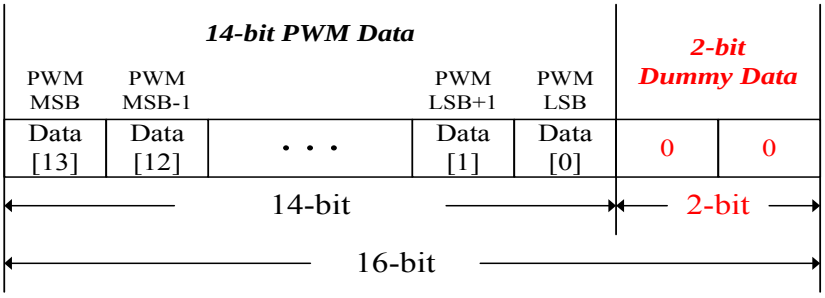


Figure 14 shows the timing diagram when the DM164 operates at n-bit PWM grayscale application. The frame cycle of n-bit PWM grayscale application can be controlled by GCK and LTH signals.

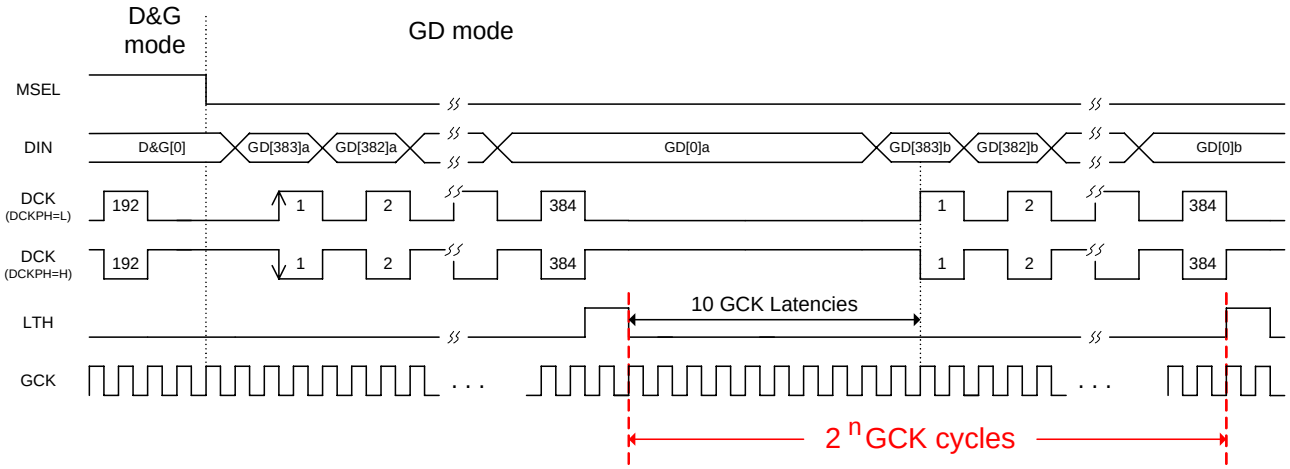
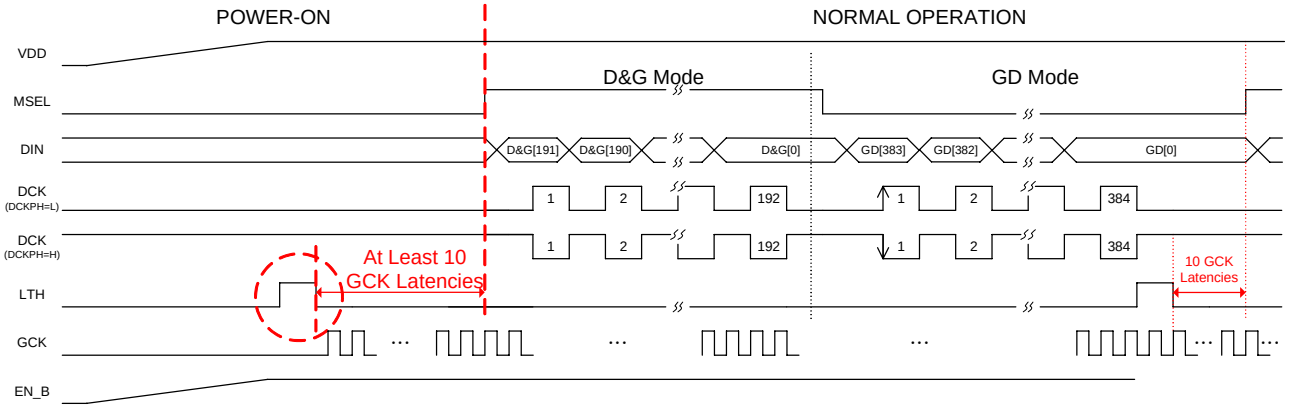


Figure 14. Operating at n-bit PWM Grayscale Application Timing Diagram

d) Power-on Reset Suggestion

The DM164 doesn't built-in automatic power-on reset function. In order to make sure the DM164 can work normally after the power-on situation. Users can add an LTH pulse before normal operation, like Figure 15 shows.

a. D&G Mode First



b. GD Mode First

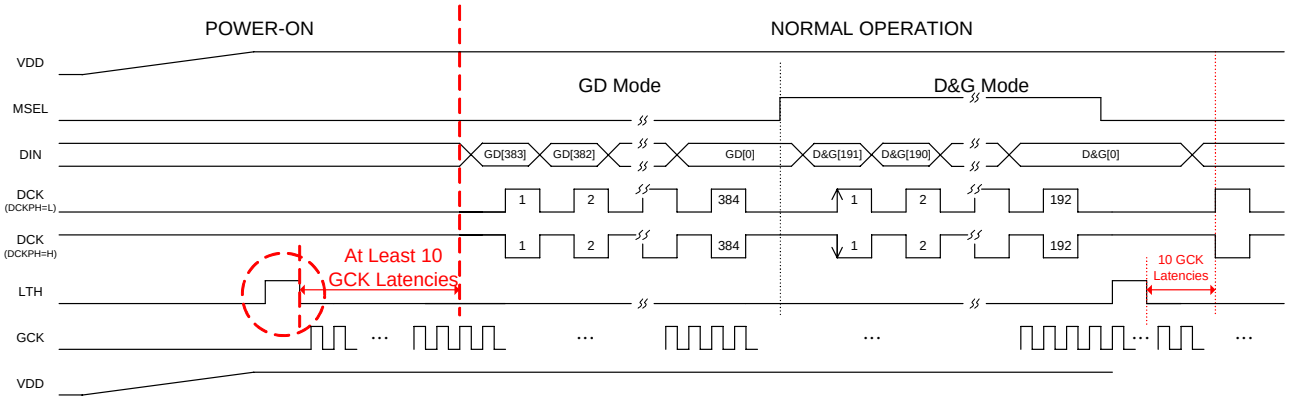
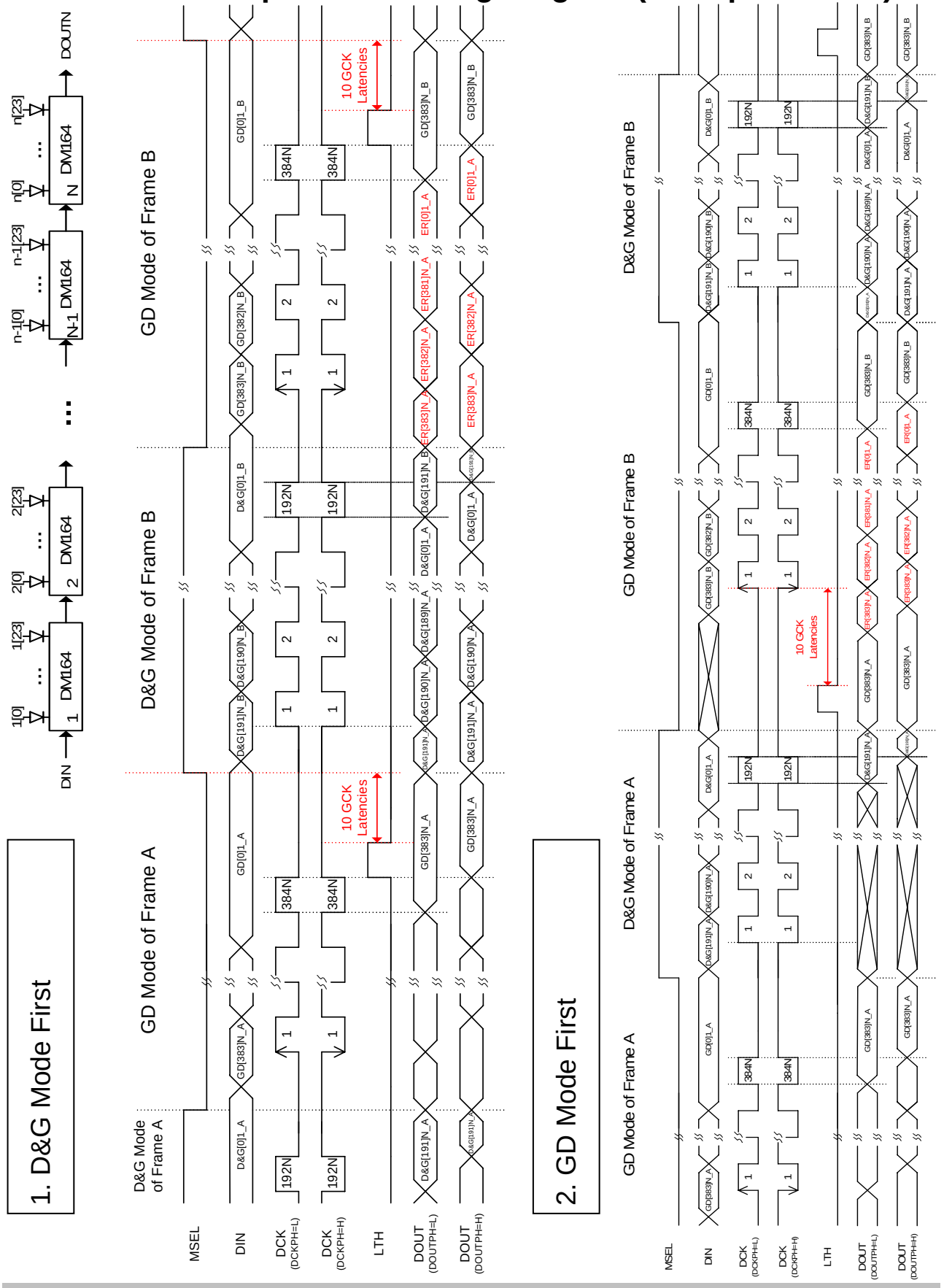


Figure 15. Power-on Reset Suggestion Timing Diagram

Mode Transfer Operation Timing Diagram (N Chip Cascade)

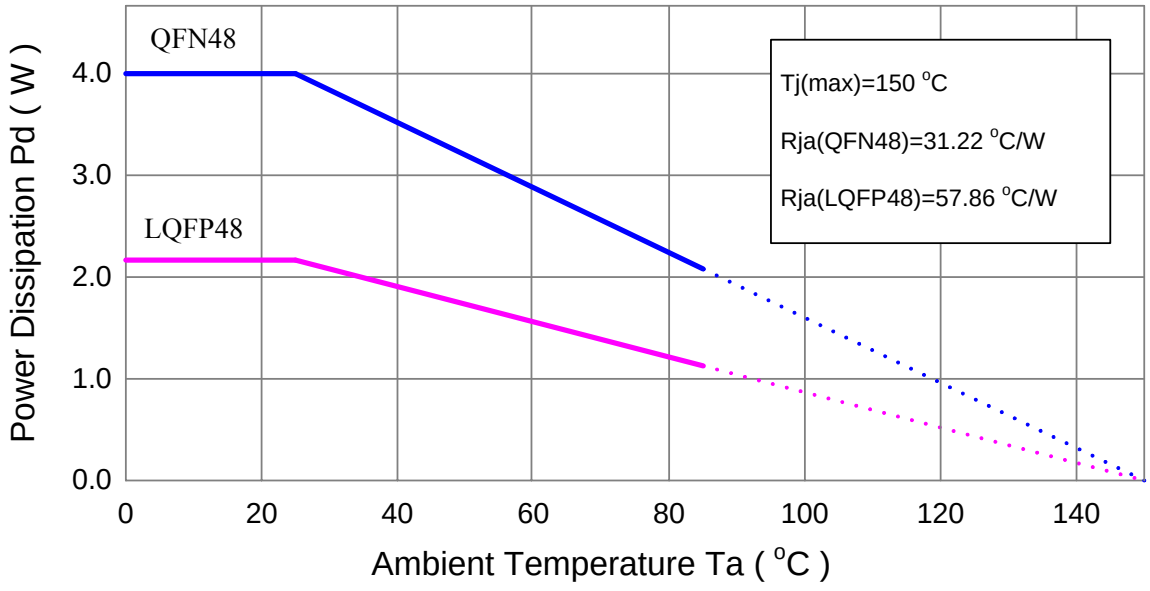


Power Dissipation

The power dissipation of a semiconductor chip is limited to its package and ambient temperature, in which the device requires the maximum output current calculated for given operating conditions. The maximum allowable power consumption can be calculated by the following equation:

$$Pd(max)(Watt) = \frac{Tj(junction\ temperature)(max)(^{\circ}C) - Ta(ambient\ temperature)(^{\circ}C)}{Rth(junction\text{-}to\text{-}air\ thermal\ resistance)(^{\circ}C/Watt)}$$

The relationship between power dissipation and operating temperature can be refer to the figure below:

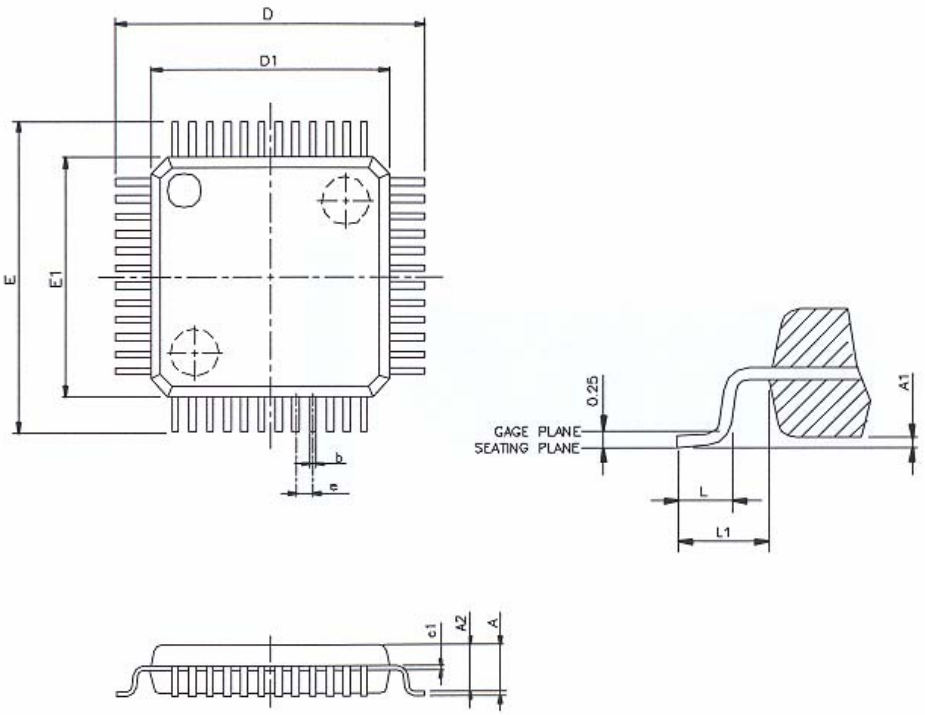


Based on the Pd(max), the maximum allowable voltage of output terminal can be determined by the following equation:

$$Vout0 \times Iout0 \times Duty0 + \ldots + Vout23 \times Iout23 \times Duty23 < Pd(max) - VDD \times IDD$$

Package Outline Dimension

LQFP48

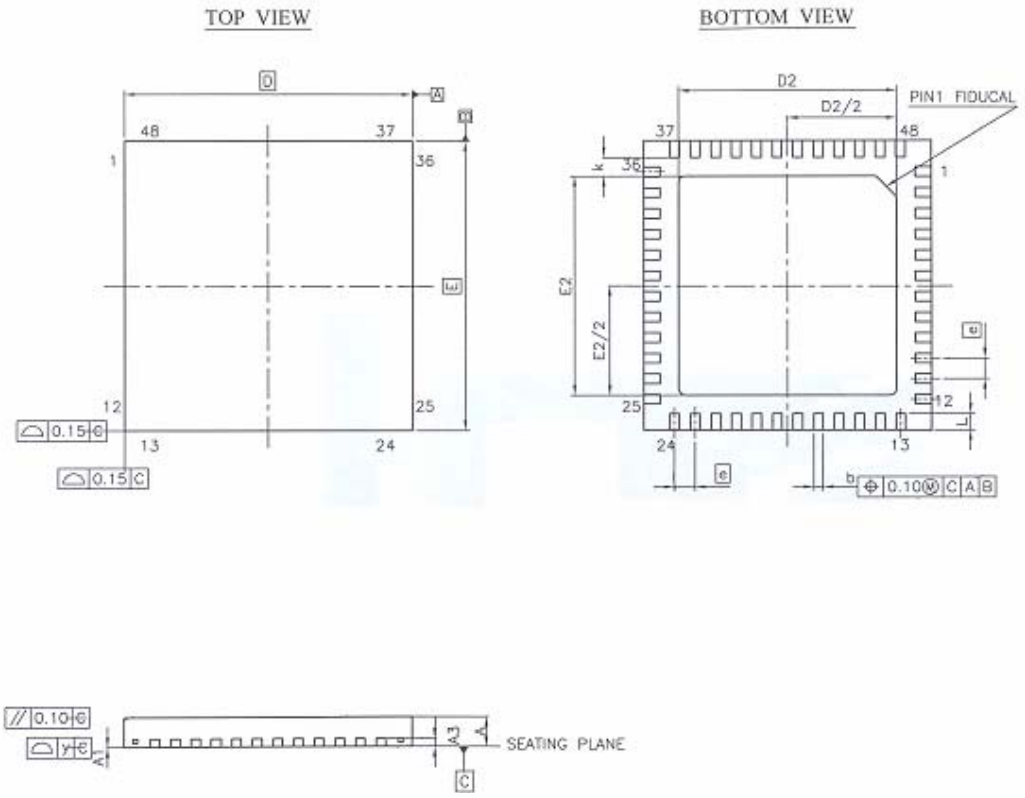


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

NOTES:
1. JEDEC OUTLINE: MS-026 BBC
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS IMCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

QFN48



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	27.6	29.5	31.5
A1	0	0.02	0.05	0	0.79	1.97
A3	0.203 REF			8 REF		
b	0.18	0.23	0.30	7.1	9.1	11.8
D	7.00 BSC			276 BSC		
D2	5.10	5.30	5.50	201	209	217
E	7.00 BSC			276 BSC		
E2	5.10	5.30	5.50	201	209	217
e	0.50 BSC			19.7 BSC		
k	0.20			7.9		
L	0.30	0.40	0.50	11.8	15.7	19.7

NOTE:
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. REFER TO JEDEC STD. MO-220 WKKD-2
3. DIMENSION "b" APPLINES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL TIP.
4. LEADFRAME MATERIAL IS OLIN194 AND THICKNESS IS 0.203mm (8 MIL)

The products listed herein are designed for ordinary electronic applications, such as electrical appliances, audio-visual equipment, communications devices and so on. Hence, it is advisable that the devices should not be used in medical instruments, surgical implants, aerospace machinery, nuclear power control systems, disaster/crime-prevention equipment and the like. Misusing those products may directly or indirectly endanger human life, or cause injury and property loss.

Silicon Touch Technology, Inc. will not take any responsibilities regarding the misusage of the products mentioned above. Anyone who purchases any products described herein with the above-mentioned intention or with such misused applications should accept full responsibility and indemnify. Silicon Touch Technology, Inc. and its distributors and all their officers and employees shall defend jointly and severally against any and all claims and litigation and all damages, cost and expenses associated with such intention and manipulation.