

Features

- **Military and Extended Temperature Range**
 - -55°C to +125°C, Operation (Military)
 - -40°C to +85°C, Operation (Extended)
 - 0°C to +70°C, Operation (Commercial)
- **End of Write Detection**
 - Optional DATA Polling Feature
- **High Endurance Write Cycles**
 - 2816A: 10,000 Cycles/Byte Minimum
 - 5516A: 100K, 400K and 1 Million Cycles/Byte
- **On-Chip Timer**
 - Automatic Erase and Write Time Out
- **All Inputs Latched by Write or Chip Enable**
- **5 V ± 10% Power Supply**
- **Power Up/Down Protection Circuitry**
- **150 ns max. Access Time**
- **Low Power Operation**
 - 100 mA max. Active Current
 - 40 mA max. Standby Current
- **JEDEC Approved Byte-Wide Pinout**
- **MIL-STD-883 Class B Compliant**

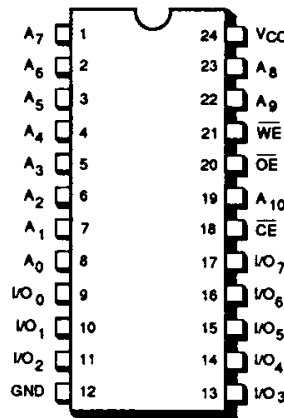
Description

SEEQ's 2816A/5516A are 5V only, 2Kx8 electrically erasable programmable read only memories (EEPROMs). EEPROMs are ideal for applications which require non-volatility and in-system data modification. The endurance, the minimum number of times that a byte may be written, is 10 thousand (K) for the 2816A, and 100K, 400K or 1 million cycles for the 5516A. The 5516A's high endurance was accomplished using SEEQ's proprietary oxynitride EEPROM process and its innovative Q Cell™ design. The 2816A/5516A is ideal for systems that require frequent updates.

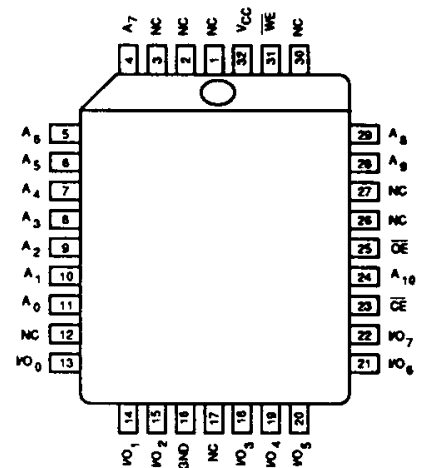
There is an internal timer that automatically times out the write time. A separate erase cycle is not required and the minimum write enable (\overline{WE}) pulse width needs to be as little as 100 ns depending on device address access time.

Pin Configuration

DUAL-IN-LINE
TOP VIEW

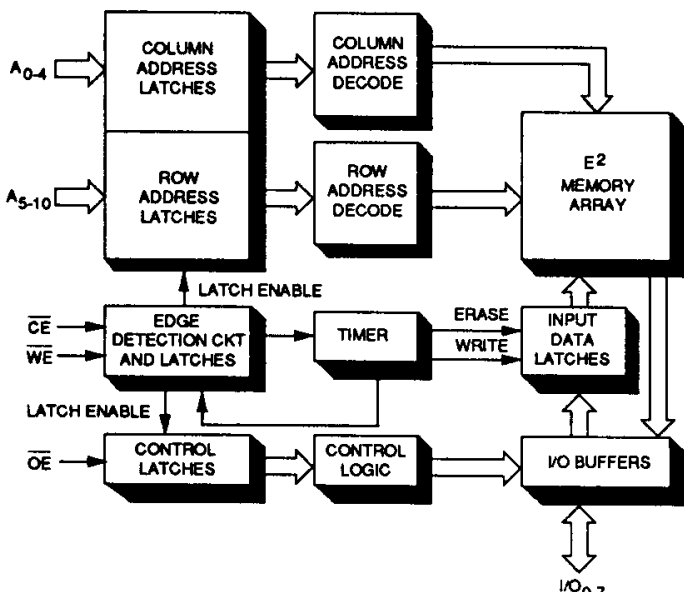


PLASTIC LEADED
CHIP CARRIER TOP VIEW



NOTE: For PLCC - Ready/Busy pin option is always connected unless otherwise specified.

Block Diagram



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Pin Names

| | |
|---------------------------------|---|
| A ₀ -A ₁₀ | ADDRESSES |
| \overline{CE} | CHIP ENABLE |
| \overline{OE} | OUTPUT ENABLE |
| \overline{WE} | WRITE ENABLE |
| I/O ₀₋₇ | DATA INPUT (WRITE OR ERASE) DATA OUTPUT (READ) |

**2816A/2816AH
5516A/5516AH**

The on-chip timer, along with the inputs being latched by a write or chip enable signal edge, frees the microcomputer system for other tasks during the write time. The standard 2816A/5516A's write time is 10 ms, while the 2816AH/5516AH write time is a fast 2ms. Once a byte is written, it can be read in a maximum of 150 ns. The inputs are TTL for both the byte write and read mode.

Device Operation

There are five operational modes (see Table 1) and, except for the chip erase mode ⁽¹⁾, only TTL inputs are required. To write into a particular location, a TTL low is applied to write enable (WE) pin of a selected (CE low) device. This, combined with output enable (OE) being high, initiates a write cycle. During a byte write cycle, addresses are latched on the last falling edge of CE or WE and data is latched on the first rising edge of CE or WE. An internal timer times out the required byte write time. An automatic byte erase is performed internally in the byte write mode.

DATA Polling (Optional Feature)

DATA polling is a method of minimizing write times by determining the actual end-point of a write cycle. If a read is performed to any address while the device is still writing, it will present the ones-complement of the last byte written. When the device has completed its write cycle, a read from the last address written will result in valid data. Thus, software can simply read from the part until the last data byte written is read correctly. Timing for a DATA polling read is the same as a normal read.

Recommended Operating Conditions

| | | 2816A/2816AH-150 5516A/5516AH-150 | 2816A/2816AH-200 5516A/5516AH-200 | 2816A/2816AH-250 5516A/5516AH-250 | 2816A/2816AH-300 5516A/5516AH-300 |
|--------------------------------|------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|
| Temperature Range | Commercial | 0°C to +70°C | 0°C to +70°C | 0°C to +70°C | 0°C to +70°C |
| | Extended | -40°C to +85°C | -40°C to +85°C | -40°C to +85°C | -40°C to +85°C |
| | Military | -55°C to +125°C | -55°C to +125°C | -55°C to +125°C | -55°C to +125°C |
| V _{CC} Supply Voltage | | 5V±10% | 5V±10% | 5V±10% | 5V±10% |

Endurance and Data Retention

| Symbol | Parameter | Value | Units | Condition | |
|-----------------|-------------------|-------|-----------|------------------------------|------------------------------|
| N | Minimum Endurance | 2816A | 10,000 | Cycles/Byte | MIL-STD 883 Test Method 1033 |
| | | 5516A | 100,000 | | |
| | | | 400,000 | Cycles/Byte | MIL-STD 883 Test Method 1033 |
| | | | 1,000,000 | | |
| T _{DR} | Data Retention | >10 | Years | MIL-STD 883 Test Method 1033 | |

Notes:

1. Chip Erase is an optional mode.
2. Characterized. Not tested.

Mode Selection (Table 1)

| Mode | CE | OE | WE | I/O |
|---------------|-----------------|-----------------|-----------------|-------------------------|
| Read | V _{IL} | V _{IL} | V _{IH} | D _{OUT} |
| Standby | V _{IH} | X | X | High Z |
| Byte Write | V _{IL} | V _{IH} | V _{IL} | D _{IN} |
| Write Inhibit | X | V _{IL} | X | High Z/D _{OUT} |
| | X | X | V _{IH} | High Z/D _{OUT} |

X: any TTL level

Absolute Maximum Stress Ratings*

Temperature

Storage -65°C to +150°C

Under Bias

Military/Extended -65°C to +135°C

Commercial -10°C to +80°C

D.C. Voltage applied to all Inputs or Outputs

with respect to ground +6.0 V to -0.5 V

Undershoot/Overshoot pulse of less than 10 ns

(measured at 50% point) applied to all inputs or

outputs with respect to ground (undershoot) -1.0 V
(overshoot) + 7.0 V

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Power Up/Down Considerations

The 2816A/5516A has internal circuitry to minimize a false write during system V_{CC} power up or down. This circuitry prevents writing under any one of the following conditions.

1. V_{CC} is less than 3V.^[2]
2. A negative Write Enable (\overline{WE}) transition has not occurred when V_{CC} is between 3 V and 5 V.

Writing will also be prevented if \overline{CE} or \overline{OE} are in a logical state other than that specified for a byte write in the Mode Selection table.

DC Operating Characteristics (Over the operating V_{CC} and temperature range)

| Symbol | Parameter | Limits | | Units | Test Condition |
|----------|--------------------------|--------|------|---------|--|
| | | Min. | Max. | | |
| I_{CC} | Active V_{CC} Current | | 100 | mA | $\overline{CE} = \overline{OE} = V_{IL}$; All I/O Open; Other Inputs = 5.5 V $\overline{CE} = \overline{OE} = V_{IL}$; All I/O Open; Other Inputs = 5.5 V |
| I_{SB} | Standby V_{CC} Current | | 40 | mA | $\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$; All I/O's Open; Other Inputs = 5.5 V |
| I_{LI} | Input Leakage Current | | 10 | μ A | $V_{IN} = 5.5$ V |
| I_{LO} | Output Leakage Current | | 10 | μ A | $V_{OUT} = 5.5$ V |
| V_{IL} | Input Low Voltage | -0.1 | 0.8 | V | |
| V_{IH} | Input High Voltage | 2.0 | 6 | V | |
| V_{OL} | Output Low Voltage | | 0.4 | V | $I_{OL} = 2.1$ mA |
| V_{OH} | Output High Voltage | 2.4 | | V | $I_{OH} = -400$ μ A |

Capacitance ^[1] $T_A = 25^\circ\text{C}$, $f = 1$ MHz

| Symbol | Parameter | Max | Conditions |
|-----------|------------------------|-------|----------------|
| C_{IN} | Input Capacitance | 6 pF | $V_{IN} = 0$ V |
| C_{OUT} | Data (I/O) Capacitance | 10 pF | $V_{IO} = 0$ V |

NOTES:

1. This parameter measured only for the initial qualification and after process or design changes which may affect capacitance.

Equivalent A.C. Test Conditions

Output Load: 1 TTL gate and $C_L = 100$ pF
 Input Rise and Fall Times: < 20 ns
 Input Pulse Levels: 0.45 V to 2.4 V
 Timing Measurement Reference Level:
 Inputs 1 V and 2 V
 Outputs 0.8 V and 2 V

AC Characteristics

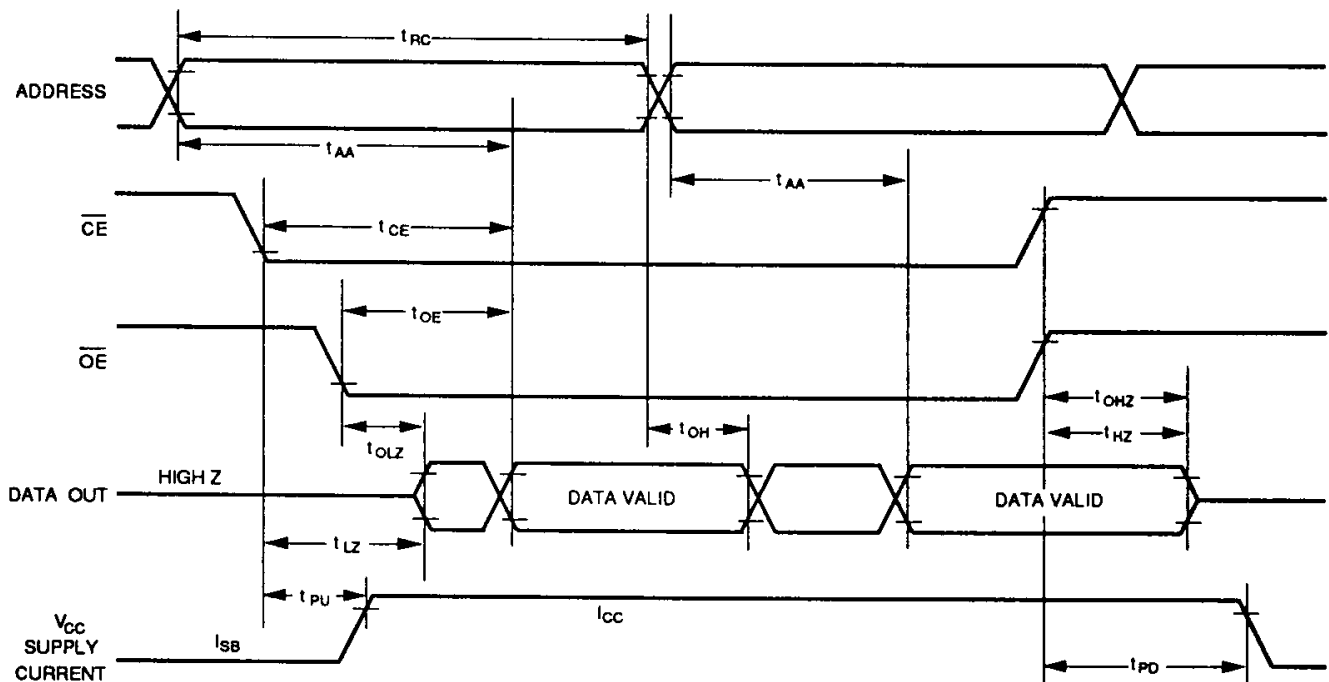
Read Operation (Over the operating V_{CC} and temperature range)

| Symbol | Parameter | Limits | | | | | | | | Units |
|----------------|-------------------------------------|--------------------------------------|------|--------------------------------------|------|--------------------------------------|------|--------------------------------------|------|-------|
| | | 2816A/2816AH-150 5516A/5516AH-150 | | 2816A/2816AH-200 5516A/5516AH-200 | | 2816A/2816AH-250 5516A/5516AH-250 | | 2816A/2816AH-300 5516A/5516AH-300 | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t_{RC} | Read Cycle Time | 150 | | 200 | | 250 | | 300 | | ns |
| t_{CE} | Chip Enable Access Time | | 150 | | 200 | | 250 | | 300 | ns |
| t_{AA} | Address Access Time | | 150 | | 200 | | 250 | | 300 | ns |
| t_{OE} | Output Enable Access Time | | 70 | | 90 | | 90 | | 100 | ns |
| t_{LZ} | \overline{CE} to Output in Low Z | 10 | | 10 | | 10 | | 10 | | ns |
| t_{HZ} | \overline{CE} to Output in High Z | | 100 | | 100 | | 100 | | 100 | ns |
| t_{OLZ} | \overline{OE} to Output in Low Z | 50 | | 50 | | 50 | | 50 | | ns |
| t_{OHZ} | \overline{OE} to Output in High Z | | 100 | | 100 | | 100 | | 100 | ns |
| $t_{OH}^{(1)}$ | Output Hold from Addr Change | 20 | | 20 | | 20 | | 20 | | ns |
| $t_{PU}^{(1)}$ | \overline{CE} to Power-up Time | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{PD}^{(1)}$ | \overline{CE} to Power Down Time | | 50 | | 50 | | 50 | | 50 | ns |

NOTES:

1. This parameter measured only for the initial qualification and after process or design changes which may affect capacitance.

Read Cycle Timing



AC Characteristics Write Operation (Over the operating V_{CC} and temperature range)

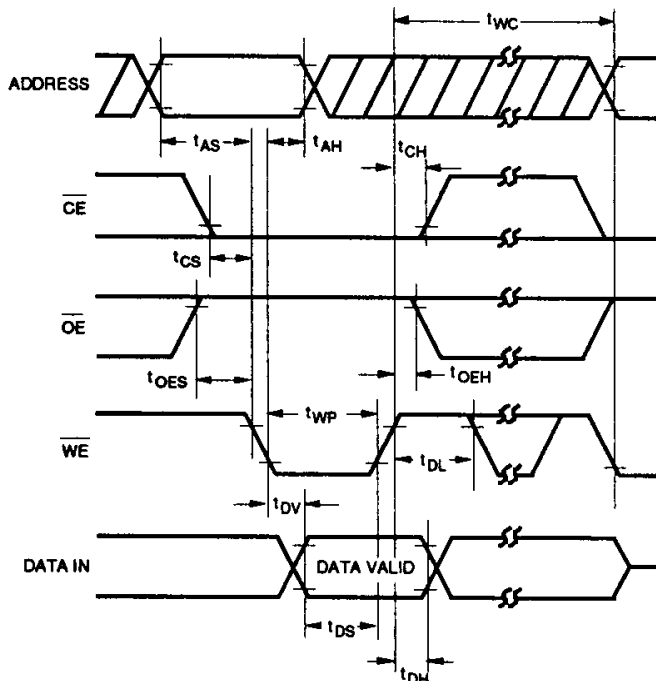
| Symbol | Parameter | Limits | | | | | | | | Units |
|----------------|---------------------------------------|------------------------------|------|------------------------------|------|------------------------------|------|------------------------------|------|---------|
| | | 2816A/AH-150 5516A/AH-150 | | 2816A/AH-200 5516A/AH-200 | | 2816A/AH-250 5516A/AH-250 | | 2816A/AH-300 5516A/AH-300 | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t_{WC} | Write Cycle Time | | | | | | | | | |
| | 2816AH/5516AH | | 2 | | 2 | | 2 | | 2 | ms |
| | 2816A/5516A | | 10 | | 10 | | 10 | | 10 | ms |
| t_{AS} | Address Set Up Time | 10 | | 10 | | 10 | | 10 | | ns |
| t_{AH} | Address Hold Time | 50 | | 50 | | 50 | | 70 | | ns |
| t_{CS} | Write Set Up Time | 0 | | 0 | | 0 | | 0 | | ns |
| t_{CH} | Write Hold Time | 0 | | 0 | | 0 | | 0 | | ns |
| t_{CW} | \overline{CE} to End of Write Input | 150 | | 150 | | 150 | | 150 | | ns |
| t_{OES} | \overline{OE} Set Up Time | 10 | | 10 | | 10 | | 10 | | ns |
| t_{OEH} | \overline{OE} Hold Time | 10 | | 10 | | 10 | | 10 | | ns |
| $t_{WP}^{(1)}$ | \overline{WE} Write Pulse Width | 100 | | 150 | | 150 | | 150 | | ns |
| t_{DL} | Data Latch Time | 50 | | 50 | | 50 | | 50 | | ns |
| $t_{DV}^{(2)}$ | Data Valid Time | | 1 | | 1 | | 1 | | 1 | μ s |
| t_{DS} | Data Set Up Time | 50 | | 50 | | 50 | | 50 | | ns |
| t_{DH} | Data Hold Time | 0 | | 0 | | 0 | | 0 | | ns |

NOTES:

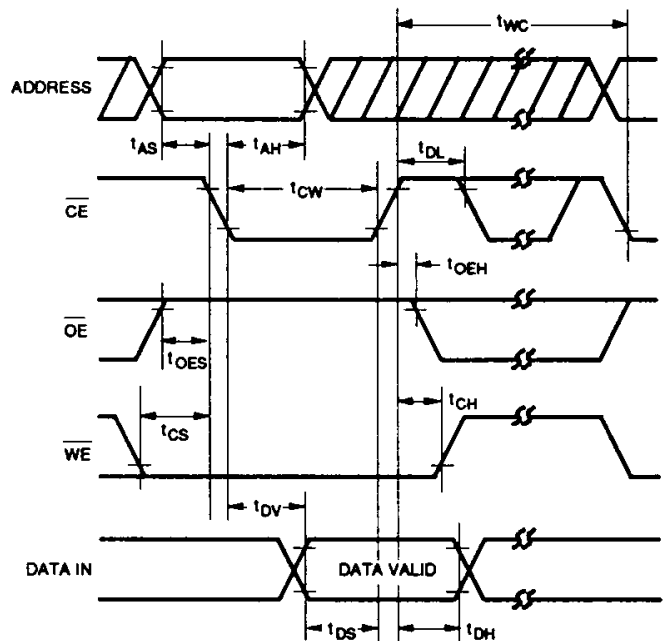
1. \overline{WE} is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
2. Data must be valid within 1 μ s maximum after the initiation of a write cycle.

TTL Byte Write Cycle

\overline{WE} CONTROLLED WRITE CYCLE



\overline{CE} CONTROLLED WRITE CYCLE



Ordering Information

