National Semiconductor

DM54251/DM74251 TRI-STATE® 1 of 8 Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources, and feature a strobe-controlled TRI-STATE output. The strobe must be at a low logic level to enable these devices. The TRI-STATE outputs permit direct connection to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time.

Features

- TRI-STATE version of 151
- Interface directly with system bus
- Perform parallel-to-serial conversion
- Permit multiplexing from N-lines to one line
- Complementary outputs provide true and inverted data
- Max no. of common outputs
  DM54251 49
  DM74251 129
- Typical propagation delay time (D to Y) 17ns
- Typical power dissipation 155 mW

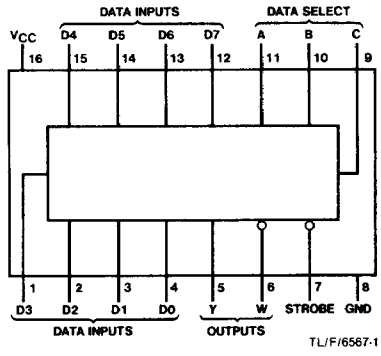
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6567-1

54251 (J) **74251 (N)**

Function Table

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Logic Level, L = Low Logic Level
X = Don't Care, Z = High Impedance (Off)
D0, D1...D7 = The Level of the respective D input.

Recommended Operating Conditions

Symbol	Parameter	DM54251			DM74251			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−5.2	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current@ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−18		−70	mA
			DM74	−18		−70	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			31	51	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the outputs open, STROBE at 4.5V or ground, and all other inputs at 4.5V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$						Units
		$C_L = 5$ pF			$C_L = 50$ pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	A, B, C (4 Levels) to Y					22	36	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A, B, C (4 Levels) to Y					23	36	ns
t_{PLH} Propagation Delay Time Low to High Level Output	A, B, C (3 Levels) to W					18	29	ns
t_{PHL} Propagation Delay Time High to Low Level Output	A, B, C (3 Levels) to W					16	27	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Y					17	28	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Y					18	28	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Data to W					11	15	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to W					10	15	ns
t_{PZH} Output Enable Time to High Level Output	Strobe to Y					15	27	ns
t_{PZL} Output Enable Time to Low Level Output	Strobe to Y					18	36	ns
t_{PZH} Output Enable Time to High Level Output	Strobe to W					15	27	ns
t_{PZL} Output Enable Time to Low Level Output	Strobe to W					19	38	ns
t_{PHZ} Output Disable Time from High Level Output	Strobe to Y	4	8					ns
t_{PLZ} Output Disable Time from Low Level Output	Strobe to Y	14	23					ns
t_{PHZ} Output Disable Time from High Level Output	Strobe to W	4	8					ns
t_{PLZ} Output Disable Time from Low Level Output	Strobe to W	15	23					ns

Logic Diagram