National Semiconductor

DM5470/DM7470 AND-Gated Positive-Edge-Triggered J-K Flip-Flop with Preset, Clear, and Complementary Outputs

General Description

This device is a positive-edge-triggered J-K flip-flop with complementary outputs. Multiple J and K inputs are ANDed together to produce the internal J and K function for the flip-flop. If the $\overline{J}$ and $\overline{K}$ inputs are not used they must be grounded for proper operation of the flip-flop. The J and K data is accepted by the flip-flop on the positive going edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the positive going edge of the clock pulse. The clear and preset inputs are asynchronous but it is necessary that the clock input be at a low level when they become active (low).

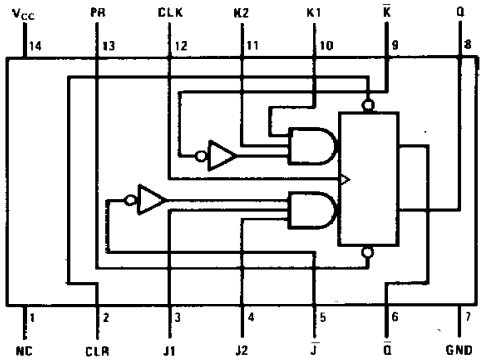
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6523-1

DM5470 (J) DM7470 (N)

Function Table

Inputs					Outputs	
PR	CLR	CLK	J (Note 1)	K (Note 1)	Q	$\overline{Q}$
L	H	L	X	X	H	L
H	L	L	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	Q_O	$\overline{Q}_O$
H	H	↑	H	L	H	L
H	H	↑	L	H	L	H
H	H	↑	H	H	Toggle	
H	H	L	X	X	Q_O	$\overline{Q}_O$

Note 1: $J = (J1)(J2)(\overline{J})$, $K = (K1)(K2)(\overline{K})$ if the $\overline{J}$ and $\overline{K}$ inputs are not used they must be grounded.

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

↑ = Positive Going Transition

* = This configuration is nonstable; that is, it will not persist when preset and/or clear inputs return to their inactive (high) level.

Q_O = The output logic level of Q before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each positive transition of the clock.

Recommended Operating Conditions

Sym	Parameter		DM5470			DM7470			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0		20	0		20	MHz
t_W	Pulse Width	Clock High	20			20			ns
		Clock Low	30			30			
		Preset Low	25			25			
		Clear Low	25			25			
t_{SU}	Input Setup Time (Note 1)		20↑			20↑			ns
t_H	Input Hold Time (Note 1)		5↑			5↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	J, K, or $\overline{R}$			40	μA
			Clock			40	
			Clear			80	
			Preset			80	

Electrical Characteristics (Continued) over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V (Note 5)	J, K, or $\overline{K}$			−1.6	mA
			Clock			−1.6	
			Clear			−3.2	
			Preset			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			13	26	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		20	35		MHz
t_{PHL} Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$			50	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Preset to Q			50	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q			50	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$			50	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$			50	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$			50	ns

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Note 4: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock input is at 4.5V.

Note 5: Clear is tested with preset high and preset is tested with clear high.