

T-52-09



PRELIMINARY

DM54ALS1242/DM74ALS1242/DM54ALS1243A/DM74ALS1243A

DM54ALS1242/DM74ALS1242/ DM54ALS1243A/DM74ALS1243A Quad Bidirectional Bus Drivers

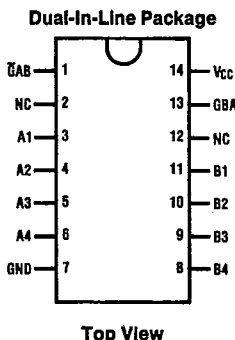
General Description

These octal TRI-STATE® bus drivers are designed to provide the designer with flexibility in implementing a bus interface with memory, microprocessor, or communication systems, and are low power dissipation versions of the 'ALS242 and 'ALS243. The 'ALS1242 has inverting buffers, while the 'ALS1243A has non-inverting buffers. The direction enable gating is configured with separate control over either buffer direction and the two control buffers are complementary. Connecting these control inputs to one common line implements single line direction control, while individual control can put both buffer directions into TRI-STATE simultaneously (disabled state) or put both buffer directions into the active state (data latch state). The TRI-STATE circuitry contains a feature that maintains the buffer outputs in TRI-STATE (high impedance state) during power supply ramp-up or ramp-down. This eliminates bus glitching problems that arise during power-up and power-down.

Features

- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Switching response specified into 500Ω and 50 pF load
- Switching response specifications guaranteed over full temperature and V_{CC} supply range
- PNP input design reduces input loading
- Low power dissipation version of the DM54/74ALS242, 243
- Low level drive current: 54ALS=8 mA, 74ALS=16 mA

Connection Diagram



Order Number DM54ALS1242J, DM54ALS1243AJ, DM74ALS1242M,
DM74ALS1243AM, DM74ALS1242N or DM74ALS1243AN
See NS Package Number J14A, M14A or N14A

Function Table

Inputs		ALS1242A	ALS1243A
GAB	GBA		
L	L	\bar{A} to B	A to B
H	H	\bar{B} to A	B to A
H	L	Isolation	Isolation
L	H	Latch A and B (A = \bar{B})	Latch A and B (A = B)

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Input Voltage	
Dedicated Inputs	7V
I/O Ports	5.5V
Operating Free Air Temperature Range	
DM54ALS	-55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	DM54ALS1242 DM54ALS1243A			DM74ALS1242 DM74ALS1243A			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			-12			-15	mA
I_{OL}	Low Level Output Current			8			16	mA
T_A	Operating Free-Air Temperature	-55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature (unless otherwise specified)

Symbol	Parameter	Conditions	DM54ALS1242 DM54ALS1243A			DM74ALS1242 DM74ALS1243A			Units
			Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V, I_I = -18\text{ mA}$			-1.2			-1.2	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V\text{ to }5.5V, I_{OH} = -0.4\text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
		$V_{CC} = 4.5V, I_{OH} = -3\text{ mA}$	2.4			2.4			V
		$I_{OH} = \text{Max}$	2			2			V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V, I_{OL} = 54\text{ ALS (Max)}$		0.25	0.4		0.25	0.4	V
		$I_{OL} = 74\text{ ALS (Max)}$		-	-		0.35	0.5	V
I_I	Input Current at Max Input Voltage	$V_{CC} = 5.5V, V_I = 7V$ ($V_I = 5.5V$ for A or B Ports)			0.1			0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V, V_I = 2.7V$			20			20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V, V_{IL} = 0.4V$			-0.1			-0.1	mA
I_O	Output Drive Current	$V_{CC} = 5.5V, V_O = 2.25V$	-30		-112	-30		-112	mA
I_{CC}	Supply Current	$V_{CC} = 5.5V, \text{ ALS1242}$ Active Outputs High		8	14		8	12	mA
		Active Outputs Low		10	17		10	15	mA
		Outputs TRI-STATE		9	16		9	14	mA
		$V_{CC} = 5.5V, \text{ ALS1243}$ Active Outputs High		9			9		mA
		Active Outputs Low		10			10		mA
		Outputs TRI-STATE		11			11		mA

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'ALS1242 Switching Characteristics

over recommended operating free-air temperature range (see Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	V _{CC} = 4.5V to 5.5V, C _L = 50 pF, R ₁ = 500Ω, R ₂ = 500Ω, T _A = Min to Max				Units
			54ALS1242		74ALS1242		
			Min	Max	Min	Max	
t _{PLH}	Propagation Delay Time Low to High Level Output	A or B to B or A	2	14	2	12	ns
t _{PHL}	Propagation Delay Time High to Low Level Output	A or B to B or A	2	12	2	10	ns
t _{PZH}	Output Enable Time to High Level Output	\overline{G} AB to B	4	20	4	17	ns
t _{PZL}	Output Enable Time to Low Level Output	\overline{G} AB to B	5	23	5	21	ns
t _{PHZ}	Output Disable Time from High Level Output	\overline{G} AB to B	2	12	2	10	ns
t _{PLZ}	Output Disable Time from Low Level Output	\overline{G} AB to B	2	12	2	10	ns
t _{PZH}	Output Enable Time to High Level Output	GBA to A	5	23	5	20	ns
t _{PZL}	Output Enable Time to Low Level Output	GBA to A	6	25	6	23	ns
t _{PHZ}	Output Disable Time from High Level Output	GBA to A	2	12	2	10	ns
t _{PLZ}	Output Disable Time from Low Level Output	GBA to A	2	15	2	12	ns

'ALS1243A Switching Characteristics

over recommended operating free-air temperature range (see Section 1 for Test Waveforms and Output Load)

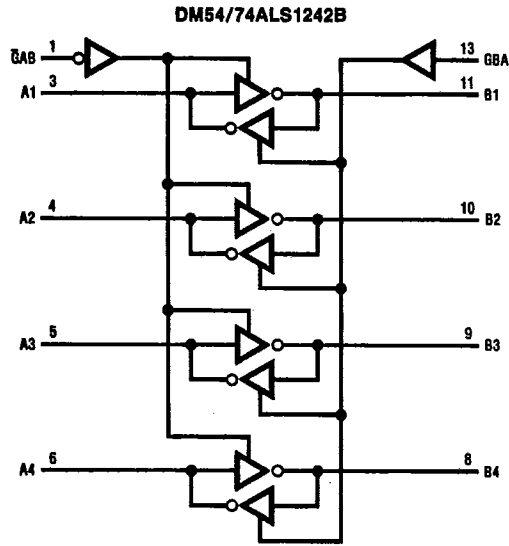
Symbol	Parameter	From (Input) To (Output)	V _{CC} = 4.5V to 5.5V, C _L = 50 pF, R ₁ = 500Ω, R ₂ = 500Ω, T _A = Min to Max				Units
			54ALS1243A		74ALS1243A		
			Min	Max	Min	Max	
t _{PLH}	Propagation Delay Time Low to High Level Output	A or B to B or A					ns
t _{PHL}	Propagation Delay Time High to Low Level Output	A or B to B or A					ns
t _{PZH}	Output Enable Time to High Level Output	\overline{G} AB to B					ns
t _{PZL}	Output Enable Time to Low Level Output	\overline{G} AB to B					ns
t _{PHZ}	Output Disable Time from High Level Output	\overline{G} AB to B					ns
t _{PLZ}	Output Disable Time from Low Level Output	\overline{G} AB to B					ns
t _{PZH}	Output Enable Time to High Level Output	GBA to A					ns
t _{PZL}	Output Enable Time to Low Level Output	GBA to A					ns
t _{PHZ}	Output Disable Time from High Level Output	GBA to A					ns
t _{PLZ}	Output Disable Time from Low Level Output	GBA to A					ns

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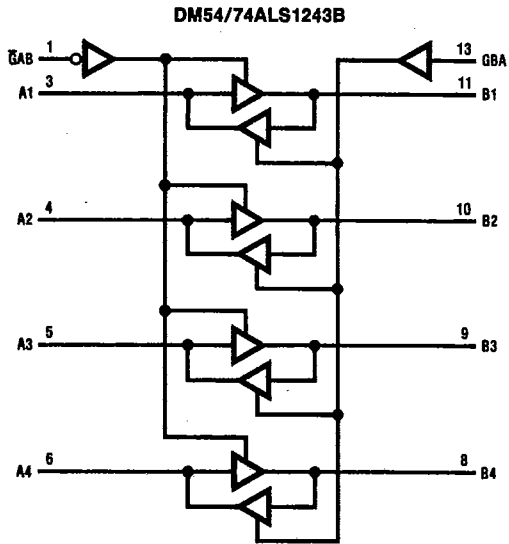
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Logic Diagrams



TL/F/6262-2



TL/F/6262-3