

## DM54LS377/DM74LS377

### Octal D Flip-Flop with Common Enable and Clock

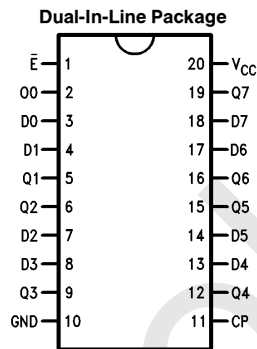
#### General Description

The 'LS377 is an 8-bit register built using advanced low power Schottky technology. This register consists of eight D-type flip-flops with a buffered common clock and a buffered common input enable. The device is packaged in the space-saving (0.3 inch row spacing) 20-pin package.

#### Features

- 8-bit high speed parallel registers
- Positive edge-triggered D-type flip-flops
- Fully buffered common clock and enable inputs

#### Connection Diagram



TL/F/9831-1

**Order Number DM54LS377E, DM54LS377J,**  
**DM54LS377W, DM74LS377WM or DM74LS377N**  
**See NS Package Number**  
**E20A, J20A, M20B, N20A or W20A**

Pin Names	Description
$\bar{E}$	Enable Input (Active LOW)
D0–D7	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
Q0–Q7	Flip-Flop Outputs

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

Symbol	Parameter	DM54LS377			DM74LS377			Units
		Min	Nom	Max	Min	Nom	Max	
V <sub>CC</sub>	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High Level Input Voltage	2			2			V
V <sub>IL</sub>	Low Level Input Voltage			0.7			0.8	V
I <sub>OH</sub>	High Level Output Current			−0.4			−0.4	mA
I <sub>OL</sub>	Low Level Output Current			4			8	mA
T <sub>A</sub>	Free Air Operating Temperature	−55		125	0		70	°C
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time HIGH or LOW D <sub>n</sub> to CP	20			10			ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time HIGH or LOW D <sub>n</sub> to CP	5.0			5.0			ns
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time HIGH or LOW E to CP	10			10			ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time HIGH or LOW E to CP	5.0			5.0			ns
t <sub>w</sub> (H) t <sub>w</sub> (L)	CP Pulse Width HIGH or LOW	20			20			ns

## Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = −18 mA			−1.5	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max V <sub>IL</sub> = Max	DM54 2.5			V
			DM74 2.7	3.4		
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max V <sub>IH</sub> = Min	DM54		0.4	V
		I <sub>OL</sub> = 4 mA, V <sub>CC</sub> = Min	DM74	0.35	0.5	
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 7V V <sub>I</sub> = 10V	DM74		0.1	mA
			DM54			
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 2.7V			20.0	μA
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 0.4V			−0.4	mA
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 2)	DM54 −20		−100	mA
			DM74 −20		−100	
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = Max			28	mA

Note 1: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

## Switching Characteristics $V_{CC} = +5.0V, T_A = +25^\circ C$



Symbol	Parameter	$R_L = 2\text{ k}\Omega, C_L = 15\text{ pF}$		Units
		Min	Max	
$f_{max}$	Maximum Clock Frequency	30		MHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay CP to $Q_n$		25	ns

## Functional Description

The  $\text{LS377}$  consists of eight edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable input ( $\bar{E}$ ) are common to all flip-flops.

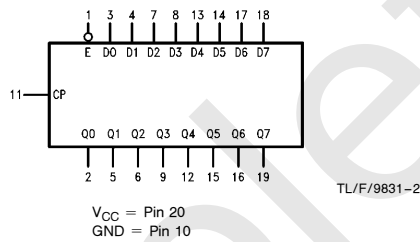
When  $\bar{E}$  is LOW, new data is entered into the register on the next LOW-to-HIGH transition of CP. When  $\bar{E}$  is HIGH, the register will retain the present data independent of the CP.

## Truth Table

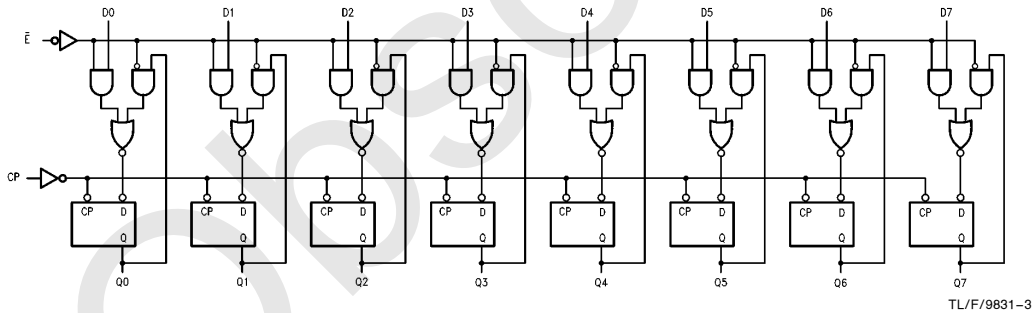
Inputs			Output
$\bar{E}$	CP	$D_n$	$Q_n$
H	X	X	No Change
L		H	H
L		L	L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

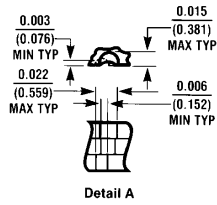
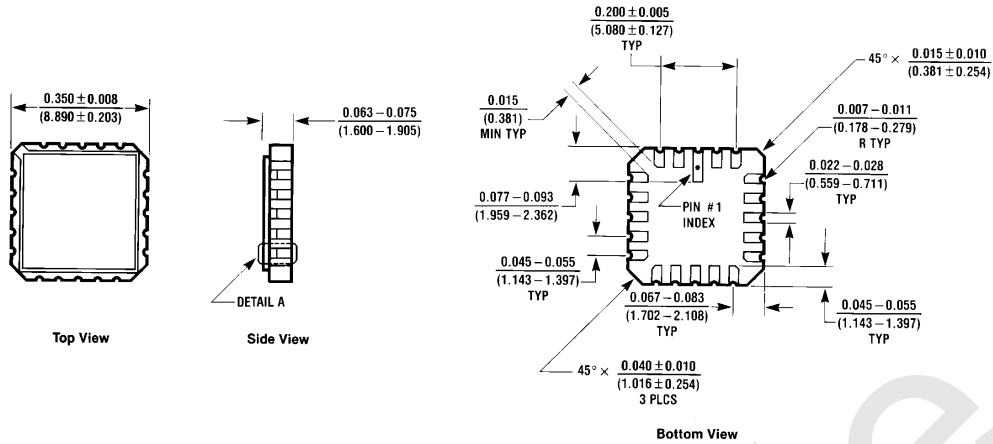
## Logic Symbol



## Logic Diagram

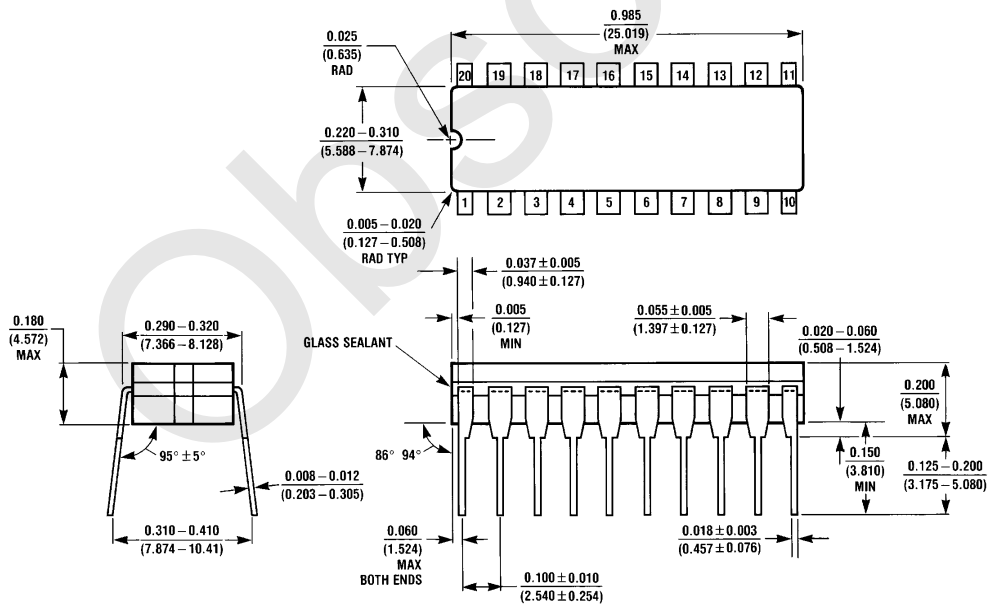


**Physical Dimensions** inches (millimeters)



**Ceramic Leadless Chip Carrier (E)**  
 Order Number DM54LS377E  
 NS Package Number E20A

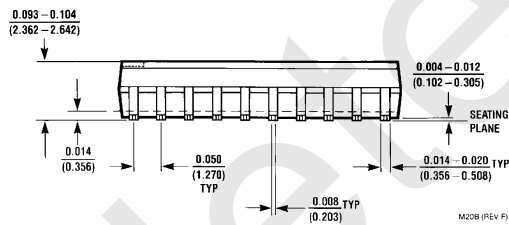
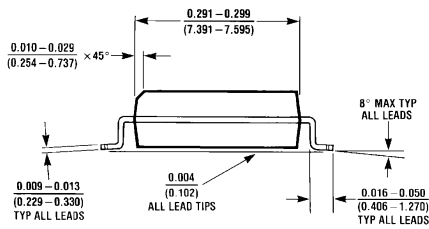
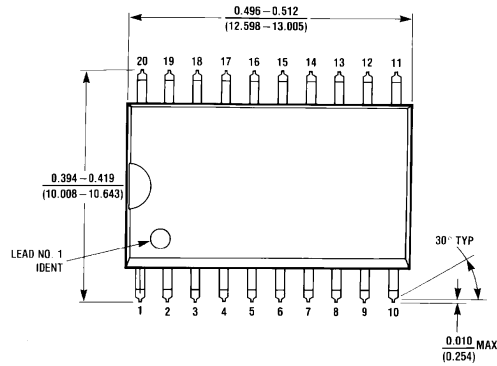
E20A (REV D)



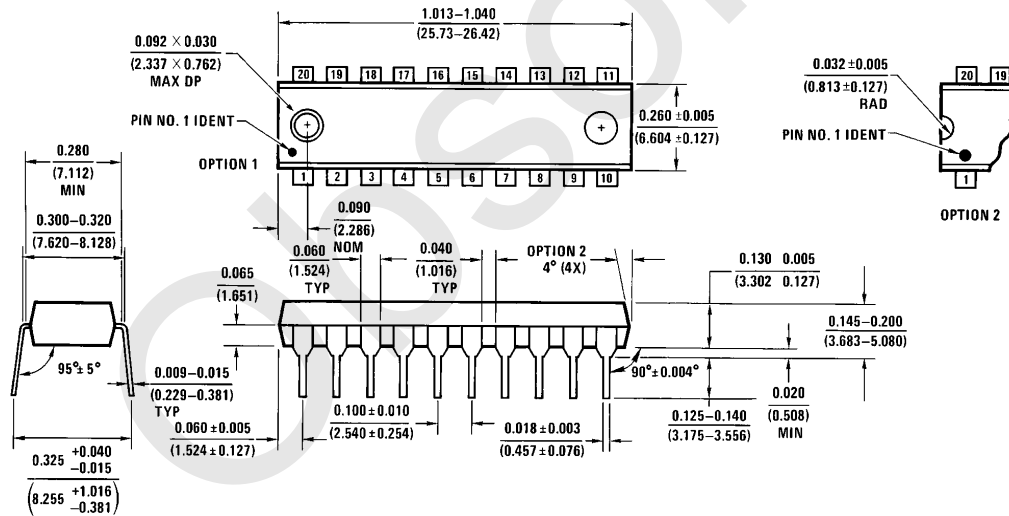
**20-Lead Ceramic Dual-In-Line Package (J)**  
 Order Number DM54LS377J  
 NS Package Number J20A

J20A (REV M)

**Physical Dimensions** inches (millimeters) (Continued)

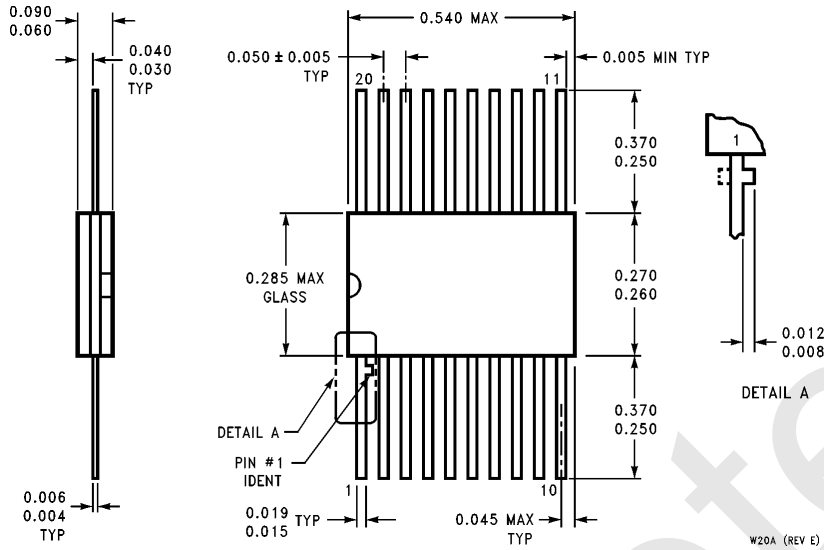


**20-Lead Wide Small Outline Molded Package (M)**  
**Order Number DM74LS377WM**  
**NS Package Number M20B**



**20-Lead Molded Dual-In-Line Package (N)**  
**Order Number DM74LS377N**  
**NS Package Number N20A**

**Physical Dimensions** inches (millimeters) (Continued)



**20-Lead Ceramic Flat Package (W)**  
**Order Number DM54LS377W**  
**NS Package Number W20A**

W20A (REV E)

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