

## DM54S194/DM74S194 4-Bit Bidirectional Universal Shift Registers

### General Description

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register; they feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

- Parallel (broadside) load
- Shift right (in the direction  $Q_A$  toward  $Q_D$ )
- Shift left (in the direction  $Q_D$  toward  $Q_A$ )
- Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs,  $S_0$  and  $S_1$ , high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

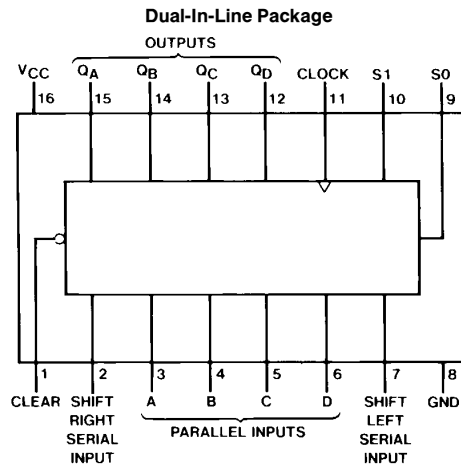
Shift right is accomplished synchronously with the rising edge of the clock pulse when  $S_0$  is high and  $S_1$  is low. Serial data for this mode is entered at the shift-right data input. When  $S_0$  is low and  $S_1$  is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low.

### Features

- Parallel inputs and outputs
- Four operating modes:
  - Synchronous parallel load
  - Right shift
  - Left shift
  - Do nothing
- Positive edge-triggered clocking
- Direct overriding clear
- Typical clock frequency 105 MHz
- Typical power dissipation 425 mW

### Connection Diagram



TL/F/6475-1

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	–55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	–65°C to +150°C

Note: The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the “Electrical Characteristics” table are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.

## Recommended Operating Conditions

Symbol	Parameter	DM54S194			DM74S194			Units
		Min	Nom	Max	Min	Nom	Max	
V <sub>CC</sub>	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High Level Input Voltage	2			2			V
V <sub>IL</sub>	Low Level Input Voltage			0.8			0.8	V
I <sub>OH</sub>	High Level Output Current			–1			–1	mA
I <sub>OL</sub>	Low Level Output Current			20			20	mA
f <sub>CLK</sub>	Clock Frequency (Note 1)	0	105	70	0	105	70	MHz
f <sub>CLK</sub>	Clock Frequency (Note 2)	0	90	60	0	90	60	MHz
t <sub>w</sub>	Pulse Width (Note 3)	Clock	7		7			ns
		Clear	12		12			
t <sub>SU</sub>	Setup Time (Note 3)	Mode	11		11			ns
		Data	5		5			
t <sub>H</sub>	Hold Time (Note 3)	3			3			ns
t <sub>REL</sub>	Clear Release Time (Note 3)	9			9			ns
T <sub>A</sub>	Free Air Operating Temperature	–55		125	0		70	°C

Note 1: C<sub>L</sub> = 15 pF, R<sub>L</sub> = 280Ω, T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5V.

Note 2: C<sub>L</sub> = 50 pF, R<sub>L</sub> = 280Ω, T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5V.

Note 3: T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5V.

## Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = –18 mA			–1.2	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max	DM54	2.5	3.4	V
		V <sub>IL</sub> = Max, V <sub>IH</sub> = Min	DM74	2.7	3.4	
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max V <sub>IH</sub> = Min, V <sub>IL</sub> = Max			0.5	V
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 5.5V			1	mA
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 2.7V			50	μA
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 0.5V			–2	mA
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 5)	DM54	–40	–100	mA
			DM74	–40	–100	
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = Max (Note 6)		85	135	mA

Note 4: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, CLEAR, and the SERIAL inputs, I<sub>CC</sub> is tested with a momentary ground, then 4.5V applied to CLOCK.

## Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25^\circ C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 280\Omega$				Units
			$C_L = 15\text{ pF}$		$C_L = 50\text{ pF}$		
			Min	Max	Min	Max	
$f_{MAX}$	Maximum Clock Frequency		70		60		MHz
$t_{PLH}$	Propagation Delay Time Low to High Level Output	Clock to Q		12		15	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	Clock to Q		16.5		20	ns
$t_{PHL}$	Propagation Delay Time High to Low Level Output	Clear to Q		18.5		23	ns

## Function Table

Clear	Mode		Clock	Inputs				Outputs					
	S1	S0		Serial		Parallel				$Q_A$	$Q_B$	$Q_C$	$Q_D$
				Left	Right	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{C0}$	$Q_{D0}$
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	$Q_{An}$	$Q_{Bn}$	$Q_{Cn}$
H	L	H	↑	X	L	X	X	X	X	L	$Q_{An}$	$Q_{Bn}$	$Q_{Cn}$
H	H	L	↑	H	X	X	X	X	X	$Q_{Bn}$	$Q_{Cn}$	$Q_{Dn}$	H
H	H	L	↑	L	X	X	X	X	X	$Q_{Bn}$	$Q_{Cn}$	$Q_{Dn}$	L
H	L	L	X	X	X	X	X	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{C0}$	$Q_{D0}$

H = High Level (steady state). L = Low Level (steady state). X = Don't Care (any input, including transitions).

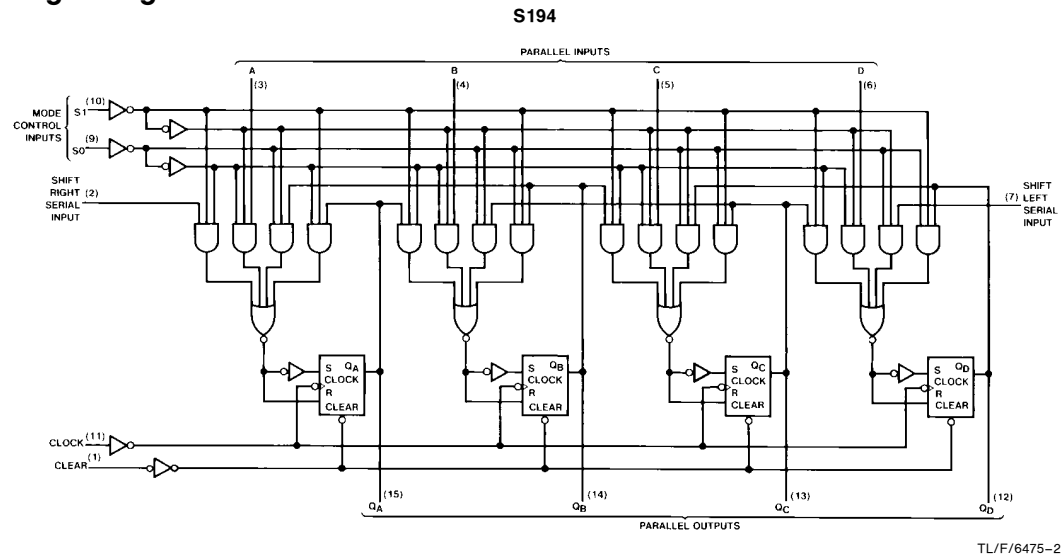
↑ = Transition from low to high level.

a, b, c, d = The level of steady state input at inputs A, B, C, or D, respectively.

$Q_{A0}$ ,  $Q_{B0}$ ,  $Q_{C0}$ ,  $Q_{D0}$  = The level of  $Q_A$ ,  $Q_B$ ,  $Q_C$ , or  $Q_D$ , respectively, before the indicated steady state input conditions were established.

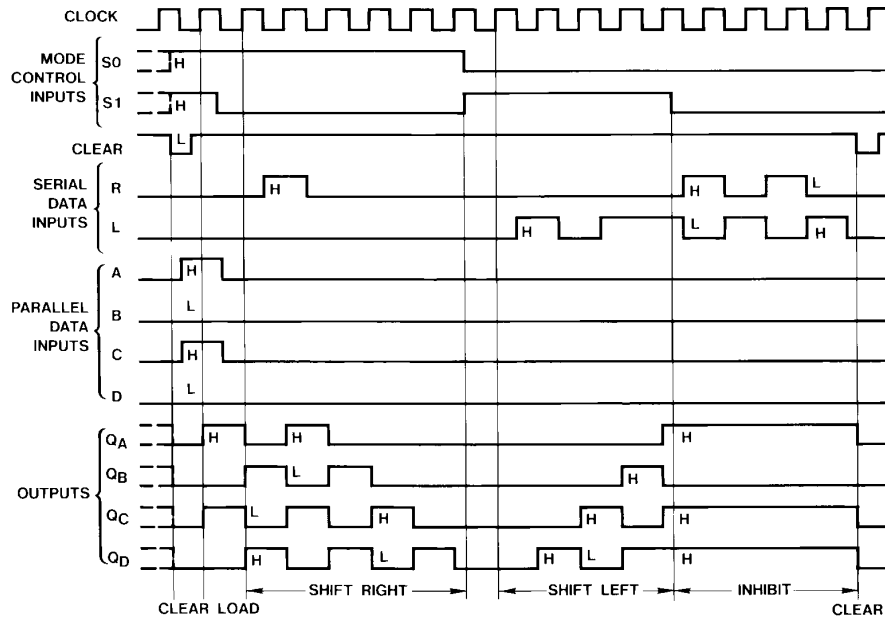
$Q_{An}$ ,  $Q_{Bn}$ ,  $Q_{Cn}$ ,  $Q_{Dn}$  = The level of  $Q_A$ ,  $Q_B$ ,  $Q_C$  respectively, before the most recent ↑ transition of the clock.

## Logic Diagram



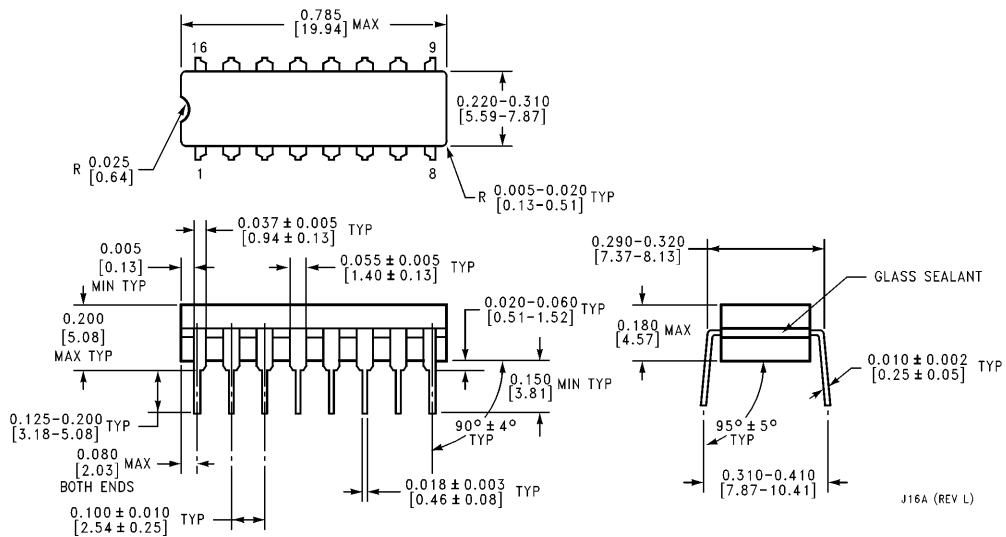
# Timing Diagram

Typical Clear, Load, Right-Shift, Left-Shift, Inhibit, and Clear Sequences



TL/F/6475-3

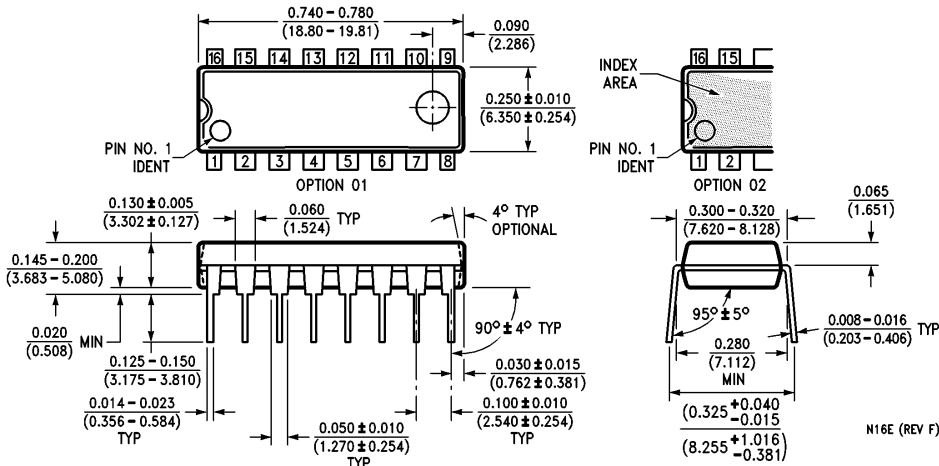
**Physical Dimensions** inches (millimeters)



**16-Lead Ceramic Dual-In-Line Package (J)**  
**Order Number DM54S194J**  
**NS Package Number J16A**

J16A (REV L)

**Physical Dimensions** inches (millimeters) (Continued)



**16-Lead Molded Dual-In-Line Package (N)**  
**Order Number DM74S194N**  
**NS Package Number N16E**

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