National Semiconductor

DM7123 Quad 2-Input Data Selectors/Multiplexers

General Description

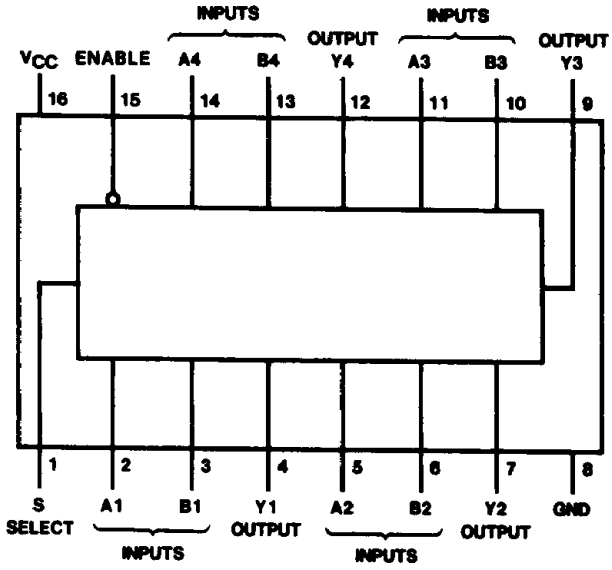
This device contains four 2-input multiplexers with common input select logic and common output disable circuitry. The DM7123 provides TRI-STATE® outputs. When the enable/strobe input is at a low logic level, the outputs of all devices are conventional TTL. However, when the enable/strobe input is raised to a high logic level, the outputs of the DM7123 go to the high-impedance third state. This device provides the designer with TRI-STATE and/or low power pin/pin replacements for the popular DM9322 and DM54/DM74157 multiplexers.

Features

- Pin equivalents popular DM9322 and DM54/DM74157 multiplexers
- Both conventional TTL and TRI-STATE outputs available
- Typical propagation delay 9.5 ns
- Typical power dissipation 200 mW

Connection Diagram

Dual-In-Line Package



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Order Number DM7123J or DM7123W
See NS Package Number J16A or W16A

Function Table

Enable	Select	Inputs		Outputs
		A	B	Y
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H
H	X	X	X	Hi-Z

L = Low Logic Level, H = High Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM71	−55°C to +125°C
Storage Temperature Range	−65°C to +150° C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM7123			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2	mA
I_{OL}	Low Level Output Current			16	mA
T_A	Free Air Operating Temperature	−55		125	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max			40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max			−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−30		−70	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)		40	51	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

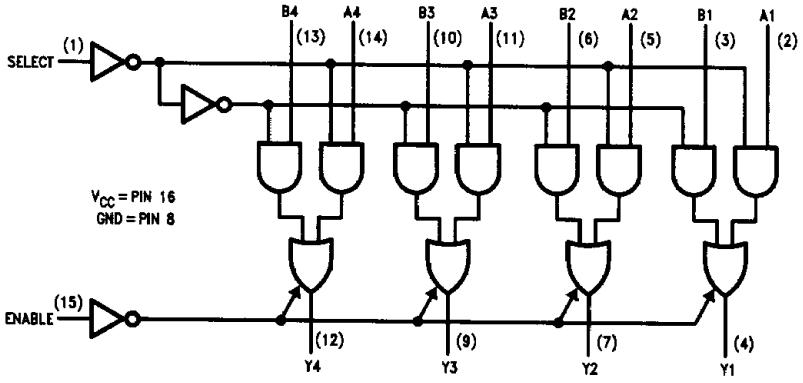
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the inputs grounded, and all outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω				Units
			C_L = 5 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output			4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output			5	18	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output			5	23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output			8	24	ns
t_{PZH}	Output Enable Time to High Level Output	Enable to Q			9	25	ns
t_{PZL}	Output Enable Time to Low Level Output	Enable to Q			10	30	ns
t_{PHZ}	Output Disable Time from High Level Output	Enable to Q	4	11			ns
t_{PLZ}	Output Disable Time from Low Level Output	Enable to Q	9	27			ns

Logic Diagram



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