

DM74ALS652 Octal 3-STATE Bus Transceiver and Register

General Description

This device incorporates an octal transceiver and an octal D-type register configured to enable transmission of data from bus to bus or internal register to bus.

This bus transceiver features totem-pole 3-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high level logic drive provide this device with the capability of being connected directly to and driving the bus lines in a bus organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The registers in the DM74ALS652 are edge-triggered D-type flip-flops. On the positive transition of the clock (CAB or CBA), the input data is stored into the appropriate register. The CAB input controls the transfer of data into the A register and the CBA input controls the B register.

The SAB and SBA control pins are provided to select whether real-time data or stored data is transferred. A LOW input level selects real-time data and a HIGH level selects stored data. The select controls have a "make before break" configuration to eliminate a glitch which would normally occur in a typical multiplexer during the transition between stored and real-time data.

The enable (GAB and $\overline{\text{GBA}}$) control pins provide four modes of operation: real-time data transfer from bus A to B, real-time data transfer from bus B to A, real-time bus A and/or B data transfer to internal storage, or internal stored data transfer to bus A and/or B.

Features

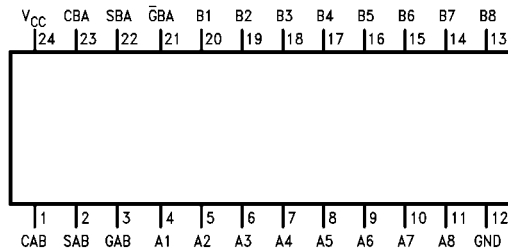
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- 3-STATE buffer-type outputs drive bus lines directly
- Independent registers and enables for A and B buses
- Multiplexed real-time and stored data

Ordering Code:

| Order Number | Package Number | Package Description |
|--------------|----------------|---|
| DM74ALS652WM | M24B | 24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide |
| DM74ALS652NT | N24C | 24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

| Inputs | | | | | | Data I/O (Note 1) | | Operation or Function |
|--------|-------------------------|------------|------------|---------------|---------------|-------------------|---------------|--|
| GAB | $\overline{\text{GBA}}$ | CAB | CBA | SAB | SBA | A1 thru A8 | B1 thru B8 | |
| X | H | \uparrow | H/L | X | X | Input | Not Specified | Store A, Hold B |
| L | X | H/L | \uparrow | X | X | Not Specified | Input | Store B, Hold A |
| L | H | \uparrow | \uparrow | X | X | Input | Input | Store A and B Data |
| L | H | H/L | H/L | X | X | Input | Input | Isolation, Hold Storage |
| L | L | X | X | X | L | Output | Input | Real-Time B Data to A Bus |
| L | L | X | H/L | X | H | Output | Input | Stored B Data to A Bus |
| H | H | X | X | L | X | Input | Output | Real-Time A Data to B Bus |
| H | H | \uparrow | \uparrow | X | X | Input | Output | Stored A Data to B Bus |
| H | H | \uparrow | \uparrow | X (Note 2) | X | Input | Output | Store A in both Registers |
| L | L | \uparrow | \uparrow | X (Note 2) | X (Note 2) | Output | Input | Store B in both Registers |
| H | L | H or L | H or L | H | H | Output | Output | Stored A Data to B Bus and Stored B Data to A Bus |

H = HIGH Logic Level

L = LOW Logic Level

X = Don't Care (Either LOW or HIGH Logic Levels, including transitions)

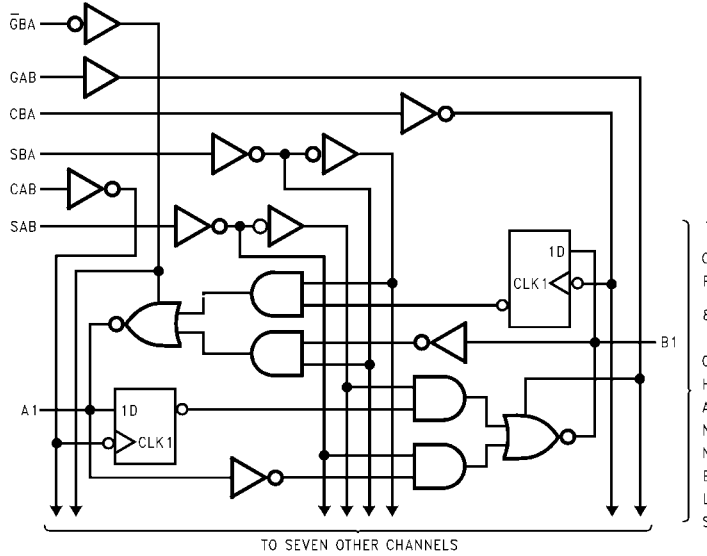
H/L = Either LOW or HIGH Logic Level excluding transitions

\uparrow = Positive-going edge of pulse

Note 1: The data output functions may be enabled or disabled by various signals at the $\overline{\text{G}}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.

Note 2: Select control = L; clocks can occur simultaneously
 Select control = H; clocks must be staggered in order to load both registers.

Logic Diagram



Absolute Maximum Ratings(Note 3)

| | |
|--------------------------------------|-----------------|
| Supply Voltage | 7V |
| Input Voltage | |
| Control Inputs | 7V |
| I/O Ports | 5.5V |
| Operating Free-Air Temperature Range | 0°C to +70°C |
| Storage Temperature Range | -65°C to +150°C |
| Typical θ_{JA} | |
| N Package | 44.5°C/W |
| M Package | 80.5°C/W |

Note 3: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

| Symbol | Parameter | Min | Nom | Max | Units |
|-----------|--|---------------|-----|-----|-------|
| V_{CC} | Supply Voltage | 4.5 | 5 | 5.5 | V |
| V_{IH} | HIGH Level Input Voltage | 2 | | | V |
| V_{IL} | LOW Level Input Voltage | | | 0.8 | V |
| I_{OH} | HIGH Level Output Current | | | -15 | mA |
| I_{OL} | LOW Level Output Current | | | 24 | mA |
| f_{CLK} | Clock Frequency | 0 | | 40 | MHz |
| t_W | Pulse Duration, Clocks Low or High | 12.5 | | | ns |
| t_{SU} | Data Setup Time, A before CAB or B before CBA (Note 4) | 10 \uparrow | | | ns |
| t_H | Data Hold Time, A after CAB or B after CBA (Note 4) | 0 \uparrow | | | ns |
| T_A | Free Air Operating Temperature | 0 | | 70 | °C |

Note 4: \uparrow = with reference to the LOW-to-HIGH transition of the respective clock.

Electrical Characteristics

over recommended free air temperature range

| Symbol | Parameter | Test Conditions | | Min | Typ | Max | Units |
|----------|--|--|-----------------------------------|--------------|------|------|---------------|
| V_{IK} | Input Clamp Voltage | $V_{CC} = \text{Min}$, $I_I = -18 \text{ mA}$ | | | | -1.2 | V |
| V_{OH} | HIGH Level Output Voltage | $V_{CC} = 4.5\text{V to }5.5\text{V}$ | $I_{OH} = -0.4 \text{ mA}$ | $V_{CC} - 2$ | | | V |
| | | $V_{CC} = \text{Min}$ | $I_{OH} = -3 \text{ mA}$ | 2.4 | 3.2 | | |
| | | | $I_{OH} = \text{Max}$ | 2 | | | |
| V_{OL} | LOW Level Output Voltage | $V_{CC} = \text{Min}$ | $I_{OL} = 12 \text{ mA}$ | | 0.25 | 0.4 | V |
| | | | $I_{OL} = 24 \text{ mA}$ | | 0.35 | 0.5 | |
| | | | $I_{OL} = 48 \text{ mA}$ | | 0.35 | 0.5 | |
| I_I | Input Current at Maximum Input Voltage | $V_{CC} = \text{Max}$ | I/O Ports, $V_I = 5.5\text{V}$ | | | 100 | μA |
| | | | Control Inputs, $V_I = 7\text{V}$ | | | 100 | |
| I_{IH} | HIGH Level Input Current | $V_{CC} = \text{Max}$, $V_I = 2.7\text{V}$, (Note 5) | | | | 20 | μA |
| I_{IL} | LOW Level Input Current | $V_{CC} = \text{Max}$, $V_I = 0.4\text{V}$ (Note 5) | Control Inputs | | | -200 | μA |
| | | | I/O Ports | | | -200 | |
| I_O | Output Drive Current | $V_{CC} = \text{Max}$, $V_O = 2.25\text{V}$ | | -30 | | -112 | mA |
| I_{CC} | Supply Current | $V_{CC} = \text{Max}$ | Outputs HIGH | | 47 | 76 | mA |
| | | | Outputs LOW | | 55 | 88 | |
| | | | Outputs Disabled | | 55 | 88 | |

Note 5: For I/O ports the 3-STATE output currents (I_{OZH} and I_{OZL}) are included in the I_{IH} and I_{IL} parameters.

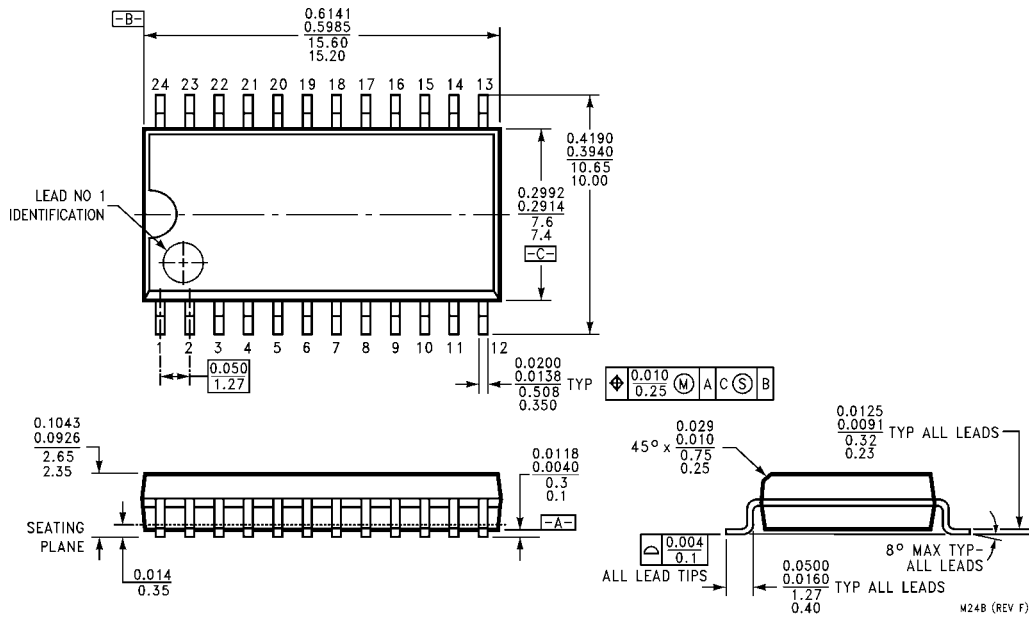
Switching Characteristics

over recommended operating free air temperature range (Note 6)

| Symbol | Parameter | Conditions | From (Input) To (Output) | Min | Max | Units |
|-----------|---|---|-----------------------------|-----|-----|-------|
| t_{PLH} | Propagation Delay Time LOW-to-HIGH Level Output | $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF, $R_1 = R_2 = 500\Omega$, $T_A = \text{Min to Max}$ | CBA or CAB to A or B | 10 | 30 | ns |
| t_{PHL} | Propagation Delay Time HIGH-to-LOW Level Output | | CBA or CAB to A or B | 5 | 17 | ns |
| t_{PLH} | Propagation Delay Time LOW-to-HIGH Level Output | | A or B to B or A | 5 | 18 | ns |
| t_{PHL} | Propagation Delay Time HIGH-to-LOW Level Output | | A or B to B or A | 3 | 12 | ns |
| t_{PLH} | Propagation Delay Time LOW-to-HIGH Level Output (with A or B LOW) (Note 6) | | SBA or SAB to A or B | 12 | 35 | ns |
| t_{PHL} | Propagation Delay Time HIGH-to-LOW Level Output (with A or B LOW) (Note 6) | | SBA or SAB to A or B | 6 | 20 | ns |
| t_{PLH} | Propagation Delay Time LOW-to-HIGH Level Output (with A or B HIGH) (Note 6) | | SBA or SAB to A or B | 6 | 25 | ns |
| t_{PHL} | Propagation Delay Time HIGH-to-LOW Level Output (with A or B HIGH) (Note 6) | | SBA or SAB to A or B | 5 | 20 | ns |
| t_{PZH} | Output Enable Time to HIGH Level Output | | $\overline{G}BA$ to A | 3 | 17 | ns |
| t_{PZL} | Output Enable Time to LOW Level Output | | $\overline{G}BA$ to A | 5 | 18 | ns |
| t_{PHZ} | Output Disable Time from HIGH Level Output | | $\overline{G}BA$ to A | 1 | 10 | ns |
| t_{PLZ} | Output Disable Time from LOW Level Output | | $\overline{G}BA$ to A | 2 | 16 | ns |
| t_{PZH} | Output Enable Time to HIGH Level Output | | GAB to B | 6 | 22 | ns |
| t_{PZL} | Output Enable Time to LOW Level Output | | GAB to B | 6 | 18 | ns |
| t_{PHZ} | Output Disable Time from HIGH Level Output | | GAB to B | 1 | 10 | ns |
| t_{PLZ} | Output Disable Time from LOW Level Output | | GAB to B | 2 | 16 | ns |

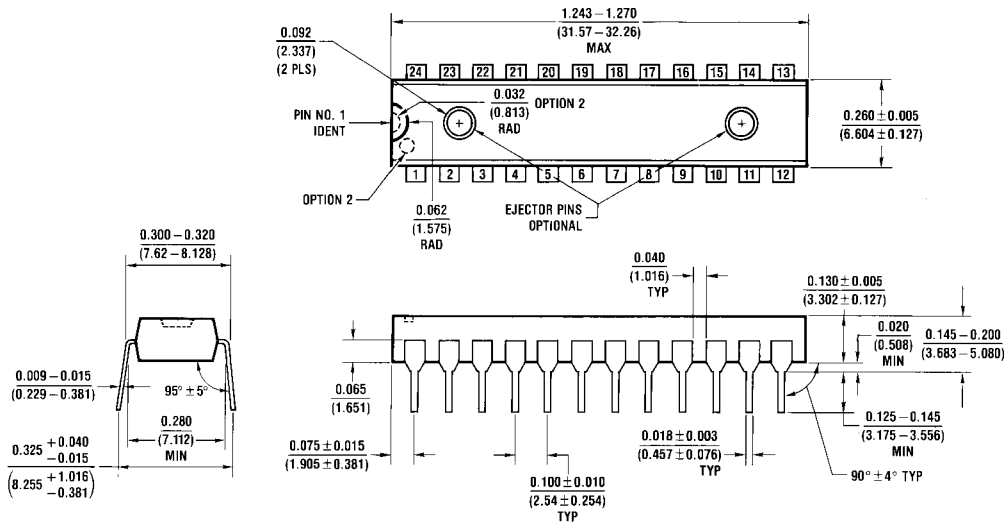
Note 6: These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

Physical Dimensions inches (millimeters) unless otherwise noted



**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide
Package Number N24C**

N24C (REV F)

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