T-45-07-00

National Semiconductor

DM74AS282 Look-Ahead Carry Generator with Selectable Carry Inputs

General Description

This circuit is a high-speed, look-ahead carry generator capable of anticipating a carry across four binary adders or groups of adders. It is cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided.

When used in conjunction with the 'AS881 arithmetic logic unit, this generator provides high-speed carry look-ahead capability for any word length. Each 'AS282 generates the look-ahead (anticipated carry) across a group of four ALUs and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under Typical Applications.

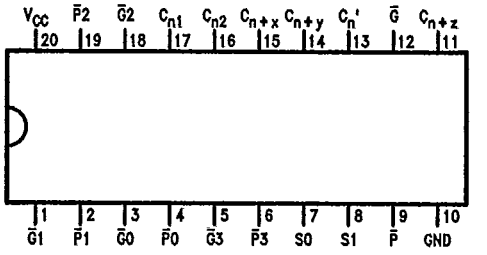
The carry functions (inputs, outputs, generate and propagate) of the look-ahead generator are implemented in compatible forms for direct connection to the 'AS881 ALU. The carry inputs are selectable in either active high or active low.

Features

- Selectable input version of 'AS182 allows double precision carry
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Switching specification at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- PNP inputs reduce input loading

Connection Diagram

Dual-In-Line Package



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Top View

Order Number DM74AS282N
See NS Package Number N20A*

Logic Equations

$$C_{n+x} = G0 + P0\,C_n$$
$$C_{n+y} = G1 + P1\,G0 + P1\,P0\,C_n$$
$$C_{n+z} = G2 + P2\,G1 + P2\,P1\,G0 + P2\,P1\,P0\,C_n$$
$$\overline{G} = \overline{G3 + P3\,G2 + P3\,P2\,G1 + P3\,P2\,P1\,G0}$$
$$\overline{P} = \overline{P3\,P2\,P1\,P0}$$

Pin Designations

Designations	Function
$\overline{G}0, \overline{G}1, \overline{G}2, \overline{G}3$	Carry Generate Inputs
$\overline{P}0, \overline{P}1, \overline{P}2, \overline{P}3$	Carry Propagate Inputs
C_{nA}, C_{nB}	Carry Inputs
C_n'	Selected Carry
$C_{n+x}, C_{n+y}, C_{n+z}$	Carry Outputs
$\overline{G}$	Carry Generate Outputs
$\overline{P}$	Carry Propagate Outputs
S0, S1	Carry Select Inputs
V_{CC}	Supply Voltage
GND	Ground

*Contact your local NSC representative about surface mount (M) package availability.

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Absolute Maximum Ratings

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Typical θ_{JA}	
N Package	67.0°C/W
M Package	97.0°C/W

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Operating Free-Air Temperature	0		70	°C

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise specified)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20 mA			0.3	0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.5V, V_I = 7V	C_{n1}, C_{n2}			200	µA
			$\overline{P3}$			200	
			$\overline{P2}$			300	
			$\overline{P0}$, $\overline{P1}$, $\overline{G3}$, S0, S1			400	
			$\overline{G0}$, $\overline{G2}$			700	
			$\overline{G1}$			800	
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V	C_{n1}, C_{n2}			40	µA
			$\overline{P3}$			40	
			$\overline{P2}$			60	
			$\overline{P0}$, $\overline{P1}$, $\overline{G3}$, S0, S1			80	
			$\overline{G0}$, $\overline{G2}$			140	
			$\overline{G1}$			160	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_I = 0.4V	C_{n1}, C_{n2}			−1	mA
			$\overline{P3}$			−1	
			$\overline{P2}$			−1.5	
			$\overline{P0}$, $\overline{P1}$, $\overline{G3}$, S0, S1			−2	
			$\overline{G0}$, $\overline{G2}$			−3.5	
			$\overline{G1}$			−4	

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Electrical Characteristics (Continued)

over recommended operating free-air temperature range (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
I_O (Note 2)	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V	−30		−112	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = 5.5V		22	35	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = 5.5V		26	49	mA

Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 2: The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current I_{OS}.

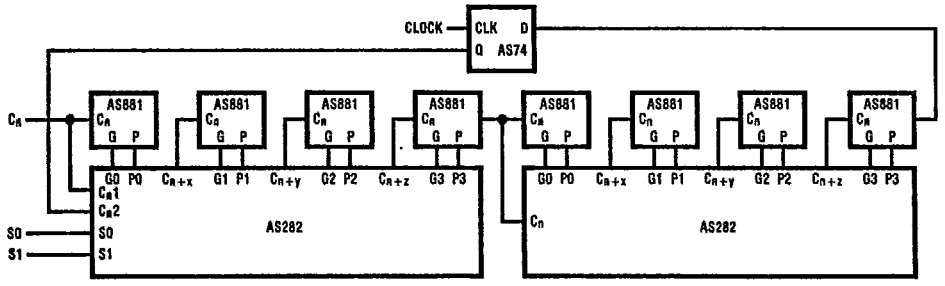
Switching Characteristics over recommended supply and temperature range (Note 3)

Symbol	Parameter	From (Input)	To (Output)	Conditions	Min	Max	25°C 5.0V Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$\overline{P}$ or $\overline{G}$	$C_n + x$, $C_n + y$, or $C_n + z$	C_L = 50 pF, R_L = 500Ω, V_{CC} = 4.5V to 5.5V	3	11	10	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	7	6.5	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$\overline{P}$ or $\overline{G}$	$\overline{G}$		2	11	10	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	8	7	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$\overline{P}$	$\overline{P}$		2	8	7	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	6	5.5	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_{n1}, C_{n2}, S1, S0	$C_n + x$, $C_n + y$, or $C_n + z$		3	14	13	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				3	12	11	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_{n1}, C_{n2}, S1, S0	C_n'		3	12	11	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				3	11	10	ns

Note 3: See Section 1 for test waveforms and output load.

Typical Application

32-Bit Look-Ahead Carry with Double Precision Carry



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Logic Diagram

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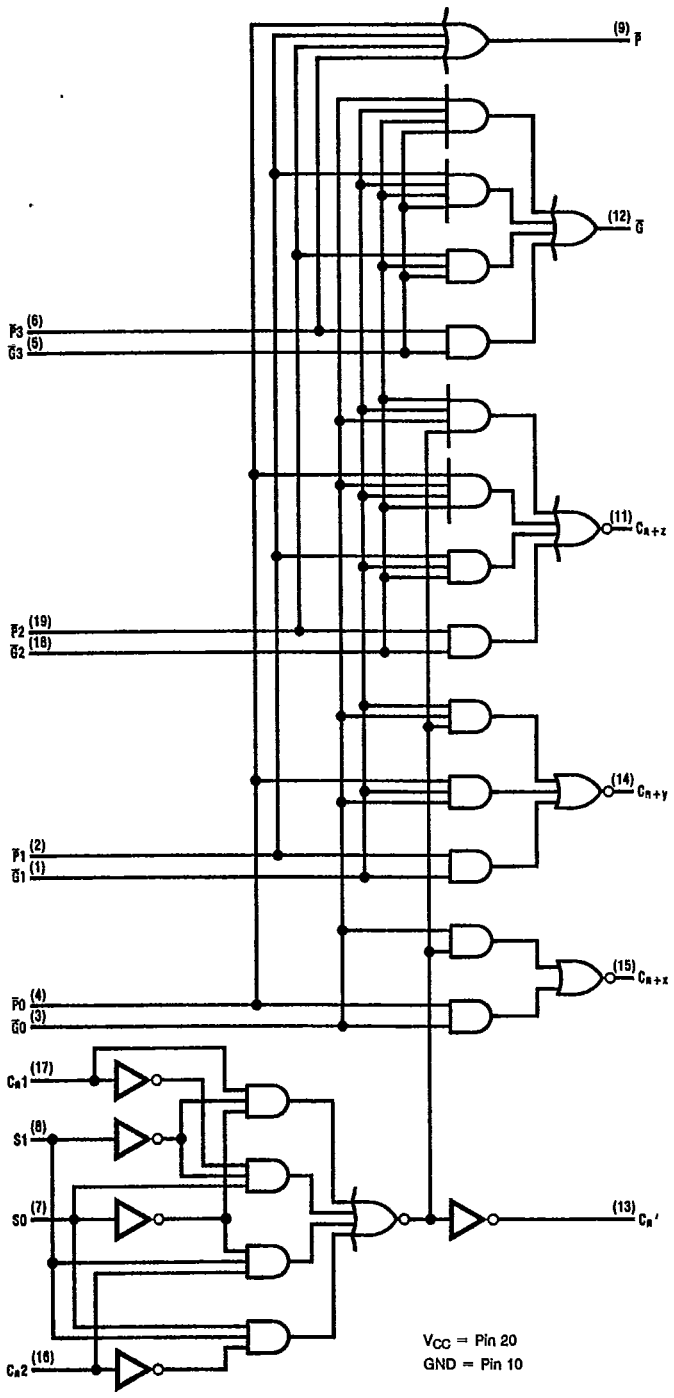

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Function Tables

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Function Table for $\overline{G}$ Output

Inputs							Output
$\overline{G}3$	$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All Other Combinations							H

Function Table for $\overline{P}$ Output

Inputs				Output
$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	$\overline{P}$
L	L	L	L	L
All Other Combinations				H

Function Table for C_n' Output

Inputs		Output
S1	S0	C_n'
L	L	C_{nA}
L	H	$\overline{C}_{nA}$
H	L	C_{nB}
H	H	$\overline{C}_{nB}$

H = High Level, L = Low Level, X = Irrelevant

Any inputs not shown in a given table are irrelevant with respect to that output.

Function Table for C_{n+x} Output

Inputs			Output
$\overline{G}0$	$\overline{P}0$	Cn'	C_{n+x}
L	X	X	H
X	L	H	H
All Other Combinations			L

Function Table C_{n+y} Output

Inputs					Output
$\overline{G}1$	$\overline{G}0$	$\overline{P}1$	$\overline{P}0$	$C_{n'}$	C_{n+y}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All Other Combinations					L

Function Table for C_{n+z} Output

Inputs							Output
$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	$C_{n'}$	C_{n+z}
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All Other Combinations							L