National Semiconductor

May 1989

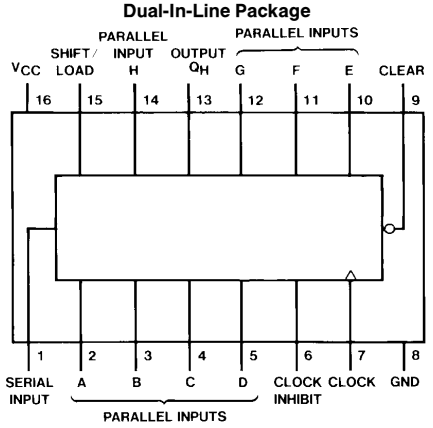
DM74LS166
8-Bit Parallel-In/Serial-Out Shift Registers

General Description

These parallel-in or serial-in, serial-out shift registers feature gated clock inputs and an overriding clear input. All inputs are buffered to lower the drive requirements to one normalized load, and input clamping diodes minimize switching transients to simplify system design. The load mode is established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input NOR gate, permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free running, and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

Connection Diagram

Dual-In-Line Package



TL/F/6400–1

Order Number DM74LS166WM or DM74LS166N
See NS Package Number M16B or N16A

Function Table

Inputs						Internal Outputs		Output Q_H
Clear	Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A . . . H	Q_A	Q_B	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)

X = Don't Care (any input, including transitions)

↑ = Transition from low to high level

a . . . h = The level of steady-state input at inputs A through H, respectively

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, Q_H, respectively, before the indicated steady-state input conditions were established

Q_{An}, Q_{Gn}, = The level of Q_A, Q_G, respectively, before the most recent ↑ transition of the clock

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM74LS166			Units
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.4	mA
I_{OL}	Low Level Output Current				8	mA
f_{CLK}	Clock Frequency (Note 1)		0		25	MHz
	Clock Frequency (Note 2)		0		20	MHz
t_W	Pulse Width (Note 6)	Clock	20			ns
		Clear	20			
t_{SU}	Setup Time (Note 6)	Mode	30			ns
		Data	20			
t_H	Hold Time (Note 6)		0			ns
T_A	Free Air Operating Temperature		0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 5)		22	38	mA

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 5: With all outputs open, 4.5V applied to the serial input, all other inputs except the CLOCK grounded, I_{CC} is measured after a momentary ground, then 4.5V is applied to the CLOCK.

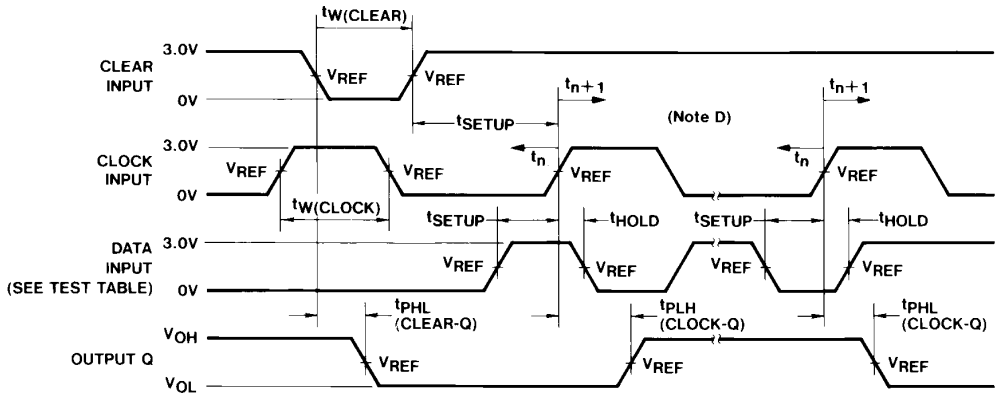
Note 6: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 2\,k\Omega$				Units
			$C_L = 15$ pF		$C_L = 50$ pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output	8	35		38	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output	8	35		41	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output	6	30		36	ns

Parameter Measurement Information

Voltage Waveforms



TL/F/6400–2

Test Table for Synchronous Inputs

Data Input for Test	Shift/Load	Output Tested (See Note C)
H	0V	Q_H at T_{N+1}
Serial Input	4.5V	Q_H at T_{N+8}

Note A: The clock pulse has the following characteristics: $t_{W(clock)} \geq 20$ ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{W(clear)} \geq 20$ ns and $t_{HOLD} = 0$ ns. When testing f_{MAX}, vary the clock PRR.

Note B: A clear pulse is applied prior to each test.

Note C: Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+8} with a functional test.

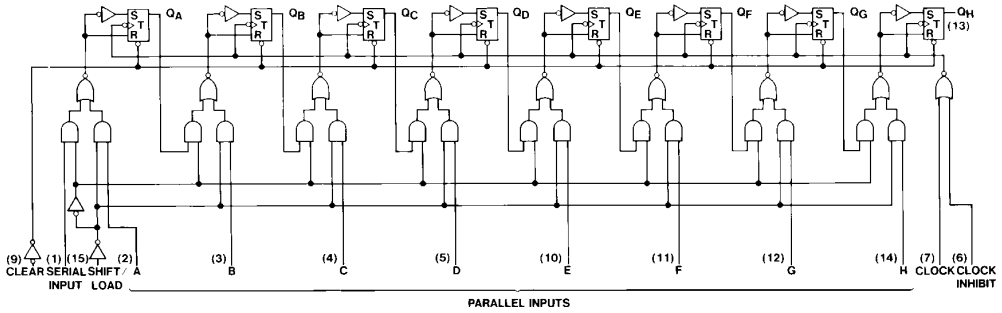
Note D: t_n = bit time before clocking transition

t_{n+1} = bit time after one clocking transition

t_{n+8} = bit time after eight clocking transitions

Note E: $V_{REF} = 1.3V$.

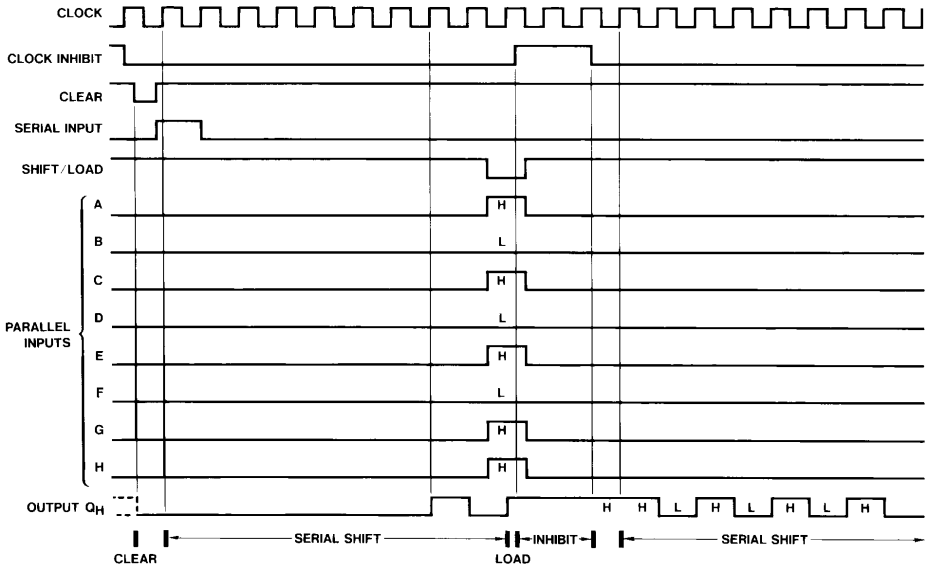
Logic Diagram



TL/F/6400–3

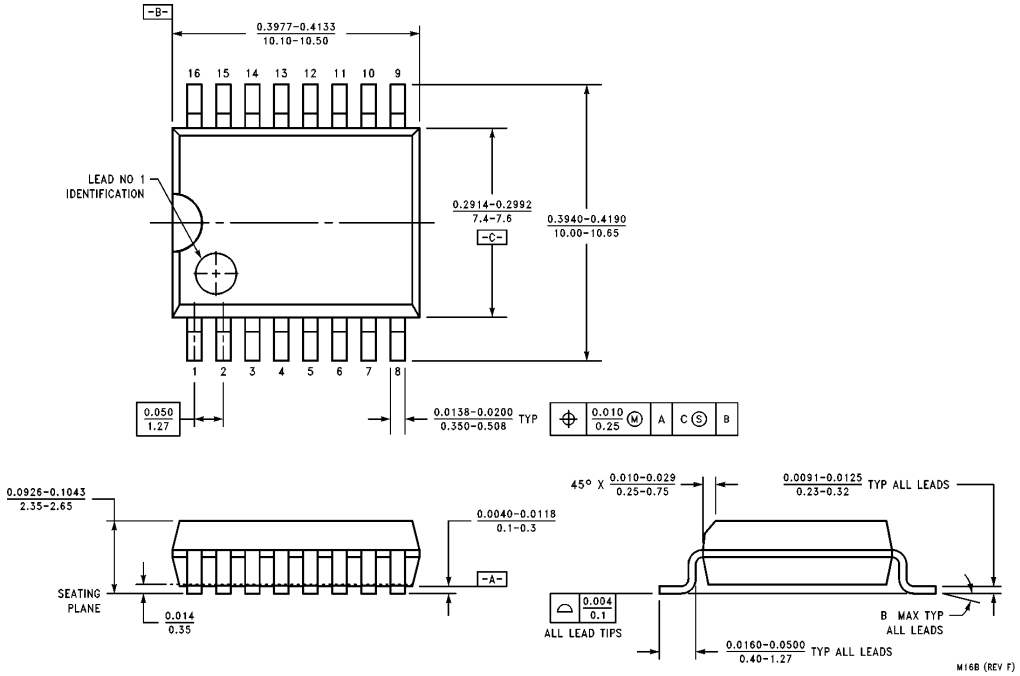
Timing Diagram

Typical Clear, Shift, Load, Inhibit and Shift Sequences



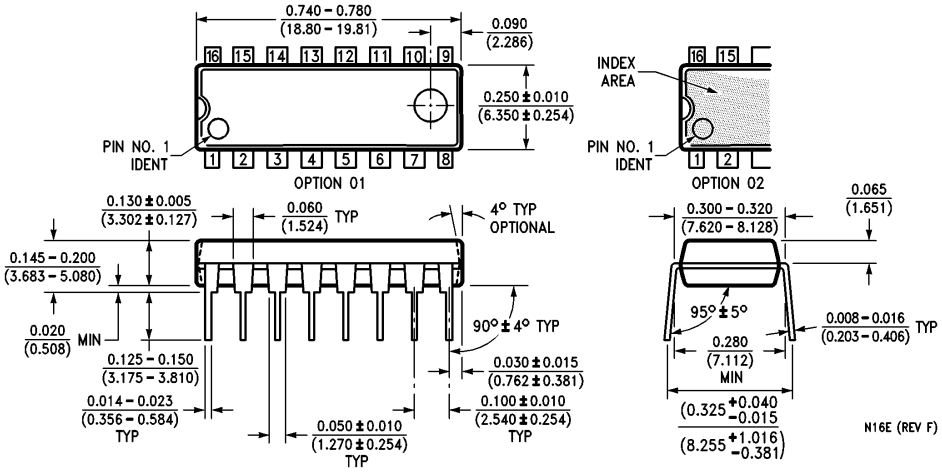
TL/F/6400–4

Physical Dimensions inches (millimeters)



16-Lead Wide Small Outline Molded Package (M)
Order Number DM74LS166WM
NS Package Number M16B

Physical Dimensions inches (millimeters) (Continued)



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS166N
NS Package Number N16E

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