

DM74LS196 Presettable Decade Counter

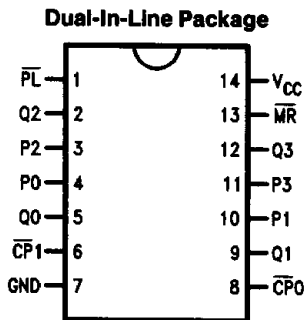
General Description

The 'LS196 decade ripple counter is partitioned into divide-by-two and divide-by-five sections which can be combined to count either in BCD (8421) sequence or in a bi-quinary mode producing a 50% duty cycle output. Both circuit types have a Master Reset (\overline{MR}) input which overrides all other inputs and asynchronously forces all outputs LOW. A Parallel Load input (\overline{PL}) overrides clocked operations and asynchronously loads the data on the Parallel Data inputs (P_n) into the flip-flops. This preset feature makes the circuits usable as programmable counters. The circuits can also be used as 4-bit latches, loading data from the Parallel Data inputs when \overline{PL} is LOW and storing the data when \overline{PL} is HIGH. In the counting modes, state changes are initiated by the falling edge of the clock.

Features

- High counting rates—typically 60 MHz
- Choice of counting modes—BCD, bi-quinary, binary
- Asynchronous preset and master reset

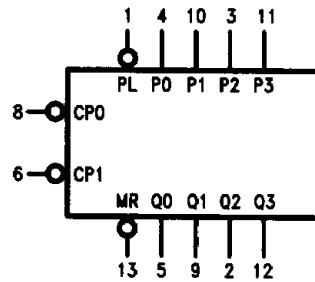
Connection Diagram



TL/F/10179-1

Order Number DM74LS196M or DM74LS196N
See NS Package Number M14A or N14A

Logic Symbol



V_{CC} = Pin 14
GND = Pin 7

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| Pin Names | Description |
|------------------|---|
| $\overline{CP0}$ | $\div 2$ Section Clock Input (Active Falling Edge) |
| $\overline{CP1}$ | $\div 5$ Section Clock Input (Active Falling Edge) |
| \overline{MR} | Asynchronous Master Reset Input (Active LOW) |
| P0-P3 | Parallel Data Inputs |
| \overline{PL} | Asynchronous Parallel Load Input (Active LOW) |
| Q0-Q3 | Flip-Flop Outputs |

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--------------------------------------|-----------------|
| Supply Voltage | 7V |
| Input Voltage | 7V |
| Operating Free Air Temperature Range | |
| DM74LS | 0°C to +70°C |
| Storage Temperature Range | -65°C to +150°C |

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

| Symbol | Parameter | DM74LS196 | | | Units |
|-----------|---|-----------|-----|------|-------|
| | | Min | Nom | Max | |
| V_{CC} | Supply Voltage | 4.75 | 5 | 5.25 | V |
| V_{IH} | High Level Input Voltage | 2 | | | V |
| V_{IL} | Low Level Input Voltage | | | 0.8 | V |
| I_{OH} | High Level Output Current | | | -0.4 | mA |
| I_{OL} | Low Level Output Current | | | 8 | mA |
| T_A | Free Air Operating Temperature | 0 | | 70 | °C |
| t_s (H) | Setup Time HIGH or LOW | 8 | | | ns |
| t_s (L) | P_n to $\overline{P_L}$ | 12 | | | ns |
| t_h (H) | Hold Time HIGH or LOW | 0 | | | ns |
| t_h (L) | P_n to $\overline{P_L}$ | 6 | | | ns |
| t_w (H) | $\overline{CP0}$ Pulse Width HIGH | 12 | | | ns |
| t_w (H) | $\overline{CP1}$ Pulse Width HIGH | 24 | | | ns |
| t_w (L) | $\overline{P_L}$ Pulse Width LOW | 18 | | | ns |
| t_w (L) | \overline{MR} Pulse Width LOW | 12 | | | ns |
| t_{rec} | Recovery Time $\overline{P_L}$ to $\overline{CP_n}$ | 16 | | | ns |
| t_{rec} | Recovery Time \overline{MR} to $\overline{CP_n}$ | 18 | | | ns |

Electrical Characteristics Over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ (Note 1) | Max | Units |
|----------|-----------------------------------|---|-----|--------------|------|---------------|
| V_I | Input Clamp Voltage | $V_{CC} = \text{Min}, I_I = -18 \text{ mA}$ | | | -1.5 | V |
| V_{OH} | High Level Output Voltage | $V_{CC} = \text{Min}, I_{OH} = \text{Max}, V_{IL} = \text{Max}$ | 2.7 | 3.4 | | V |
| V_{OL} | Low Level Output Voltage | $V_{CC} = \text{Min}, I_{OL} = \text{Max}, V_{IH} = \text{Min}$ | | 0.35 | 0.5 | V |
| | | $I_{OL} = 4 \text{ mA}, V_{CC} = \text{Min}$ | | 0.25 | 0.4 | |
| I_I | Input Current @ Max Input Voltage | $V_{CC} = \text{Max}, V_I = 10V$ | | | 0.1 | mA |
| I_{IH} | High Level Input Current | $V_{CC} = \text{Max}, V_I = 5.5V, \overline{CP1}$ | | | 40 | μA |
| I_{IL} | Low Level Input Current | $V_{CC} = \text{Max}, V_I = 0.4V$ | | | -0.4 | mA |
| I_{OS} | Short Circuit Output Current | $V_{CC} = \text{Max}$ (Note 2) | -20 | | -100 | mA |
| I_{CC} | Supply Current | $V_{CC} = \text{Max}, V_{IN} = \text{GND}$ | | | 20 | mA |

Note 1: All typicals are at $V_{CC} = 5V, T_A = 25^\circ\text{C}$.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25^\circ C$ (See Section 1 for waveforms and load configurations)

| Symbol | Parameter | $R_L = 2k$ $C_L = 15 pF$ | | Units |
|------------------------|---|-----------------------------|----------|-------|
| | | Min | Max | |
| f_{max} | Maximum Count Frequency at $\overline{CP}0$ | 45 | | MHz |
| f_{max} | Maximum Count Frequency at $\overline{CP}1$ | 22.5 | | MHz |
| t_{PLH} t_{PHL} | Propagation Delay $\overline{CP}0$ to $Q0$ | | 15 | ns |
| t_{PLH} t_{PHL} | Propagation Delay $\overline{CP}1$ to $Q1$ | | 15 | ns |
| t_{PLH} t_{PHL} | Propagation Delay $\overline{CP}1$ to $Q2$ | | 34 | ns |
| t_{PLH} t_{PHL} | Propagation Delay $\overline{CP}1$ to $Q3$ | | 15 21 | ns |
| t_{PLH} t_{PHL} | Propagation Delay P_n to Q_n | | 25 35 | ns |
| t_{PLH} t_{PHL} | Propagation Delay \overline{PL} to Q_n | | 31 37 | ns |
| t_{PHL} | Propagation Delay \overline{MR} to Q_n | | 42 | ns |

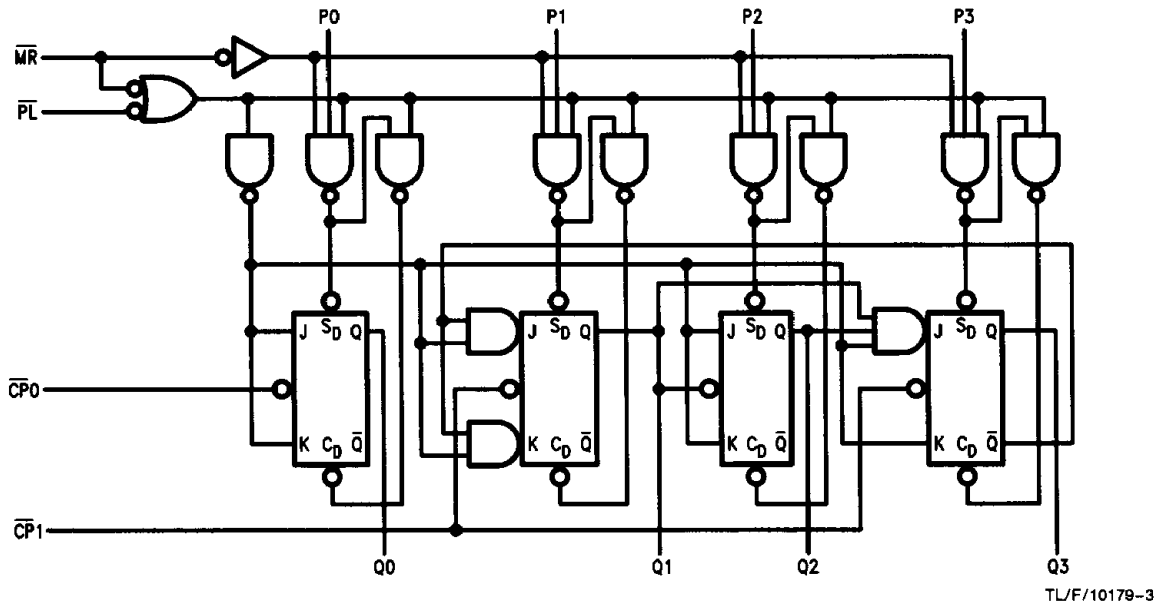
Functional Description

The '196 and '197 are asynchronous presettable decade and binary ripple counters. The '196 decade counter is partitioned into divide-by-two and divide-by-five sections while the '197 is partitioned into divide-by-two and divide-by-eight sections, with all sections having a separate Clock input. In the counting modes, state changes are initiated by the HIGH-to-LOW transition of the clock signals. State changes of the Q outputs, however, do not occur simultaneously because of the internal ripple delays. When using external logic to decode the Q outputs, designers should bear in mind that the unequal delays can lead to decoding spikes and thus a decoded signal should not be used as a clock or strobe. The $\overline{CP}0$ input serves the $Q0$ flip-flop in both circuit types while the $\overline{CP}1$ input serves the divide-by-five or divide-by-eight section. The $Q0$ output is designed and specified to drive the rated fan-out plus the $\overline{CP}1$ input. With the input frequency connected to $\overline{CP}0$ and with $Q0$ driving $\overline{CP}1$, the '197 forms a straight forward modulo-16 counter, with $Q0$ the least significant output and $Q3$ the most significant output.

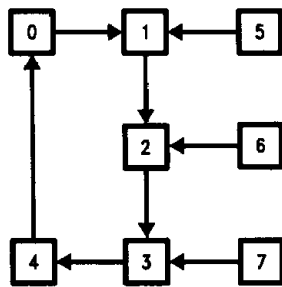
The '196 decade counter can be connected up to operate in two different count sequences. With the input frequency connected to $\overline{CP}0$ and with $Q0$ driving $\overline{CP}1$, the circuit counts in the BCD (8421) sequence. With the input frequency connected to $\overline{CP}1$ and $Q3$ driving $\overline{CP}0$, $Q0$ becomes the low frequency output and has a 50% duty cycle waveform. Note that the maximum counting rate is reduced in the latter (bi-quinary) configuration because of the interstage gating delay within the divide-by-five section.

The '196 and '197 have an asynchronous active LOW Master Reset input (\overline{MR}) which overrides all other inputs and forces all outputs LOW. The counters are also asynchronously presettable. A LOW on the Parallel Load input (\overline{PL}) overrides the clock inputs and loads the data from Parallel Data ($P0-P3$) inputs into the flip-flops. While \overline{PL} is LOW, the counters act as transparent latches and any change in the P_n inputs will be reflected in the outputs. In order for the intended parallel data to be entered and stored, the recommended setup and hold times with respect to the rising edge of \overline{PL} should be observed.

Logic Diagram

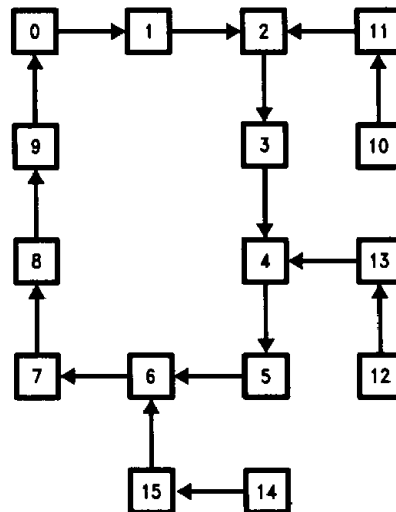


÷ 5 State Diagram



TL/F/10179-4

BCD State Diagram



TL/F/10179-5

Mode Select Table

| Inputs | | | Response |
|--------|----|----|---------------|
| MR | PL | CP | |
| L | X | X | Qn forced LOW |
| H | L | X | Pn → Qn |
| H | H | | Count Up |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial